Esprit

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The Project Synopses

Microelectronics and Peripheral Technologies

Volume 2 of a series of 8

September 1989

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The Project Synopses

Microelectronics and Peripheral Technologies

Volume 2 of a series of 8

September 1989

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2 Also in Materials

3 Also in III/V Technology

4 Also in Equipment

5 Also in Silicon Technology

GENERAL OUTLOOK OF ESPRIT

ESPRIT was launched in 1984 for a ten-year period, with three main objectives:

- to contribute towards providing the European IT industry with the basic technology it needs to meet the competitive requirements of the 1990s
- to promote European industrial cooperation in IT
- to contribute to the development of internationally accepted standards.

Building on the results obtained, and the experience gained in its first phase, the second phase of ESPRIT (launched in 1988) is designed to continue the successful approach of the first phase, based on the same objectives of improving the competitiveness of Europe's IT industry and its user industry on a worldwide scale. However, the scope has been somewhat extended, and among the main objectives and tools of ESPRIT can be stressed the following:

- The programme supports precompetitive R&D in those areas where the necessary critical mass exists and the gains made can be maintained and further developed.
- Further technology R&D projects are started in areas of promising industrial impact.
- Cooperation should be consolidated, both across IT sectors and between manufacturers and users, thereby creating a multiplier effect and spawning productive collaborative efforts.
- The scope is enlarged by undertaking a limited number of Technology Integration Projects (TIPs). These projects are aimed at meeting ambitious, well-defined industrial targets and require industrial effort on a very large scale.
- The efforts in preparation of international standards is intensified.
- Technology transfer in the IT sector is promoted with particular emphasis on the capabilities and the needs of small and medium enterprises (SMEs).

MICROELECTRONICS AND PERIPHERAL TECHNOLOGIES

Introduction

Within the general scope outlined above, 49 projects were launched in the first phase of ESPRIT in the domain of microelectronics and peripheral technologies, and these are either already completed or near completion. In the second phase of ESPRIT, 30 projects have already been launched.

A cross-reference list of projects identifiable by acronym is also provided. The present volume provides an inventory of the synopses of all ESPRIT projects (including those already terminated) listed sequentially in increasing project number order. A cross-reference list of projects identifiable by acronym is also provided. The synopses provide a brief description of the objectives, the technical content and the updated state of advancement of each project. A list of partner names, a technical contact address, as well as the starting date and the duration, are also given for every project.

General Overview

The competitiveness of the European Community in all advanced areas of information technology depends on mastery of state-of-art semiconductor technology supported by computer-aided design (CAD) capability. The market for integrated circuits (ICs) is expected to approach 60 BECU by 1992 and some 20% to 30% of this will be for application-specific integrated circuits (ASICs) required by electronic systems producers to reach optimised solutions and protect proprietary architectures.

A very substantial part of the work performed within ESPRIT addresses the specific needs of this latter strategic sector. Other areas covered include Compound Semiconductor Devices and ICs, Optoelectronics, and Peripherals.

The ESPRIT projects listed in the present volume can, in very general terms, be classified under four sub-areas, according to the functionalities pursued:

1) High-Density Integrated Circuits

2) High-Speed Integrated Circuits

3) Multifunction Integrated Circuits

4) Peripheral Technologies.

Within each sub-area, individual projects address issues related to technology, CAD, manufacturing equipment and materials.

The key topics covered by each sub-area can be summarised as follows:

1) The High Density sub-area covers a number of linked topics: integration of design and production for the fast turn-around of prototype ASICs, advanced technology for chip fabrication, application-specific architecture compilation, CAD integration and standards, VLSI validation and test, and equipment for integrated circuit manufacture.

2) Advances in the High Speed sub-area are required (on Silicon Bipolar and/or GaAs technologies) for such IT application areas as telecommunications, mobile radio and computers. The topics addressed are packaging, CAD and process development, with the aim of establishing a European capability for systems applications where substantial improvements in speed and packing density are mandatory for penetration of world markets.

3) The topics covered by the Multifunction Integrated Circuits sub-area include non-volatile memory macrocells, mixed analogue-digital circuits, three-dimensional ICs, optoelectronics, and smart power technology. All require combining, on a single chip, design and process functions which would normally be developed and optimised independently. The ability to manufacture a multifunction IC therefore presents a significant challenge in the integration of different materials and design constraints to achieve costs and performances which are competitive to a multi-chip approach.

4) The Peripherals sub-area covers technologies where the potential business impact is seen to be greatest, building on existing strengths in Community IT industries. Included are high density magnetic mass storage, magneto-optical drives, large-area flat-panel displays and electro-thermal ribbon technologies.

ESPRIT I PROJECTS

HIGH-LEVEL CAD FOR INTERACTIVE LAYOUT AND DESIGN

PROJECT NUMBER: 10

The objective was to define and demonstrate a CAD system for the design and layout of VLSI integrated circuits from the initial specification to the masks. Circuit complexity up to 1 million transistors was to be addressed. Reduced design times were the overall aim. The main topics under investigation included high-level design methodology based on Petri nets, hierarchic floorplanning with a high degree of automation, analogue and general cell design, data modelling and data base management.

The project ended in March 1987.

A prototype system has been produced which allows a specification expressed as a Petri net (type of flowgraph) as input and produces mask tapes as output.

- It incorporates a design methodology for analogue cells which has circuit performance optimisation properties.

- This system features a sophisticated interface to the circuit level simulation package and is technology-independent in its application. Tests of this system demonstrated its efficiency. The work-on-design rule independent description of cells has been completed. A translation procedure from a physical into a symbolic description of cells and back into a different physical representation has been described. The elaborated method has been applied to both NMOS, CMOS and bipolar circuit examples.

- Another major accomplishment was the verification of the operation of a multi-cache bus system by proving the correctness of the marking graph of its model. This model was described by means of high-level Petri nets (RTPN) and proved by using a methodology that permits a fast formal verification in place of the more usual slow simulation. Unfolding of the RTPN to an ordinary Petri net then leads to a correct and easy (one-to-one) hardware synthesis.

- The final revision of the design manual of 200 pages in length has been carried out entitled: "Design of digital systems using Petri nets". It contains all the important results on the design methodology.

- The data requirements of each tool of the CAD system have been defined. A data model, which is adequate for the relational DBMS of the design system, has been established in a close liaison between the project partners. A graphic representation, which shows both how the attributes are associated to the relations and the access mechanism, has been established.

- Software for placement of general cells has been developed. It is based on constructive initial placement, using a mixture of rules and algorithms. A simulated annealing placement improver has also been developed. This

software has been tested in a variety of technologies. The software has been integrated with the Oracle Data Base Management System on Apollo workstations, and with the PLESSEY MEGACELL Data Base Management System on DEC VAX. Studies have been made of the impact on future placement software of the power routing and hierarchy problems anticipated in future generations of technology.

Overall, the project has achieved its stated objectives in terms of the design and production of a CAD design. Validation of its performance, however, has not been demonstrated.

The feasibility of describing systems using the Petri net notation and the fact that this can be automatically translated into circuits and layout has been demonstrated. This translation can substantially reduce the design time for complex chips.

The work on analogue circuits carried out has also made a valuable contribution to the state-of-the-art knowledge in this area, the more so as analogue in combination with digital functions on the same chip is gaining in importance.

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PLESSEY RESEARCH LTD	*U*	*P*

Start Date	**Duration**	**Status**
01-OCT-83	*42 months*	*Finished*

ADVANCED INTERCONNECT FOR VLSI

PROJECT NUMBER: 14

The objective of this programme was to develop high density interconnect compatible with one micron MOS and Bipolar VLSI technologies. This interconnect technology was to feature four levels of low resistivity metal interconnect with high electromigration resistance and stable, low resistance contacts to the underlying silicon circuit.

The project ended, after a three month extension, in December 1987 having achieved its overall objectives and having demonstrated several advanced new techniques.

The main milestones of the programme were:

- demonstration of 3-layer metal at 5 micron pitch in September 1986
- demonstration of 4-layer metal at 3 micron pitch in March 1987.

The first main milestone was reached on time and several variants of the developed structures for non-nested vias and pillars were evaluated by means of the final test mask towards the final milestone.

A major technical difficulty was encountered while setting up the final process. Although good progress had been made with optimised aluminium for step coverage, it was discovered that these conditions did not fill small holes such as contacts and vias. The work was therefore restructured and new sub-tasks added in order to reach the final milestone with a three months' delay.

Eventually, the fabrication of 100% filled small vias with Al alloys has been demonstrated, in close collaboration with advanced equipment manufacturers.

Work on contact systems and tests on the reliability of polyimide and nitride have produced very good results.

All the partners make use of the developed interconnect results in their CMOS or bipolar processes. Plessey has notably transferred the developed 3-layer metallisation scheme to its CMOS process.

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TELEFUNKEN ELECTRONIC	*D*	*P*
THOMSON CSF	*F*	*P*

Start Date	Duration	Status
06-SEP-84	*36 months*	*Finished*

ADVANCED ALGORITHMS, ARCHITECTURE AND LAYOUT TECHNIQUES FOR VLSI DEDICATED DSP CHIPS

PROJECT NUMBER: 97

The objectives were:

- To produce a set of methods, algorithms and CAD tools for the design of digital signal processing chips in state-of-the-art CMOS technology using new advanced optimised circuit techniques and clocking schemes.
- To produce tools to support formal as well as interactive design from specifications down to chip layout. The CAD tools so produced should be capable of optimizing chip area and power dissipation for given system requirements.

Design methodologies and the appropriate design tools for several specific digital signal processing architectures have been developed. These architectures are:

A. Bit-Serial architecture

B. Cooperating Datapath architecture, restricted to linear pipelined bit-parallel hardwired structures within the project

C. pipelined Regular Array structures, restricted to systolic or semi-systolic arrays within the project

D. micro-coded Multi-Processor structures.

ACHIEVEMENTS AND RESULTS

A. Bit-serial

The work on the hardwired bit-serial architecture has resulted in a complete set of integrated tools to specify a filter, synthesise it in a wave digital form, simulate it on different levels, optimise the coefficients and the data-wordlengths, map the algorithm - including the control - into the bit-serial primitives and generate the complete layout.

A study of design methods for two-dimensional wave digital filters with approximately circular symmetry has been made. Besides the design of two-dimensional cross-antimetric filters, a new method has been worked out, which can be extended to any number of dimensions. Several structures for two-dimensional antimetric filters have been developed with a high degree of modularity.

The whole integrated CAD package is called CATHEDRAL-I, which is a fully operational silicon compiler from specifications to layout.

B. Cooperating Datapath

A novel carry-save technique and special circuits cells for overflow protection have been studied and documented with the intention to achieve 100 MHz clocking rate in a modern CMOS technology. This is very important in order to achieve the performance aimed at e.g. in the RACE programme, with more traditional and therefore cheaper technologies than GaAs.

The set of software tools that has been developed is embedded in the CATHEDRAL-III environment.

C. Regular Array

A standard module library which can be used to span most of the arithmetic-intensive operations in the area of image processing has been derived, and a composition methodology has been studied which can later be translated in a set of synthesis tools for regular array structures (not part of this project).

Self-test approaches for the concurrent sorting architecture have been investigated. A fault coverage of 100% for stuck-at and up to 99.6% for stuck-open faults have been obtained for a bit-serial word sorter. Two word-parallel bit-serial sorting networks have been implemented using MGE. The circuits occupy areas of 13.6 mm^2 and 36.6 mm^2 respectively.

D. Multi-Processor

In the project the main emphasis has been put on this type of architecture. It is most suited for a large majority of applications in the spectrum up to 1 MHz sample rate and it is addressing the implementation of more general real-time algorithms. The design methodology for this architecture has been derived from four large applications in speech processing and telecommunication.

This work resulted in a true silicon compiler called CATHEDRAL-II. It translates a behavioural, flowgraph-type algorithm description, expressed in the SILAGE language, into a dedicated multi-processor architecture. It allows the system designer to investigate and compare in an interactive way a number of silicon implementations of a certain digital signal processing algorithm.

The datapath of the chip is constructed from a customised set of parameterisable execution units. This customised datapath is generated automatically from the high-level behavioural specification. The set of available execution units is restricted to six: ALU/shift, Address Computation Unit, multiplier/accumulator,

comparator, normaliser, RAM/FIFO. A study has been made on the interprocessor communication protocols, addressing techniques and bus interconnection strategy. The results have been embedded in a software tool outside the scope of the project (IMEC).

Although the first CATHEDRAL-II prototype showed very promising results, the different exercises that have been done have shown that the inference mechanism, as implemented, was not efficient enough for larger examples and missed the robustness to handle complicated nestings of loops and conditionals. Therefore, a new inference mechanism has been implemented, based on demand driven rule firing, by which a higher efficiency is reached for much more complex examples (IMEC).

IMPACT OF THE PROJECT

A. Bit-Serial

CATHEDRAL-I has already been installed at different universities, research institutes and companies throughout the world. Besides installation at the partner sites, the software is also used at, amongst others, Italtel, RCA, University of California (Berkeley), University of Lund (Sweden), Institut de Microtechnique de l'Université de Neuchâtel (Switzerland), University of Sao Paulo (Brazil).

The CAD system has been successfully applied to the design of a viewdata filter (Philips, IMEC) and to the design of a PCM-FDM Transmultiplexer with a complexity of 35 000 transistors (Siemens, IMEC).

B. Cooperating Datapath

CATHEDRAL-III is oriented to the efficient synthesis of high-throughput digital signal processing circuits in which the clock rate/sample rate ratios vary between one and twenty.

A bit-parallel digital transversal filter, with real-time programmable coefficients, has been designed in a 1.5 micron CMOS technology. It has been measured and verified for a clock rate of up to 50 MHz. A third order wave digital filter has been designed by Siemens, and implemented on chip. The total chip area is 14.7 mm^2 (in a 2 micron CMOS technology) and the maximum measured clock rate is 50 MHz.

Other demonstrators are the integration of a Cordic algorithm and a digital video signal convertor (RGB to luminance/chrominance) with decimation filters (DMF). This last application will be used in a 140 Mbit/s video codec in order to replace analogue circuitry. The design is suited to be implemented with a 1.5 micron CMOS technology, yielding a chip with about 80 000 transistors on a total chip area of about 35 mm^2 (Siemens, IMEC).

C. Regular Array

At IMEC, architectures for the distance computation unit in a video codec have been investigated in cooperation with Alcatel/Bell Telephone. In addition several efficient semi-systolic architectures for one-dimensional and two-dimensional running order statistics filters have been developed.

D. Multi-Processor

Different instances of almost all required execution units have been put on MPC in a 3 micron and a 2.4 micron double metal CMOS technology and tested out successfully. This has been done partly outside the scope of the ESPRIT 97 project (IMEC). A 1.6 micron version has also been developed by Philips outside the scope of the project.

From this a powerful microcode-rom based multi-branch controller architecture has been selected (IMEC, Philips), though other architectures such as a simple FSM can also be incorporated. Alcatel/Bell has studied one particular controller architecture, the binary decision machine, and has translated this into a set of specifications for dynamic ROM and RAM structures.

The CATHEDRAL-II version, as delivered at the end of the project, has proven its usefulness in different applications. Within Philips, CATHEDRAL-II has been used in order to build PIRAMID, an operational silicon compiler fitted to Philips' requirements. Different designs have been completed. CATHEDRAL-II and/or PIRAMID are being used intensively within IMEC, Philips and Alcatel/Bell Telephone.

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Start Date	**Duration**	**Status**
01-SEP-83	*60 months*	*Finished*

COMPOUND SEMICONDUCTOR MATERIALS AND INTEGRATED CIRCUITS - I

PROJECT NUMBER: 232

The overall objective of this project was to establish gallium arsenide digital integrated circuit technologies using the GaAs MESFET, high electron mobility transistors (HEMT/TEGFET) and heterojunction bipolar transistors (HBT) as the active circuit elements. These circuits will be configured to enable the speed and power advantages of GaAs over silicon to be suitably demonstrated.

This project is now successfully terminated.

It was started in competition with project number 522. At the decision point (the end of the first year), all the demonstrator milestones had been met. These were:

- Fully operational 1K SRAM in MESFET technology with 3-6 ns access time and a typical power consumption of 80 mW.

- 19-stage TEGFET circuits with gate delays of 20 ps.

- 19-stage heterojunction bipolar circuits with delays of 50 ps.

The achievements of the consortium in fabricating all the demonstrators defined at the outset of the project was further enhanced by the fact that the MESFET demonstrator and the TEGFET demonstrator had performances equal to the current world state of the art.

In addition, complementary programmes had been set up in the areas of lithography, dry processing, the selection of suitable dielectrics, material assessment techniques and specific process technologies.

Finally, the complementary technological tasks carried out in this project have identified the main areas of work leading towards a production of digital GaAs ICs. Project numbers 843, 971 and 1128 have resulted in ESPRIT reallocating the resources in a more efficient way towards the establishment of a European capability in manufacturing GaAs ICs.

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Start Date	**Duration**	**Status**
01-NOV-84	*12 months*	*Finished*

SUBMICRON BIPOLAR TECHNOLOGY - I

PROJECT NUMBER: 243

The overall objective of this programme is to develop specific bipolar submicron technology suitable for manufacturing very high performance integrated circuits, such as high speed circuits for Electronic Data Processing (EDP) and Digital Signal Processing (DSP).

Two main milestones are scheduled:

- End of year 3 (March 1988); demonstration of a gate delay capability of 100 ps at a complexity level of 10 Kgates.
- End of year 5 (March 1990); demonstration of a gate delay capability of 50 ps at a complexity level greater than 20 Kgates.

After year 1, two new research tasks were added to complement the work programme:

- Development work and processing schemes for sidewall base contact structures, providing very low base access resistance and enabling a good symetric performance of the transistor.
- Research and development of high performance polymers for insulation between metallic interconnection layers in a submicron technology. These performant polymers would be polyimide-based resins.

After two years a process using 1 micron design rules was set up and the first test mask was completed. The lateral isolation between components is provided by deep trenches and a polysilicon layer has been added between the metallic contact and the monosilicon emitter region. Implementation of a 21-stage ring oscillator has shown that propagation delay times lower than 100 fJ and speed power products of less than 100 fJ were reached.

By the end of year 3, the capability of this technology to implement complex, high speed VLSI circuits had been demonstrated with a 4x512 bit shift register (35 000 transistors) in which operation at 950 MHS for 1.8 mW per stage was obtained. The layout used a "sea of cells" approach implemented with an interconnect system consisting of one polycide and two metal levels.

During the fourth year, the sequence of a double poly self-aligned emitter structure was worked out, a second test mask was processed and the design of the final demonstrator has been started.

Three of the partners intend to implement the developed technologies progressively following the achievement of the major milestones in 1988 and 1990. Likely applications are:

gate arrays and programmable ROM, microcells for DSP ASICs and high-speed analogue/digital-digital/analogue converters, and very high speed ASICs for high bit rate telecommunications.

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CEMOTA	*F*	*P*

Start Date	**Duration**	**Status**
01-JAN-85	*60 months*	*Running*

HIGH YIELD AND HIGH RELIABILITY ULSI SYSTEM (HYETI)

PROJECT NUMBER: 244

This project ended in September 1985.

The objective of the project was to develop the design methodology, design tools and architecture necessary to achieve high yields on ULSI (Ultra Large Scale Integration) and WSI (Wafer Scale Integration) integrated circuits. The yield models, specialised architectures and focussed CAD tools required for reconfiguration at the end of manufacture were to be studied in this project. Because defect densities in modern process technology are such that working wafer scale circuits can only be manufactured by introducing redundancy into a chip, enabling the defects to be avoided by reconfiguration during production, this work was of high value.

The need to produce a demonstrator to focus the many multi-discipline, interrelated facets of the WSI design problem was an important consideration from the start of the project.

As a conclusion to the work on yield analyses, the project found that the most satisfactory way to handle yield prediction for a specific topology is by graphic simulation.

Two architectures were selected for WSI implementation after a wide investigation, namely, a 2-D Fast Fourier Transform (FFT) processor and a processor array. After extensive investigation, the decision was taken during this pre-project study to design and manufacture, in the follow-up project, a 4 Mbit static RAM, a systolic array and a reconfigurable 16-bit microprocessor.

As this was only a one-year pre-project to investigate the feasibility of WSI, only limited results have been achieved. The work, with an adjusted workplan and modification in the partnership, has been continued under project number 824.

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Start Date	**Duration**	**Status**
01-OCT-84	*12 months*	*Finished*

SOI MATERIALS AND PROCESSING: TOWARDS 3D INTEGRATION

PROJECT NUMBER: 245

The objective was to investigate new silicon technologies suitable for three-dimensional (3D) integration in order to achieve the possibility of higher density integration, higher speed of operation and multifunctional signal processing. Three main technological steps were explored:

- The growth of SOI active layers having electronic properties needed for the realisation of high quality devices and circuits;

- The stacking of two active levels in a way that avoids any degradation of already built devices;

- The single level SOI processing for the fabrication of individual components and for their connection; also the development of a process incorporating two active layers.

The project finished in December 1987; final demonstration was presented during the ESPRIT Conference in November 1988.

The first two years' experimental work demonstrated the capacity to fabricate monocrystalline SOI layers compatible with the underlying bulk silicon layers and with limited influence of the first device level on the SOI characteristics. Specifically:

- Industrial E-beam equipment was built for SOI preparation and two different research laser systems were optimised.

- Unified test structures and characterisation methods were adopted for quantitative comparison of the crystallisation techniques of E-Beam, Laser Zone Melting and CVD epitaxy.

In parallel, design options and product application studies showed two choices for 3D circuits:

- conventional applications (high density - high performance VLSI)

- system applications (specialised superimposed layers; performance independence of different functions).

One major conclusion of the application study was that 3D SOI CMOS for VLSI is unlikely to provide sufficient benefit, in terms of packing density and circuit speed, to compete with single level technologies using bulk or SOI substrates. In contrast, the development of silicon technologies where devices of different types (e.g. CMOS, bipolar and power transistors) can be fabricated on a single chip,

was demonstrated as an important application area for 3D SOI. Such mixed technologies are difficult to produce in a single level of silicon as the requirements of the different device types often conflict. However, using a 3D SOI approach, the development of a mixed technology with individual optimisation of the separate device levels can be envisaged.

In the light of these findings, the orientation of the current project and the end of year 3 demonstrator has been focused on the development of a "smart power" technology using a 3 micron CMOS SOI level to control medium current/voltage (1 A/50 V) LDMOS bulk transistors. The chosen demonstrator is a first step towards the integration of very different functions on the same chip in a way which allows the independent optimisation of each one and their complete dielectric isolation, thus opening the route for complex system integration on chips allowing more reliability and better performances. The particular application considered is a stepper motor controller using a gate array design approach for both the CMOS and LDMOS levels. At this stage, a "mezzanine" layout has been adopted where the SOI devices are displaced laterally from the underlying bulk devices.

On the materials development side, significant improvements in the SOI starting material, especially the use of selective epitaxial growth of silicon in the seed windows, together with refinements of the laser and electron beam recrystallisation systems, have allowed the production of device-grade SOI compatible with the requirements of the end of project demonstrator. High quality SOI devices have been produced, and fine geometry bulk CMOS devices which had undergone SOI recrystallisation under similar conditions were found to be essentially unaffected by the process. These device results confirm the viability of the demonstrator production technique. Full demonstrator device batches were processed in December 1987. A working chip, integrated in a prototype board and activating a stepper motor, was shown during the ESPRIT Conference in November 1988.

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Start Date	**Duration**	**Status**
01-JAN-85	*36 months*	*Finished*

CAD METHODS FOR ANALOGUE GAAS MONOLITHIC ICS

PROJECT NUMBER: 255

The objective was to make available a comprehensive CAD package, named MMIC-CAD, suitable for the design of GaAs ICs operating up to 18 GHz. The package uses the development of a full CAD library of theoretical models and experimental data for passive elements and active components required for the design of GaAs analogue ICs.

The work started by deriving physical models and equivalent circuits for different types of MESFET and passive elements both for lumped and distributed approaches. The next step was the CAD of groups of passive and active devices for the integrated implementation of elementary functions. Here, besides circuit analysis, coupling between adjacent elements and thermal distribution have also been simulated. In the successive phase, analogue ICs, defined as high-level functional blocks, have been considered with special analysis programs. The final CAD program includes package effect evaluation and error-sensitivity analysis. Interactive optimisation have been organised in a user-oriented, transferable package.

The initial C and X-band investigation has been extended up to 18 GHz. The CAD capability has been proven with different GaAs IC demonstrators, including submicron dimension devices.

After the first two years, the work was considered to be on target and in line with the original objectives. However, following a major review and in the light of updated requirements for activity in this area, the work programme was re-organised towards a more focussed final objective. The required negotiations have undoubtedly introduced some delays but the new work plan was geared towards achieving the final objective within the originally planned timescale.

The results of this project are expected to benefit a small but potentially highly important application area, that of high frequency telecommunications. They will be available for possible exploitation during 1990.

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Start Date	**Duration**	**Status**
20-DEC-84	*48 months*	*Finished*

INTEGRATED OPTOELECTRONICS ON INP

PROJECT NUMBER: 263

The general objective is to significantly increase the data rate in optical transmission systems, by the use of high performance devices with a variety of multiplexing techniques, mainly with the use of different wavelengths.

In the first three years, activity was focused on achieving and utilising single mode discrete functions suitable for subsequent monolithic integration. Full hybrid integration during the first three years is followed in years four and five by monolithic integration of some important functions, e.g. an integrated light source with independent control of both output power and wavelength using electro-optic effect and/or current injection to tune a distributed feedback (DFB) laser.

The work on materials is oriented towards reproducible growth of high quality, high homogeneity, large area heterostructures suitable for low threshold current density and well-controlled wavelength lasers, for low doped photodetectors and low loss waveguides.

The second part of this programme is now addressing the development of the technology needed for the fabrication of the electronic devices in a form which can be integrated with the optical devices. A range of devices is investigated and compared. As a result of the importance of longer wavelength operations, all this work is based on InP-based semiconductor compounds. An important additional potential benefit of the project is that these materials are also expected to yield very high performance in purely electronic applications. Thus the programme may lead to improved electronic functions as well as sophisticated opto-electronic circuits.

The first integrated structure, a DFB laser with a tuning section, has been realised. Good control on laser manufacturing has been demonstrated (threshold current density <1.5 kA.cm^{-2}, wavelength dispersion <3 nm) and short cavity lasers with bandwidth higher than 8 GHz have been fabricated.

Finite element techniques have been integrated into user-friendly packages to model optically integrated devices easily and precisely, and applied to:

- the design of an optical demultiplexer
- the evaluation of the guiding properties of the very low loss structure (0.04 dB/cm), previously demonstrated.

This is forging a strong link also between the modelling and fabrication partners.

Important results have been obtained on operating integrated receiver circuits. The sensitivity of an Optoelectronic IC (OEIC) consisting of an InGaAs PIN detector with a JFET achieved a world record in sensitivity of -32.5 dBm at

560 Mbit/s. This is a very important result because the gap between hybrid and monolithic OEIC is beginning to be eroded.

This project, in debugging the opto-electronic monolithic integration which has been found more difficult to achieve than forecast, is playing a pilot role in a wide range of projects, dealing with low cost optical systems, in the RACE programme.

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Start Date	**Duration**	**Status**
15-DEC-84	*60 months*	*Running*

AUTOMATIC DESIGN VALIDATION OF INTEGRATED CIRCUITS USING E-BEAM

PROJECT NUMBER: 271

The objective is to produce a prototype system capable of automatic error diagnosis of VLSI devices.

The chosen approach is to be based on utilizing the observability facilities of E-beam equipment.

In order to achieve the above, the following will need to be carried out:

- interfacing to CAD software
- pattern recognition for automatically positioning the E-beam
- development of a global methodology to define the diagnostic strategy
- development of new hardware for enhancement of E-beam performances.

Furthermore the following problems will need to be solved:

- computer control of the E-beam system
- identification of circuit elements
- test pattern generation for electron beam debugging
- design for electron beam testability
- electron beam equipment development.

Following the completion of the first phase of the project which included the definition and preliminary investigation of all aspects for the design of a fully computer controlled E-beam testing system, the three industrial partners have installed at their premises core systems that are now fully operational.

Some of the key features already included in the core systems are:

- interfaces between CAD and E-beam systems
- pattern recognition
- hardware and software for computer control.

The results up until now satisfy all the realistic goals set at the beginning and following the first phase. These results are at least state-of-the-art as

exemplified at the various presentations and demonstrations given by the partners.

The E-beam design validation and testing technique is a new and very promising one. Its impact and time horizon for industrial applications depends strongly on the refinement of this or other competing techniques (e.g. scan design) that may emerge. The complete system is expected to be available by the end of 1989. Approaches have been received from two independent vendors of such systems with a view to marketing a product based on the prototype system developed in the project. British Telecom are meanwhile selling waveform averaging equipment based on one of the results of the project.

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Start Date	**Duration**	**Status**
01-DEC-84	*60 months*	*Running*

SUBMICRON BIPOLAR TECHNOLOGY - II

PROJECT NUMBER: 281

The objective is the development of a bipolar technology for high speed data and signal processing products. The generation of bipolar technology in production at the start of the project was characterised by minimum feature size of 2 micron, a delay time of about 350 ps and an integration level for gate arrays of about 2500 gates.

The project aimed at developing a technology with a minimum feature size of 1 micron, a self-aligning transistor structure with delay times below 100 ps, a multilayer metallisation technique of up to four layers, and an integration level of about 50K gates. In the area of high speed data processing, such a technology will increase the performance by minimizing the number of inter-connection lines among the chips and by increasing the reliability. Both require an increase of the integration level and a reduction of the power delay product. The 10 Mips capacity of present mainframe computers could be increased to about 40 Mips by means of this new technology. In the area of signal processing, the main advantage results from a reduction of the gate delay. The new technology would allow an increase of the signal processing speed of presently about 600 Mbits to more than 2 Gbits.

It was intended to achieve the above objectives in three stages characterised by the following gate delay and power delay product: 200 ps and 0.4 pJ; 100 ps and 0.1 pJ; less than 100 ps and less than 0.1 pJ.

The first demonstrator, a 10K gate array, was available on schedule mid-1986. The device is characterised by the following features: minimum structure size (mask dimension) 2 micron, minimum metal pitch 6 micron, 3-layer metallisation technique, self-aligned base-emitter structure, gate delay 200 ps, speed power product 0.4 pJ. The measurement results showed that both DC and AC parameters are meeting the specifications. Furthermore, the yield results indicated a sufficient state of maturity of the processing technology (OXIS III) to produce bipolar arrays with 10K gate complexity.

The second demonstrator, a 4K random access memory with an access time of less than 5 ns was demonstrated in March 1987, three months ahead of schedule. The high performance of the second demonstrator's technology is mainly due to a reduced base width and reduced lateral dimensions using a 1.0 micron stepper lithography. The metal pitch was decreased to 5 micron including non-nested vias between the first and second metal layer.

For the realisation of the second demonstrator, a 4-layer metallisation scheme was not needed. However, as a complement to the memory development a testchip was developed for 4-layer metallisation with a metal pitch of 4 microns.

During the fourth year the concept development for the third demonstrator and its technology have been worked out. Key features are a packing density of >5000 devices per mm^2, a delay time of 70 ps at 800 uA gate current and a power delay product of 40 fJ (single ended logic, three level series gating). The gate current will be programmable in three power steps (200 uA, 400 uA and 800 uA). This demonstrator will contain about 7K gates and will demonstrate a technology which will enable the realisation of 25 to 30K gate arrays within a chip area of less than 150 mm^2.

The production of the ECL-Gate Arrays was started in a new pilot line at Siemens in the first quarter of 1987. These circuits are primarily intended to be used in advanced computers and are now available for all other user companies.

The results achieved with project 281 have enabled Siemens to start the development of a new family of gate arrays based on an improvement of the design rules previously used to assess the maturity of the developed technology (OXIS III) to produce bipolar gate arrays with 10K gate complexity. These new design rules enable a reduction of the speed-power product by approximately 40% and an increase in the packing density of approx 30% (OXIS III H). This new gate array family provides a programmable speed-power product with 3 power steps where power dissipation amounts to 1 W per 1000 gate functions. The complexity of these arrays varies from 1.5K to 13K gate functions. The 13K gate array has been available since September 1988.

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Start Date	**Duration**	**Status**
01-JAN-85	*60 months*	*Running*

ASSESSMENT OF SILICON MBE LAYERS

PROJECT NUMBER: 305

The objective of this project was to improve the characteristics of silicon epitaxial layers grown by Molecular Beam Epitaxy (MBE). Capability of growing structures for microelectronic devices, application of appropriate methods to assess the epitaxial material and aspects of improved Si MBE process control were also addressed.

The workplan was divided into three objectives:

a) Growth of silicon layers by Molecular Beam Epitaxy.

b) In situ measurement of deposition conditions.

c) Implementation and development of techniques for the characterisation of MBE layers.

This information was used to optimise growth conditions.

For objectives a) and b), submicron n (Sb) and p (GaAs) doped MBE layers have been grown and analyzed in detail and the results used for in situ doping control. Multi-layer structures for high frequency device applications have been made and assessed showing flat doping profiles and sharp transitions. Spreading Resistance profiling, SIMS and preferential etching have been proven to be the most useful set of assessment techniques. For objective c), ISA RIBER, who joined the project in June 1987, worked on the development of an improved process control instrumentation, based on the use of a spectroscopic ellipsometer.

Silicon MBE is potentially a key process in the production of future generations of Si and Si-related devices. As a first approach, using the benefits of low growth temperature and precise control of layer thickness and doping profiles in any sequence, it is well suited for high speed devices and other integrated circuit applications. Furthermore, Si MBE also offers advantages for three-dimensional integration, because local epitaxial structures can be realised if a prepatterned substrate is used. Finally, utilizing the wide choice of material combinations and layer numbers made available, Si-MBE can open up a broader field of application for novel devices, e.g. SiGe heterostructures and superlattices, and heterojunctions with III-V alloys. This project has been contributing to these objectives by further improving the quality of the layers achievable by MBE. Additionally, a range of characterisation techniques for the assessment of the MBE material have been produced, which may find a broad application in the characterisation of Si films.

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Start Date	**Duration**	**Status**
01-FEB-85	*36 months*	*Finished*

PLASMA DEPOSITION TECHNOLOGY FOR MAGNETIC RECORDING THIN-FILM MEDIA

PROJECT NUMBER: 334

The objective is to exploit the potential advantages of a significant increase in recording capacity when metallic thin films, instead of conventional oxide particles, are used as the basis for magnetic recording media. In order to develop such a technology, the interdependence of substrate materials, thin magnetic layers, overcoats, heads and drive systems need to be assessed, developed and produced accordingly.

Leybold-Heraeus is responsible for the development of various deposition methods, e.g. sputtering, evaporation and plasma-CVD for the magnetic layer stack, while the definition of the quality standards of the disks and their possible implementation into a disk drive system has been entrusted, since October 1987, to SAGEM, which is also responsible of the evaluation of differently prepared media.

Among the different deposition methods, the sputtering has reached the most advanced status. At Leybold-Heraeus a sputtering system, suitable for the study of production conditions, has been designed and built. The machine is a vertical in-line system for double-sided disk coating and provides the best conditions for continuous production and for a high disk quality with a minimum risk of defects. The process technology for fabrication of disks with longitudinal recording has developed so far that the quality can compete with other good quality disks available on the market but the maximum storage capacity is expected to be achieved by vertical recording. For this purpose, special emphasis has been put on carbon overcoat for mechnical and chemical protection of the recording layer. Complete layer systems were deposited, both in the above mentioned machine on hard disks and in a large roll coater on foils for the industrial production of floppy disks, with promising results.

Media studies by the partners clearly demonstrate the potential advantage (substantial increase in recording capacity) of thin magnetic layers over conventional oxide particles for high density recording. However, the switch-over to thin film media requires many modifications of the standard production technology. Nevertheless, tribological problems between heads and disc still remain the actual drawbacks in vertical recording. Strong involment of heads manufacturers is necessary to overcome these problems and to define the needed standard heads and the subsequent characteristics of media. Accordingly, the work will now focus on hard discs for longitudinal recording and on protective/lubricating layers for use in Winchester-type drives. The new production technology of thin film should also be developed to ensure the best quality and reproducibility in a future production line.

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Start Date	**Duration**	**Status**
01-APR-85	*60 months*	*Running*

PHYSICAL-CHEMICAL CHARACTERISATION OF SILICON OXYNITRIDES IN RELATION TO THEIR ELECTRONIC PROPERTIES

PROJECT NUMBER: 369

The objective of the project was to investigate the feasibility of implementing a process step based on silicon oxynitrides by establishing:

a) the relationship between the physical-chemical and the electrical properties of silicon oxynitride films

b) the relationship between the physico-chemical properties and the growth parameters.

Work on oxynitrides is important in view of the possible applications of these films in IC technology, for instance in MNOS-based non-volatile memories and in submicron MOS devices.

Towards a), a large number of material characteristics of silicon oxynitrides have been generated. This knowledge is very important for assessing the improvement of the cost/performance ratio and the reliability of future generations of integrated circuits.

Towards b), extensive studies into the basic understanding of the growth and characteristics of LPCVD and thermally grown silicon oxynitrides have been carried out.

Concerning the LPCVD films, the following three technologically important conclusions have been drawn:

- The stress in the silicon oxynitrides is lowered upon introduction of oxygen in the nitride lattice, whereas the oxidation resistance is comparable or even better than that for the nitride. Accordingly, the "bird's beak" length in a LOCOS process, using a single oxynitride layer instead of the conventional nitride/pad oxide structure, is considerably shortened without any increase in the number of defects.

- For the application in MNOS type devices, the oxynitrides with the ratio of $O/(O+N) = 0.1 : 0.2$ have been proved to be the most suitable films.

- The hydrogen chemistry in the films is extremely important for various electrical and optical properties.

In the last year emphasis has been given to the preparation of oxynitrides by Rapid Thermal Nitridation (RTN) of silicon oxide films, because of the shortened process times which allow prevention of the redistribution of impurities, induced otherwise in a conventional high temperature process step. Optimum nitridation

conditions for thin (15 nm) layers to be used in submicron MOS transistors have been established.

Concerning the implementation of oxynitrides in devices, a 64K SRAM with a lateral isolation scheme consisting of a RTN silicon oxide film capped with a LPCVD Si_3N_4 layer, is now in production at Matra. A decrease of bird's beak length from 0.5 micron down to 0.2 micron was achieved.

Non-volatile memory devices have been fabricated at IMEC. In particular, SONOS structures with better retention and endurance have been prepared. Application of oxynitrides as tunnel dielectrics in EEPROM cells has also been performed, the results of which confirm the improvement in yield associated to the nitridation.

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MATRA HARRIS SEMICON.	*F*	*P*
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Start Date	**Duration**	**Status**
01-DEC-84	*48 months*	*Finished*

SILICON-ON-INSULATOR SYSTEMS COMBINED WITH LOW TEMPERATURE SILICON EPITAXY

PROJECT NUMBER: 370

The objective of this project was to obtain single crystalline layers of silicon-on-insulator (SOI) with thicknesses from 0.5 micron to 30 micron, for a variety of applications. The results are potentially applicable both to silicon-on-insulator, for high performance integrated circuits, and as alternative to dielectric isolation processing.

- A new strip-heater system has been developed for the recrystallisation of full wafers based on focussed high-pressure mercury lamps.
- Recrystallisation experiments have been performed with focused laser beams and with the stripheater system.
- A detailed study of the influence of all process parameters for both techniques has been carried out.
- Successful seeded and unseeded recrystallisations have been performed with both techniques leading to good quality material. Stripheater layers of between 0.5 micron and 10 micron have been directly recrystallised with good success. In both cases good electrical characteristics have been obtained in test devices.
- Epitaxial thickening of thin SOI layers has been performed on limited as well as large area structures.
- A range of trench etching equipment has been evaluated and a system has been purchased and installed. Very good trench etching has been achieved up to a depth of 20 micron. Oxide-polysilicon sandwich layers have been evaluated as the best choice for trench filling.
- The design of a combined insulator and epitaxy equipment for the photochemical deposition of insulators and silicon has been completed. This technique has then been abandoned since it became clear that it was not commercially viable.

The project has demonstrated that the methods used, based on lamp and laser beams, are technologically feasible but not, as yet, economically viable. In particular, the lamp re-crystallisation has been proven as the best approach for material synthesis if 0.5 micron or thicker layers are required, such as for smart power and high voltage applications, whereas laser re-crystallisation can be viewed as a viable method for 3-D integration (see project number 245).

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MIETEC	*B*	*P*

Start Date	**Duration**	**Status**
01-DEC-84	*36 months*	*Finished*

OPTICAL INTERCONNECT FOR VLSI AND HIGH BIT-RATE ICS

PROJECT NUMBER: 380

The objective of this programme was to investigate the use of optical interconnection between VLSI and high bit-rate ICs. As the operating speed and the complexity of microelectronic circuits increases several packaging and interconnection problems arise. At high bit rates the input/output pins of packages and printed circuit interconnections between packages must be treated as microwave transmission lines for impedance matching and crosstalk suppression. As circuits grow more complex, the pin count in the package increases creating potential reliability problems and excessive package cost. The use of optical rather than electronic interconnection is expected to circumvent these problems.

The inherent wide bandwith and crosstalk immunity of optical transmission media permits very high bit rate signals to be readily distributed. Because of this, many lower bit-rate signals, each of which would conventionally employ a package pin, can be multiplexed together to form an easily transmitted, high bit-rate, optical signal which leaves the integrated circuit package via an "optical pin". During the course of this project the application and implementation of optical interconnection have been assessed.

This programme investigated the role and capability of interconnection and got underway in early 1985. Work has included design studies of the performance, cost and implementations of optical sources and detectors and the choice of optical fibre for optical interconnect. The limitations of optical interconnect have been assessed in terms of power budgets and bit rates and the technology has been studied considering various communication protocols, IC performance boundaries and the impact on processor architectures. Limited experimental work has been done on investigating low cost techniques for fibre to chip interfaces and for the incorporation of optical fibres into printed circuit boards.

This one year project has been continued with project 986 in which experimental investigation of the optical interconnection solutions developed here took place.

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TELETTRA S.P.A.	*I*	*P*

Start Date	**Duration**	**Status**
01-DEC-84	*12 months*	*Finished*

MOLECULAR ENGINEERING FOR OPTOELECTRONICS

PROJECT NUMBER: 443

Optics and microelectronics will increasingly co-exist in the form of active or passive optical interconnects between microelectronic chips, mixed opto-electronic devices and purely optical devices as part of mixed opto-electronic systems. Furthermore organic electro-optic and non-linear optical materials can find application in logic elements, large band modulators, tunable parametric amplifiers and emitters in transmission and signal processing systems. The objective of this project was to provide a basis for the essential knowledge of the development of molecular-based IT devices. The progress achieved includes the following:

- The assembly of a reliable code for the prediction of the molecular beta coefficient from atomic coordinates.
- Synthesis and demonstration of excellent properties in pyrazoline and polyene molecules predicted from the above.
- The development of an efficient routine for searching the crystallographic data bases for active molecules of suitable symmetry for $X^{(2)}$.
- Knowledge of the effects of hydrogen bonding on hyperpolarisability.
- A methodology to calculate the static polarisability and hyperpolarisabilities of molecules within the Routine Hartree Fock (RHF-Sum Over States and RHF-Finite Field frameworks).
- A methodology to calculate the static polarisability of infinite regular polymers within the RHF-Sum Over States framework.
- Identification of various bonding patterns capable of high electronic responses.
- The setting up of relevant facilities for the characterisation of beta and $X^{(2)}$.
- The synthesis and dipping of a range of tailor-made molecules from which high second harmonic generation has been observed.
- The attachment of active molecules to a polyester backbone to give liquid crystal phases. Addition of beta has been obtained by aligning under an electric field applied above T_g and cooling to the immobile phase vectorial.
- Quantification of the factors which govern the lattice symmetry for the polar molecules of interest is now well underway and a number of effective routines have been written to model crystallisation.

- The successes in L-B and liquid crystal techniques, motivated by the desire to construct planar waveguide arrays for integrated optics. L-B technology has highly benefited from this collaboration, and the knowledge of deposition conditions, structural properties and nonlinear properties, started from almost nil at the onset of the Project, reached a level where technological follow-ups are in view.
- The development of ultrafast ultrasensitive spectroscopic or I-R signal processing tools (PASS).

All the above points achieved in this 3-year project are a significant step towards the development of devices for signal processing and optical computing. However, other specific aspects such as packaging, electrode deposition, integration of devices onto arrays, etc need to be addressed in parallel with the material studies, before such devices can be realised.

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ICI	*UK*	*P*

Start Date	**Duration**	**Status**
31-DEC-84	*36 months*	*Finished*

IMPROVEMENT OF YIELD AND PERFORMANCE OF ICS BY DESIGN CENTRING

PROJECT NUMBER: 456

The objective was to investigate mathematical means to shift the parameters of a integrated circuit (IC) to a location (design centre), where they can fluctuate in a wider range without impairing the function of that circuit. This increases the fabrication yield. The same method can be used to enhance the performance of such circuits.

An already existing computer program for design centring and a program for the improvement of the circuit performance was improved and adapted to the special problems occuring in the design of VLSI-circuits in the participating companies.

The involvement of industrial firms ensured the availability of transistor models which reflect the properties of their IC-fabrication lines.

The project finished in December 1986.

The main deliverables were:

- An optimisation program package based on the well-known network simulator SPICE called MCSPICE.

- A user-friendly interpreter and an intermediate results processor for run-time control for the above program.

- Pre and post processors for workstation-based input and output.

The program was tested successfully on circuits with 16 parameters, but that is not thought to be the maximum limit. Example circuits and physics-based models from the industrial partners were used to test the effectiveness of the program as the basis for a real industrial design tool with promising results.

Although the project achieved its initial objectives, which are thought likely to be the basis of a useful industrial design facility, its continuation was not thought to belong to the precompetitive ESPRIT programme.

The impact of the results is expected as industrialisation, which should now be possible initially within the participating organisations.

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Start Date	**Duration**	**Status**
01-JAN-1985	*24 months*	*Finished*

MATERIALS AND TECHNOLOGIES FOR HIGH MOBILITY TFTS FOR LC DISPLAY BUS DRIVERS

PROJECT NUMBER: 491

The progress in the development of Thin Film Transistor (TFT) for pixels or drivers is a key step towards the evolution of alternative displays technologies (such as LCDs) which can replace CRTs when low consumption and portability are required. These TFT technologies can also impact other applications in large-area microelectronics such as motionless scanners.

The objective of this project was to develop polycrystalline silicon (p-Si) thin films and technologies for column-bus and line-bus drivers to replace external ICs for peripheral driver circuits of active matrix liquid crystal displays (LCDs).

The main task was to develop a low-temperature deposition process for the thin semiconductor films compatible with the glass substrates used for the LC display. The investigated deposition processes were Plasma Enhanced CVD and e-gun evaporation, whereas Low Pressure CVD was used to establish the Thin Film Transistor (TFT) process technology. Furthemore, elementary TFT circuits, suitable for bus driver shift registers, were investigated and developed. Driver prototypes of short length were also combined with LCD matrices and tested.

The first three year milestones were achieved on schedule.

- Polycrystalline Si films prepared below 600°C on borosilicate glasses were processed to produce TFTs.

- TFTs, prepared from e-gun Si films deposited at 550 °C, were using an Atmosperic Pressure CVD deposited SiO_2 layer. These TFTs exhibit field effect mobilities up to 16 cm^2/V and enable a better yield than TFTs using plasma-processed gate insulators.

- With PECVD, the capability exists to prepare Si_3N_4 transistors with field effect mobilities up to 35 cm^2/Vs in Si layers deposited at around 0 °C

Using these deposition processes there is no need to use the costly process of ion implantation to obtain TFTs with the requested characteristics. Furthermore, at the above mentioned deposition temperatures high quality glass substrates can be used instead of the expensive quartz substrates needed for higher temperatures. Nevertheless, additional investigation will be necessary to reduce the deposition temperature to values where cheap soda lime glass substrates can be used.

A new TFT equivalent circuit was inserted into the "SPICE" simulation programme, from which a 5-level inverter with static TFT could be simulated. Tests of the dynamic behaviour of this programme were performed and good correlation with actual TFT has been found.

Although the project was originally planned to last 5 years, the project stopped after 36 months in May 1988 on a common agreement between the partners, following the decision of CNET to work on a production line in a competitive environment, using some of the first three-year results (two masks process for TFT manufactured with LPCVD-deposited p-Si films).

The goal, previously expected at the end of the project (mid-1990), i.e. driver circuits on soda lime glass able to address a 300 x 300 pixels LCD matrix with a resolution of 4 pixels per millimetre, has obviously been not achieved. But the work forecast during the last two years in this project is now a part of the on-going ESPRIT II project on Active Matrix LCDs (number 2283). It is included in this new project as a specific task to be carried out by the same companies AEG and CETIA.

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CETIA (CSEE)	*F*	*P*

Start Date	**Duration**	**Status**
01-JUN-85	*36 months*	*Finished*

SUBSTRATES FOR CMOS VLSI TECHNOLOGY

JECT NUMBER: 509

The objectives of this project consisted of two parts:

1. To set up an intrinsic gettering (IG) process for wafers with medium high oxygen concentration. The process was to have been independent of the type, p or n, of the substrate and able to produce:

   - a highly defective bulk region

   - a defect-free denuded zone.

     A thickness of this zone around 1-10 micron was identified as an optimum compromise for several factors (such as leakage current and insensitivity to latch up a soft error).

2. To characterise epi wafers diameters of 4 and 6 inches. The thickness of the epilayer was to have been in the range 5-10 micron, both for p+ and n+ substrates. This thickness range is suitable for submicron CMOS. Finally, IG and epi processes were eventually to match in order to have intrinsically-gettered, low leakage epiwafers for submicron CMOS devices insensitive to soft errors.

Problems of supply of EPI-wafers caused delays to the programme of work during the first year. This situation improved in the second year and some of the main targets were achieved at the end of the two year contract. Initial work was carried out on both the correlation between intrinsic defects, processes and device electrical performance and also the area of self-interstitials (injected by oxygen precipitation and by Source-to-Drain ion implantation) as a cause of leakage and lifetime degradation.

The final area of work addressed by the project was the design of the pre-anneal process to match the desired defectiveness/lifetime characteristics.

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IMEC	*B*	*P*

Start Date	**Duration**	**Status**
01-JAN-85	*24 months*	*Finished*

QUANTUM SEMICONDUCTOR DEVICES

PROJECT NUMBER: 514

The recently developed methods of semiconductor crystal growth (MBE, MOCVD) have opened an era of new semiconductor devices which incorporate the principles of quantum mechanics in their design and operation. The objective of this project was to provide new knowledge in this area by investigating new concepts in the promising field of "Quantum Semiconductor Devices" both experimentally and theoretically. The main efforts were devoted to one- and two-dimensional device operations and to perpendicular transport through multilayers.

Some of the results obtained are listed below:

- Two-dimensional electron gas and multi-quantum wells in the GaInP/GaAs.
- The demonstration of the two-dimensional hole gas in GaInAs/InP.
- The room-temperature demonstration of a superlattice tunnel oscillator.
- Demonstration of ballistic motion of hot-electrons injected from graded-gap heterojunctions.
- The highest reported electron density in a planar-doped GaAs structure.
- The first observation of simultaneous electrical and optical bistability in a semiconductor multilayer structure.
- The first observation of the Quantum Hall effect at the GaInAsP/InP heterojunction.
- The observation of extremely low dark currents in graded parameter superlattices.
- Lasing in the GaInAs/InP system.

The theoretical work in support has achieved the following:

- A theory of high field transport in superlattices for the design of novel structures.
- The theory of graded parameter superlattice structures giving rise to new design rules for photodiodes.
- Detailed bandstructure calculations giving new insights with device implications.
- The simulation of delta doped GaAs structures allowing both electron states and transport.

The project has generated 85 scientific papers and some of the results listed have been fed into other ESPRIT projects (522, 843, 971) on III-V devices.

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Start Date	**Duration**	**Status**
01-FEB-85	*36 months*	*Finished*

DOPANT PROFILING FOR SUBMICRON STRUCTURES

PROJECT NUMBER: 519

The objective is to provide the capabilities necessary for the accurate determination of shallow dopant profiles as used in submicron devices, by the further development of one specific electrical technique, Spreading Resistance measurement.

This involves the improvement and optimisation of the measurement operating conditions, the development and implementation of new software correction algorithms, the simulation and assessment of one- and two-dimensional carrier spilling effects, the preparation of special test structures using ion implantation and Molecular Beam Epitaxy (MBE), and the intercomparison of the results of this technique with other electrical and non-electrical methods, e.g. Secondary Ion Mass Spectrometry (SIMS), Rutherford Back Scattering (RBS), Neutron Activation Analysis (NAA), CV Profiling and Electrochemical CV Profiling (ECV).

Through the experimental and theoretical work effected up to now, useful experience has been gained in the deeper understanding of Spreading Resistance measurements and the profiling of special structures. Work has started and is expected to continue on the transferability of probe conditioning and calibration techniques developed within the project. Further work also remains to be done on the understanding of certain discrepancies that remain between theory and experimental data.

This Type B project provides an optimised Spreading Resistance technique which is required by Type A technology development projects under the ESPRIT programme as well as the European IT industry as a whole. The outputs from this project will be recommendations for hardware modifications, improved measurement procedures, improved software for the data processing, and a good understanding of the fundamental possibilities and limitations of this profiling technique.

One of the original participants, GEC, withdrew from the consortium near the end of the fourth year. Two new partners joined in at that time: GeMeTec (D) and Semiconductor Assessment Services Ltd. (UK). The latter is exploiting many of the results obtained within the project.

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Start Date	**Duration**	**Status**
15-FEB-85	*60 months*	*Running*

COMPOUND SEMICONDUCTOR MATERIALS AND INTEGRATED CIRCUITS - II

PROJECT NUMBER: 522

The general objective of the project was to develop advanced aspects of GaAs digital integrated circuit process technology and associated expertise to enable the fabrication of fast, high performance digital circuits. Demonstrator digital ICs have been developed to evaluate the performance of the various logic circuit technologies.

There were some good results at the technological level:

- assessment of refractory metal gate MESFET process
- in-depth evaluation of electron resist
- demonstration of transistor effect in GaInAs-InP structures
- comparison between numeric model and experience for short gate MESFET and HEMT.

However, the major milestones on demonstrator circuits were missed and the overall objective of the project was not reached. Consequently the project was discontinued, but some effort has been made by the partners to achieve the missing milestones on their own resources.

Some of the successful tasks have been used to complement project 232, leading to the launching of project 843.

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FARRAN TECHNOLOGY	*IRL*	*P*
TELEFUNKEN ELECTRONIC	*D*	*P*

Start Date	**Duration**	**Status**
01-JAN-85	*12 months*	*Finished*

INVESTIGATION OF ALL ASPECTS OF THE INTERCONNECTION OF HIGH PINCOUNT ICS

PROJECT NUMBER: 544

The objectives were:

- The development of alternative methods of connecting the integrated circuit to its interconnection medium. This is seen to be particularly appropriate for devices fabricated according to the end-user's design with high pincount.

- The development of large area (30 x 30 cm) high density (250/125 micron pitch) interconnect using multilayer polymer techniques (since polymers are very low in cost and layers can be superimposed quite easily).

- The development of medium area (17.5 x 12.5 cm) ultra high density (50/25 micron pitch) interconnect based on a combination of thick film dielectrics and additive base metal electroplating methods.

The goal was to realise all interconnect systems with just two signal layers, thereby achieving low cost through reduced handling and inexpensive materials. The project was completed at the end of 1987.

The deposition of copper on silicon has been studied. The aim was to deposit high conductivity copper tracks on the passivation layer of an IC. Ten microns wide and 3 microns high copper tracking with a conductivity close to bulk copper has been realised on the passivation of silicon ICs.

A system using screen-printed polymer thick film material has given good results at 250 micron resolution in structures of at least two layers. It was found that the benefits of such a system lie not so much in high track density but rather in the realisation of a large area medium density interconnection on an organic substrate which cannot withstand high processing temperatures. For that reason the original target of 125 micron pitch was not further pursued.

The process for producing ultra high density interconnection patterns on aluminia substrates using a combination of copper plating technology and laser drilled vias in thick film dielectric has been established, with good results (25 micron pitch) achieved. This combines the advantages in reliability and thermal performance of thick film with the conductivity and line definition obtainable from electroplated copper. The process already developed yields tracking down to 25 microns in width with thickness up to 25 microns over areas up to 50 mm square. The limitation on size comes from undercutting during chemical etching. The reactive ion etcher purchased by British Aerospace at the end of the project showed, however, better results should a larger area of extreme density ever be required by a practical application.

The copper tracking has application for the distribution of power in VLSI and wafer-scale circuits where the areas and current requirements may impede the use on conventional metallisations.

A new small dedicated processing equipment line based on thick dielectric films was set up by BAe. The low cost multilayer polymer techniques, which are of prime interest for the industrial printed circuit board manufacturer, have been introduced since 1988 by Lucas Stability Electronics for the realisation of their current products. In addition, NMRC is applying the results of the first objective in WSI applications (Project 824).

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Start Date	**Duration**	**Status**
01-AUG-84	*36 months*	*Finished*

SUBMICRON CMOS TECHNOLOGY (SPECTRE)

PROJECT NUMBER: 554

The objective is to develop the necessary building blocks for a 0.7 micron CMOS process, primarily dedicated to the production of high speed (within the limitations imposed by MOS) digital circuits. In order to allow the programme to proceed with the best chances of success, two main phases have been identified and organised: the first refers to an intermediate step at the 1 micron level; the second to the final 0.7 micron CMOS family. Two additional tasks were added to the original project at the end of the first year making eight tasks now identified to meet the final goal of the project. These address the topics of architecture (T1), optical and electron-beam lithography (T2, T3), MOS Structures (T4), Isolation (T5), Interconnect (T6, T7) and refractory metal gates (T8). It is the responsibility of Task 1 to arrange the pilot-line demonstration of the 1 micron and submicron demonstrators. Tasks 2 to 8 provide the technology inputs for this.

By the end of year three, the demonstrator of the 1 micron CMOS process had been fabricated by CNET. The process is an N-well CMOS process, with polycide gates and two metal levels. The first metal level is formed by CVD Tungsten. Isolation is based on an optimised LOCOS technique, while LDD with deposited oxide spacers has been used to increase the reliability of N-channel devices.

The demonstrator device is a multichip including:

- a 4K, 6-transistor SRAM by CNET
- a 4K, 6-transistor SRAM by IMEC
- an image processor by BT (obtained from the Wafer Scale Integration project)
- modules for the extraction of electrical parameters, including the common test developed for electromigration studies.

In parallel, a 64K, 6-transistor SRAM designed by MHS, whose size of 27 mm^2 prevented it from being included the multichip, was processed in the same line, making use of the same process.

The access time of the 4K SRAM from CNET was 20 ns, limited by design, while the 64K SRAM by MHS showed parts with access time lower than 15 ns and a stand-by current absorption of 10 uA. A logic circuit (70 000 transistors, 35 mm^2, 54 MHz) has subsequently been realised by CNET in the 1 micron process issued by SPECTRE.

Several technologies have also been developed but not been included in the 1 micron demonstrator. This is the case of E-beam lithography, which after a

three years development has been dropped, due to the appearance on the market of I-line steppers and of G-line lenses with good submicron performances. Amongst other development technologies, three could be included as achievements of the first phase:

- Trench isolation: this technology has been developed and demonstrated, and found to be compatible with 5 V power supply. However, since comparable results could be obtained with a more conventional approach the trench will not be used in the final demonstration.

- Metal Gate Transistor: the program has been pursued up to the processing of a 16K SRAM memory. Nevertheless, due to the lack of availability of the equipment, the programme has been stopped.

- Two Aluminium Layers: test devices have given good results down to pitches of 2.8 micron and 3.6 micron for the first and the second metal.

During year four, the partners have agreed upon a submicron "core" process flow, that is, a common skeleton to which different technologies could be grafted and a common set of design rules was developed. To investigate the possible evolution toward a 0.5 micron process, special "advanced" rules were developed, to be used by one of the research laboratories. The investigation of the problems connected with the implementation of these rules will open the way to the definition of the technologies needed for the 0.5 micron process.

At the end of December 1987, the one micron CMOS process results were disseminated throughout eleven companies and research laboratories located in five European countries.

Additionally, Matra Harris successfully transferred the SPECTRE CMOS technology into its fast static RAMs and microprocessor fabrication lines and selected process steps are being integrated in the fabrication process of a 1 MEGA EPROM by STM.

The above are indications of the uses to be made of the technological results which will be exploited as a result of this project. The objectives are in line with the world-wide state-of-the-art expectations for high density ICs.

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BULL S.A.	*F*	*P*
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MATRA HARRIS SEMICONDUCT.	*F*	*P*
SGS MICROELETTRONICA SpA	*I*	*P*
UCL	*B*	*P*
HARWELL LABORATORY	*UK*	*P*
TELETTRA SPA	*I*	*P*

Start Date	**Duration**	**Status**
31-DEC-84	*60 months*	*Running*

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HIGH RESOLUTION PLASMA ETCHING IN SEMICONDUCTOR TECHNOLOGY: FUNDAMENTALS, PROCESSING AND EQUIPMENT

PROJECT NUMBER: 574

It is widely recognised within the electronics industry that plasma etching will play a vital role in achieving submicron technology both in silicon and III-V semiconductor systems.

The objective of this project was to gain a better understanding of the complex chemistry and physics involved in plasma etching by applying suitable diagnostics methods.

The knowledge gained could then be applied to the manufacturing of improved equipment and process realisation.

The first part of the work was devoted to the development of measurement instrumentation and equipment setup. In particular, an optical emission spectrometer and a quadrupole mass spectrometer were installed in a reaction chamber in order to detect the chemical species created when the etching reaction takes place. A reactive ion etching process was successfully established for a 0.5 micron structure size.

The study of the reaction kinetics paves the way for an improved etching process to be designed which can be utilised as a term of reference by other industries because of the widespread research work. Already as a result of this project an advanced three-chamber plasma etching machine has been produced by one of the partners. This equipment is capable of processing 200 mm wafers with ICs designed with 0.5 micron structure size. A prototype was shown at the Produktronika 87 Fair in Munich and commercialisation is expected. However, additional and up-to-date etching processes are still needed for full exploitation of the machine's capabilities.

The new optical spectrum analyser (including software) developed by Monolight is due for commercialisation in 1989.

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MONOLIGHT INSTRUMENTS LTD.	*UK*	*P*

Start Date	Duration	Status
01-JAN-85	*48 months*	*Finished*

CAD FOR VLSI SYSTEMS (CVS)

PROJECT NUMBER: 802

The objective is to implement an integrated CAD system capable of coping with the needs of the 1990s, where improvements in semiconductor technology will allow the production of chips with about 1 million transistors. Such a CAD system must lead to a factor of 10 improvement in design time, based on novel tools for automatic construction of designs at the level of system architecture by interconnecting cells representing parts of the total system which have themselves been constructed automatically from a set of given parameters.

The areas of work include therefore, architecture synthesis, digital cell building, analogue cell design, integration of tools and design of demonstration chips. The first prototypes of tools will be delivered by the end of 1989.

During the first 30 months of the project the design and first implementation of the tools were completed. In order to demonstrate the effectiveness of the tools developed in the project, an ambitious demonstrator chip has been selected. This is an advanced signal processing VLSI forming part of a new mobile telephone receiver. The overall system design of this chip has now been completed, and the implementation using the CVS system will take place during the next year.

Such a CAD system is expected to lead to a factor of 10 improvement in design time. For chips which will not be sold in very large numbers, rapid and accurate design is of the utmost importance. The techniques of automatic construction of the designs, both at the architectural level and for analogue cell design, should be important elements in achieving this aim.

In order to have maximum impact on industry in general, in addition to internal use by the partners, it was agreed that the resulting software will be made available to third parties (e.g. software houses) for the marketing of the results. One company (ANACAD) in Germany has already taken steps to bring some of the results to the market place.

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CNET CNS	*F*	*P*
GMD	*D*	*P*
ITALTEL	*I*	*P*
MATRA HARRIS SEMICONDUCT.	*F*	*P*
SGS MICROELETTRONICA SpA	*I*	*P*

Start Date	Duration	Status
01-MAR-86	*54 months*	*Running*

WAFER-SCALE INTEGRATION

PROJECT NUMBER: 824

The objective is to use the Wafer-Scale Integration (WSI) approach to build systems of up to 25 million transistors on a 4-inch wafer using a hierarchical approach to implement tolerance to end-of-manufacturing defects. Progress will materialise in three demonstrators:

- A 4.5 Mbit Static Ram

  The main goal of the 4.5 Mbit RAM memory (access time 100 ns) is to check the possibility of efficiently using switches in order to discard faulty elements and replace them with spares. Starting from cells of 64 Kword of 1 bit, the final interconnection network to be produced on a 4" wafer will implement 18 blocks of 256K x 1 bit.

- A WSI Systolic Array

  Systolic arrays are well suited to WSI because all communications are between nearest neighbours. The approach is to define a general purpose architecture that is likely to cope with many application problems notably in processing video images, display graphics and advanced memory devices. The chosen architecture is a 128 x 128 array of processing elements.

- A 16-bit Microprocessor

  The long-term goal is to integrate a fully dedicated system on a single chip using pre-defined blocks embedded in a flexible interconnection structure (a sea of gates, for instance). Being the master block of the system and one of the biggest ones, the microprocessor has to be particularly adapted to the application, but its architecture must also be compatible with fault tolerance. The project is to develop a library of pre-defined and parameterised elements as well as design tools to produce the layout of a 16-bit reconfigurable microprocessor. Such an approach is needed in order to guarantee short design times together with adaptation to the application constraints in both terms of functionality and speed.

During the first year, the first silicon (WSI test mask) on Wafer Scale Integration was processed successfully. Switches to reconfigure a wafer were dispatched to every partner; either to blow the fuse, or to correct with Laser Lithography and lift-off, or to charge and discharge floating gate FETs. The first results on the characterisation of these switches are in agreement with the target.

Blocks for building the Wafer-Scale demonstrators have been designed and processed during the second year:

- 16 + 1 spare bits application-specific microprocessor (building block for a "big chip" with microprocessor, memory, peripherals, etc)
- 2 x 2 and 8 x 8 systolic arrays (building blocks for a Wafer Scale systolic array)
- extra hardware necessary to interconnect on wafer 72 static RAM of 64 Kword x 1 bit, in order to achieve a 4.5 Mbits SRAM.

Additionally, two WSI architectures, for a memory and a systolic array, have been proposed with solutions to the difficult problem of reconfiguration and testability. The first silicon demonstrating WSI implementation is foreseen early in 1989.

The developed know-how in technology will allow correction of end-of-manufacturing defects and hence improve the ability to realise full custom, one million transistor chips for the ASIC sector.

From the system point of view, the developed systolic array, as it is more compact and can contain more processors than any other available system, is opening up a whole new range of uses, notably for signal processing functions in video applications.

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DARMSTADT TECH. HOCHSCHULE	*D*	*P*
INPG	*F*	*P*
LETI	*F*	*P*
NAT. MICROEL. RESEARCH CENTRE	*IRL*	*P*

Start Date	**Duration**	**Status**
15-MAI-86	*48 months*	*Running*

PACKAGES FOR HIGH-SPEED DIGITAL GAAS INTEGRATED CIRCUITS

PROJECT NUMBER: 830

The various package design requirements being evolved to meet the requirements of the GaAs IC industry were to be investigated. The objective was the establishment of package standards, together with clearly defined design principles and methods of fabrication.

The project goal was to develop 8, 16, 24 and 40 I/0 lead packages having the necessary operational characteristics for mounting and hermetically encapsulating GaAs ICs for use in high speed digital applications. Extensive use was intended to be made of sophisticated computer-aided design and simulation modelling, the success of which had been already been established in the case of the 8 I/0 lead package.

Three technical approaches to package construction were investigated: the use of direct-sealing techniques, glass joining fired ceramic, and co-firing glass-ceramic. Associated topics included materials, metallisation and heat dissipation.

This project was complementary to project 958 as part of the "Advanced Packaging" workprogramme.

During the first year, the direct sealing method of package fabrication, originally used at Thomson, has been established at EEV. Valve samples of 8 I/O and 16 I/O (original design) fabricated under the fired glass joining structure have been supplied to Thomson for qualification, and prototype structures of green glass ceramic have emerged.

Within the second year, the redesign of 8 and 16 I/O packages has been performed. However, at that time, the analysis of the industrial partners has shown that the prospects of developing a viable business in competition with other sources had seriously diminished and consequently it has been decided to discontinue the project.

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Start Date	**Duration**	**Status**
31-JAN-86	*24 months*	*Finished*

LARGE-AREA COMPLEX LCDS ADDRESSED BY THIN-FILM SILICON TRANSISTORS

PROJECT NUMBER: 833

The project was completed in May 1987.

Liquid Crystal Displays (LCDs) have emerged to become the dominant flat panel display technology in recent times. Their low power and voltage requirements are advantageous, not only for portability, but also because they lead to unstressed highly reliable electronics which, when combined with the lack of inherent failure modes in LCDs, yield very thin lightweight displays with service lives orders of magnitude longer than Cathode Ray Tubes (CRTs). Thin-film transistor addressing of LCDs allows an increase in display size and complexity to levels adequate for word processor and graphics displays.

The aim of this project was to investigate a viable technology for the fabrication of large area (A5 to A4) and complex (up to 1000 addressable lines) LCDs based on polycrystalline and amorphous silicon transistor active matrices. Silicon Thin Film Transistors (TFTs) showed higher yield and reliability than other TFT materials.

Extensive investigation of the following areas was made:

- optimisation of transistor characteristics, yield and stability over large areas
- special high throughput, large area semiconductor processing equipment
- special LCD fabrication techniques
- colour systems
- interactive displays
- human factors.

A breakthrough in the technology of polysilicon TFTs on glass allowed GEC to achieve, in a reproducible manner, and in small-geometry (10 x 10 micron) devices, on-off ratios in excess of 105, mobilities of 10 cm^2/Vs and threshold voltages as low as 8 V. A new active matrix circuit was patented which entirely eliminates line failures and this increases the yield enormously. These breakthroughs were verified on test displays 6 x 4 cm in size with 96 x 64 pixels, which were fabricated with less than 10 defects. In the amorphous Silicon (a-Si) area, in addition to the CNET proprietary technology, Thomson-CSF developed an alternative potentially high-yield process based on small-geometry (10 x 20 micron) high-mobility (0.4-0.7 cm^2/Vs) TFTs and demonstrated almost defect free 6 x 8 cm displays with 256 x 320 pixels.

CNET demonstrated an 8 x 8 cm colour display with 320 x 320 pixels based on a new RGB colour filter technology. A system based on capacitive interaction with resolution of 0.4 mm was realised. AEG achieved very low pinhole density (1 per cm^2) sputtered silicon dioxide. Modulex developed drive circuitry interconnections using high throughput tape automated bonding of chips on to flexible p.c. board. Significant achievements were also made in the areas of plasma silicon nitride and large area display photo-lithography.

Following the end of the planned work schedule, a number of prototype displays were demonstrated at the ESPRIT conference in September 1987. A major follow-up project, which exploits the results achieved in these studies, is now going on ESPRIT II (project number 2283).

Some recent surveys have underlined the importance of new display technologies because of their potential for eventually replacing CRTs as the principal visual display medium for a range of informatics based products. The progress on topics listed above places the collaborators in a strong position, even with respect to the Japanese competition, particularly because of the availability of both polysilicon and amorphous silicon technologies.

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THOMSON CSF/LCR	*F*	*P*
CNET LANNION	*F*	*P*

Start Date	**Duration**	**Status**
10-DEC-85	*18 months*	*Finished*

COMPOUND SEMICONDUCTOR INTEGRATED CIRCUITS

PROJECT NUMBER: 843

This project involved six major European companies from three countries. The objective was to develop advanced GaAs integrated circuit technologies leading to the fabrication of high performance integrated circuits addressing key memory and fast signal processing functions. The availability of state-of-the-art GaAs-ICs will serve European system and equipment manufacturers in the IT and telecoms industry and help to provide them with the necessary worldwide competitive edge.

The programme could be broadly divided into high complexity ICs using enhancement/depletion mode MESFET logic (STC, LEP, and Siemens), and high speed ICs using depletion mode based MESFETs and HEMTs (Thomson, Plessey and GEC). GaAs heterojunction bipolar transistors (HBT) were also included in the latter part of the project to complement the MESFET and HEMT technologies.

MESFET, HEMT and HBT technologies are in different stages of maturity, but many key technologies are shared, such as ion implantation, advanced lithography (E-beam, deep UV and DSW), dry processing, self-alignment techniques and testing tools. These technologies have been investigated in parallel, from device modeling to manufacturing capability.

During this programme, key demonstrators of increasing complexity have been produced and some of those achieved state-of-the-art performances: low power consumption (220 mW) GaAs 1K SRAM with access time in the range of 1.4 ns, 4-stage serial multiplier using self-aligned technology which can be clocked at over 800 MHz equivalent to 1.25ns/bit multiplication time, 4:1 divider reaching 9.7 GHz clocking speed, and finally 4-bit ADC capable of 1 G sample/s with on-chip sample and hold and error correction functions, with performance equivalent to the best 0.6 micron Si ECL technology.

The technology developed under this project is exploited in different ways by each company in the consortium. Some have transferred it into their pilot lines to improve their commercial products or to add new products to their catalogue. Others have applied the technology in broader areas of III-V semiconductors such as optoelectronic integrated circuits, and have helped to accelerate their research activities.

Finally, this project had led to over 40 publications in international conferences and technical journals.

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LAB DE PHYSIQUE APPLIQUEE	*F*	*P*
PLESSEY RESEARCH LTD	*UK*	*P*
SIEMENS A.G.	*D*	*P*

Start Date	**Duration**	**Status**
01-JAN-86	*36 months*	*Finished*

EUROPEAN CAD INTEGRATION PROJECT (ECIP)

PROJECT NUMBER: 887/2072

ECIP investigates the area of data exchange and infrastructure standards with the objective of defining and promoting standards within the European IT industry. The ability to readily interchange data and CAD tools between companies is a key area for bringing into practical reality many of the benefits of collaborative tool development in Europe and for making available the results of ESPRIT to the wider European IT community. The final goal of ECIP is the definition of a multilayered open model for CAD systems with recommendations for rules and/or standards at each level.

Effective liaison between the ECIP project and all other ESPRIT CAD projects has been established ensuring transfer of experience in both directions. In this way it will be ensured that the standards developed in ECIP are based on a wide experience of requirements and should therefore be widely acceptable to developers of present and future CAD systems.

Following an analysis of the requirements and needs of the existing CAD systems of the partners, with particular reference to standard interfaces, together with a corresponding investigation of existing standards in the field of CAD for VLSI, the partners presented a summary of their preliminary recommendations at the first and second ECIP Seminars during the ESPRIT Conferences in 1987 and 1988.

Although the partners represent a reasonable cross-section of the relevant European industry, importance has been attached to broadening the peripheral involvement to include other interests which cannot be directly represented. To this end, liaison has been established and joint meetings held with the other existing ESPRIT CAD projects. Representatives from many of these projects attended the ECIP Seminars.

This project is central to the strategy of optimising the results of past, present and future work in the CAD area. It will define standard interfaces which will allow tools from different projects to be interconnected and design data to be shared between a range of design systems and silicon manufacturers. In order to ensure the acceptance of such proposed standards by the appropriate industries, the results will be made widely available and potential users will be encouraged to comment on interim results.

Following a successful proposal in 1988, a new ECIP project (2072) with some new partners and broader terms of reference was started. In addition to amplifying the work started in ECIP1, ECIP2 will add the important standardisation of high level description languages, and of providing objective ways of measuring the performances of CAD modules. The work on CAD frameworks, started in ECIP1, will be greatly expanded covering user interfaces, database interfaces and data interchange interfaces. In all cases, tools to implement and check the

recommended standards will be provided and these recommendations will be validated in real design environments.

The direct involvement of six major European microelectronics companies and the indirect involvement of many other projects will provide the basis to ensure the successful adoption of the standards on a wide scale. Some impact (adoption of interim recommendations) can be expected during the project but the main impact will be on later generations of CAD systems 5 years from now.

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NIXDORF	*D*	*P (2072 only)*
SGS THOMSON MICROELECT. SPA	*I*	*P*
SIEMENS A.G.	*D*	*P*
THOMSON CSF/SCTF	*F*	*P (2072 only)*

Start Date of ECIP1	**Duration**	**Status**
01-JAN-86	*36 months*	*Finished*

Start Date of ECIP2	**Duration**	**Status**
01-JAN-89	*60 months*	*Running*

ADVANCED INTEGRATED-CIRCUIT DESIGN AIDS (AIDA)

PROJECT NUMBER: 888

The objective of the AIDA project is to master the complexity of VLSI chips (more than one million transistors within the next few years) by obtaining a drastic improvement in design methods. CAD tools, new methods and concepts will be defined, proved on experimental software and finally developed into industrial tools integrated into the existing CAD environments of the partners. AIDA explores the application of modern programming techniques and knowledge-base engineering to CAD tool development. It will constitute a design assistant that proposes solutions rather than merely records and validates the designer's ideas. This will allow the designer to apply his creativity where it is most efficient, leading to improved design quality. Modern programming techniques will be applied (e.g. those developed for expert systems to VLSI-CAD tools). The potential contribution of these techniques is twofold:

- The basic techniques may be used to make new tools much more efficient than classical ones.

- The basic integrated circuit design knowledge may be recorded into the machine, and used by "expert" modules, under the control of a system designer.

The following 7 work packages show the full span of problems tackled by the project: Data Management, Specification, Synthesis, Layout, Testing, Man-Machine Interface and Evaluation.

The project started with an in-depth study and refinement of the requirements catalogues in each work area and the establishment of priorities in the different approaches towards implementation. In data management, particularly, the large volume and complex structure of the design data, together with the extensive range of necessary design tools and all their varied interactions, means that the requirements of CAD systems for VLSI design are probably among the most challenging of all database applications. Here the partners have concentrated on aspects of portability, exchange formats and interfaces and data security concepts, especially for CAD systems distributed over a range of interconnected computers.

During its second year the project entered the implementation phase. During the third year most of the first prototype tools have been produced. Many of these were demonstrated at the exhibition during the ESPRIT 1988 Conference.

The final year of the project, which is now underway, sees the completion of the implementation and integration of the tools.

Prompted by the need to share design data and tools between the three corporate databases, the project evolved an internal standard for the presentation

of conceptual data models. This development has been taken into account in the work on conceptual models in the ECIP project. The last year of the project contains work to implement the software bridges between the three CAD systems.

All three partners have a large existing investment in CAD systems in-house. The project will have a significant impact on the ability of these companies to design complex chips of several million transistors. Furthermore, the partners are committed to marketing the results both as stand-alone tools and as integrated systems, thus making the results available to a much wider community. AIDA should also prove a useful test-bed for the proposed standards emerging from the ECIP Project (number 887).

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Start Date	**Duration**	**Status**
15-NOV-85	*48 months*	*Running*

BASIC TECHNOLOGIES FOR GAINAS MISFETS

PROJECT NUMBER: 927

Solid solution of InGaAs epitaxially grown on semi-insulating InP substrates is promising for high speed logic devices as well as for integrated opto-electronic circuits for 1300-1500 nm wavelengths. The objective of this project was the fabrication of insulated gate field-effect transistors (MISFETs) on GaInAs.

There were three main tasks:

- To evaluate the influence of the InP substrate quality on the overlying devices and to improve accordingly its quality.
- To obtain a better understanding of the basic phenomena at the interface between the insulator and the InGaAs.
- To explore the possibilities of ion implantation, compared to MOCVD epitaxy for implementing active devices in this ternary compound.

Full scale equipments for InP synthesis and for crystal pulling under magnetic field have been installed and tested. Large semi-insulating InP crystals (up to 3" in diameter) weighting more than 4 kg have been successfully grown with low dislocation density (around 10^3 EPD.cm^{-2}).

Good progress has been achieved in growth uniformity on 50 mm wafers by MOCVD (thickness <3%, composition <2% , doping level <5%).

Various technological processes for high speed logic devices and integrated optoelectronics have been optimised. Typical transconductance for E and D-mode MISFET obtained is 300 ms/mm and 140 ms/mm respectively, while complete stability of the drift of drain current is observed when Si_3N_4 is used as insulator.

Besides the strengthening of European supply of InP wafers for integrated optoelectronics, this project investigated new active devices in the III-V family based on InP. This is of the utmost interest for the development of low cost optical communication systems.

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WACKER CHEMITRONIC	*D*	*P*

Start Date	**Duration**	**Status**
01-JAN-86	*36 months*	*Finished*

HIGH-DENSITY MASS STORAGE MEMORIES FOR KNOWLEDGE AND INFORMATION STORAGE

PROJECT NUMBER: 957

This project was completed in January 1989.

The objective was to develop vertical and magneto-optical recording technologies for mass storage on rotating discs. Compared with classical recording techniques, these technologies are potentially capable of providing much higher storage densities, as well as higher storage reliability and more competitive storage costs.

Vertical recording technology was investigated and developed for both floppy and rigid discs. Addressed topics include media and substrates and read/write heads. A new optical pick-up was designed for magneto-optical recording. In addition to the development of basic components and technologies, work was carried out for simulation of the mechanical dynamics of the flying heads.

The specific technical objectives achieved in the case of vertical recording were a linear density of 40 000 fci and a radial density of 1500 tpi for rigid discs. The magneto-optical system should provide a linear density of 20 000 bpi and a radial density of 10 000 tpi. In terms of the capacities, these results for 5.25 inch drives correspond to 150 to 200 MB for vertical rigid discs, and 400 to 500 MB for magneto-optical discs. The project was divided into four tasks:

Floppy Discs:

Problems linked to CrCo tribology at high linear densities in perpendicular recording were encountered, and could not be satisfactorily solved from an industrial point of view. Even with a carbon upper layer the head-media interface still poses major problems which induce a lifetime far below the expected values. So, studies on BaFe were emphasised during the last year, both on material preparation and on coating technologies. Powders made by BASF make it possible to achieve media characteristics at the best worldwide level and will lead to commercial products as soon as the market is developed.

Rigid Discs:

Optimisation of composition for the media was reached. A new sublayer was developed and the intermediate layer was studied. Glass substrates showed excellent mechanical and structural characteristics. Recording with a linear density up to 40 KFCI was successfully done with magnetic heads which are available in the market place. Improvements are still needed on the studied thin film heads to increase the recording density on these discs from 20 to 40 FCI.

The optimisation of the RF sputtering deposition conditions for CrCo films also led to the realisation of layers adapted to magneto printers.

Magneto-Optical Media and Heads:

Work was carried out on media (garnets and amorphous Rare Earth Transition Metal (RETM) alloys) and pick-up systems.

Amorphous RETM alloys films were shown to have suitable properties as storage media but to exhibit aging when the media are stored in a wet atmosphere. Optimum deposition conditions (especially Argon pressure) improve the ageing of the layer through a control of its microstructure.

Thin garnet films are thought to be possible competitors to RETM alloys especially if they can be deposited by sputtering. Moreover, the combination of a magneto-optical garnet film for read out and of a ferrite film for the storage of the information looks very promising. Garnet films obtained by facing target sputtering need to be improved by focussing on the sputtering conditions.

Optical components for a pick-up system based on a new original concept were developed and tested. A complete mock-up was built with the integrated read-out and write functions, and tested with respect to noise sources and defects.

Simulation:

Specification of the head interface was completed, and software tools for testing different coding schemes were developed.

The three major objectives of this project (vertical magnetic recording for achieving extremely high storage densities, reversible optical recording, and the magneto-optical technology to achieve extremely high surface densities) are currently considered worldwide as strategic targets, and hence their achievement put the partners in a strong competitive position.

Some of the results pave the way to industrial products in the near future (such as BaFe floppy discs). The other results, especially on magneto-optical discs and heads, give the partners a strong background to be used in the ESPRIT II project (number 2 013) on magneto-optical disc drives.

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Start Date	**Duration**	**Status**
01-FEB-86	*36 months*	*Finished*

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HIGH-PERFORMANCE VLSI PACKAGING FOR COMPLEX ELECTRONIC SYSTEMS

PROJECT NUMBER: 958

The objective was to exploit the potential advantages of high density structures on which VLSI chips will be connected with very dense (100 to 125 micron pitch) TAB (Tape Automated Bonding) interconnects on a high performance multichip substrate.

This project was complementary to project number 830 as part of the "Advanced Packaging" workprogramme.

Two TAB technologies have been developed: bumped chip TAB and bumped tape TAB (BTAB). Bumped chip requires additional wafer processing, bumped tape requires an additional photolithography stage for the tape.

Manufacturing processes have been adjusted to reach the level of fully controlled product at 125 micron pitch. At 100 micron, good results have been achieved but at laboratory level.

The high density substrate development has been concentrated on the fabrication of multilayer structures with track pitches as small as 125 micron in order to enable the pitches on the chips and on the substrate to be identical and hence to maximise the interconnection density. Under these conditions, the via-hole diameters needed to be 50 micron or less. This was beyond the limits of mechanical drilling, so laser drilling techniques have been developed.

Liquid immersion in fluorocarbon has been chosen to extract heat from the rear surface of the chips. Thermal trials have corroborated the thermal modelling work which indicated that power densities up to more than 20 W/cm2 can be effectively dealt with by this means.

In order to bring together the various developments in the hardware and design techniques, two demonstrators have been realised. The first is an array of 36 ICs, each 100 mm^2 with 284 I/Os on 125 micron pitch, mounted by TAB onto a multilayer substrate of 100 cm^2 having tracks at 125 micron pitch and 50 micron laser-drilled via-holes. The ratio of silicon area to substrate area is extremely high (36%).

The second demonstrator incorporates a high speed multiplexer circuit, using ECL ICs designed and made by British Telecom with TAB pitches of 162 and 200 micron. There are also ten of the same chips (125 micron pitch) as on the first demonstrator which will enable testing under conditions of high total power dissipation. Additional surface-mounted resistors and capacitors are reflow-soldered onto both sides of the substrate. The multiplexer circuit has been connected to a de-multiplexer built in conventional technology and compared to a conventionally built multiplexer. Electrical and thermal

performance measurements have shown that such a structure, can be used as a basic building-block of a very high performance system (1 GHz clock or 20-50 ns system cycle time).

The main application areas for the TAB technology within the telecommunication and industrial segments are for high-speed switches and processors, display drivers and high-speed transmission systems.

TAB offers a packaging technique allowing the assembly of VLSI chips in compact modules, where electrical signals are closely monitored and heat can be efficiently evacuated.

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Start Date	**Duration**	**Status**
31-JAN-86	*36 months*	*Finished*

THREE-DIMENSIONAL ALGORITHMS FOR ROBUST AND EFFICIENT SEMICONDUCTOR SIMULATOR (EVEREST)

PROJECT NUMBER: 962

The numerical analysis and prediction of the detailed behaviour of semiconductor devices is an important step in the development of a new process. With the advent of sub-micron feature sizes, this analysis is becoming increasingly difficult. For certain calculations one-dimensional or two-dimensional analysis is no longer sufficiently accurate. Three-dimensional analysis is only just becoming available inside certain major industries and is prohibitively expensive in computing time.

The goal of this project is to develop, for 3-D devices, a set of fully tested algorithms, initially for steady-state analysis and later for transient and small signal loading conditions. The interaction with the temperature of the crystal lattice will also be taken into account. Success in this aim implies crossing new research frontiers in non-linear numerical analysis techniques both to solve the problem reliably and within reasonable computing costs. As part of the drive to reduce computing costs, the applicability of computers with advanced architectures will be investigated. Following validation against measurements of real devices, the successful algorithms will be incorporated into computer systems in the industrial partners and in a common project research code.

On the basis of the first year's work, a reappraisal of priorities led to an effort to augment the work package which will produce the project research code. The definition of the plan for this work package has been greatly strengthened. This work culminated in delivery of the first release of the code for the solution of the initial target of the off-state 3-D problem which was demonstrated at the project review in December 1987, with further enhancements shown in 1988. The validity of the results will be demonstrated using an agreed set of benchmarks in 1989.

Fully transient 3-D analysis at a reasonable computing cost is an ambitious goal. Even 2-D solutions of this problem are only to be found inside large semiconductor companies (predominantly US and Japanese) at this time, and it has been claimed that even these programs cannot solve all of the device problems in this category. The availability of such an analysis tool in Europe by 1990 would put Europe in a strongly competitive situation. In addition to the industrial use of the results by the companies in the project, the research project code will be available to other European research organisations for research purposes. The possibility of eventual commercial exploitation of the research code is also being examined.

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Start Date	**Duration**	**Status**
10-APR-86	*48 months*	*Running*

TECHNOLOGY FOR GAAS-GAALAS BIPOLAR ICS

PROJECT NUMBER: 971

The general objective was to develop a high performance GaAs process using GaAs-GaAlAs HBTs for ultrafast emitter coupled logic. E-beam lithography, plasma deposition and etching techniques have been investigated together with all aspects of the IC process including material epitaxy (both MBE and MOCVD), ion implantation, rapid thermal annealing, lithography, dry etching, ohmic contacts (including refractory alloys) and dielectrics. This work was accompanied by a strong effort on modelling, concerning both 1-D and 2-D device numerical modelling and analytical CAD block models.

This two-year program was thus dedicated to the development of a basic process validated on HBTs and SSI divider (D/2 and D/4) ECL circuits and to the investigation of the specific steps of a future advanced self-aligned process.

The most significant achievements obtained during the project are a high degree of quality and uniformity of both MBE and MOCVD layers, world record values for p-type base doping, assembling, validation and comparison of three basic technological processes using ion implantation, rapid thermal annealing (RTA), dry etching and high performance n-type and p-type ohmic contacts (including the non-conventional InGeAu and AuMn alloys). Also, several approaches leading to self-alignment and micron and submicron rules have been investigated with already a very exciting successful fabrication of exploratory self-aligned HBTs. On the other hand, all three basic processes have been characterised on HBTs with cut-off frequencies above 20 GHz and up to 29 GHz, and division by two and by four circuits has been demonstrated with input rates as high as 7.6 Gbits/s.

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Start Date	**Duration**	**Status**
01-FEB-86	*24 months*	*Finished*

OPTICAL INTERCONNECT FOR VLSI AND HIGH BIT-RATE ICS

PROJECT NUMBER: 986

The inherent wide bandwidth and crosstalk immunity of optical transmission media permits very high bit rate signals to be distributed, overcoming the transmission line and r.f. interference problems encountered with very high bit rate ICs. Many lower bit-rate signals, each of which would conventionally employ a package pin, can be time multiplexed together to form one easily transmitted, high bit rate optical signal which leaves the package via one optical pin, thus avoiding very high pin counts for VLSI chips. Many processor architectures require a high density of long range interconnections which, when implemented conventionally, can cause major interference, signal degradation and space consumption problems when integration into compact systems or increased bit rates are required. Optical interconnection offers a way of overcoming these problems.

The objective of Project 986 was to demonstrate the potential advantages of optical interconnection technologies for high bit rate signals in electronic assemblies such as circuit boards and other asssemblies of an equivalent integration level, and to examine some of the technological and practical aspects of implementing optical interconnection.

The project was divided into four distinct tasks:

Task A was directed towards the design, construction and evaluation of an optical interconnect demonstrator comprising a significant circuit/processor function and utilising optical connection at data rates lower than 1 Gbit/s. The implementation was based on hybrid circuit technology, assembled on printed circuit boards and employing an optical fibre link designed to transmit data without any format restrictions (i.e. operation down to d.c.).

The main activities have been to design and build high speed optical transmitters and receivers and 16:1 multiplexers and demultiplexers. Appropriate protocols for the signalling circuits have also been selected and interfaces to the processing functions constructed which were predominantly further stages of multiplexing from the processors bit rate. The hybrid multiplexers and demultiplexers have been built and have been evaluated at data rates up to 2 Gbit/s. Testing of the transmitters and receivers up to 1 Gbit/s has also taken place.

These modules were assembled together to form an optical interconnect demonstrator to explore the advantages, disadvantages and limitations of time multiplexed optical interconnect.

Finally testing of the demonstrator has shown error free operation at above 600 Mbit/s although timing tolerances and power budget were critical.

Task B has been directed towards the design and evaluation of short haul optical links operating at up to 5 Gbit/s. The main impetus of this work has been to

examine the limitations on high bit rate optical links designed for operation with unformatted data, and with as simple a receiver as possible since low cost and power consumption are essential if optical links are to play a part in communications between VLSI chips.

The conclusion is that, except for special requirements such as when the basic circuits operate at gigabit rates, OIC bit rates above 2 Gbit/s are not attractive and in many cases it is expected that less than 1 Gbit/s will be more cost effective, depending on multiplexer technology. As a result, work on this task was terminated in June 1987.

Task C was directed towards the development of planar waveguide technology suitable for optical interconnect on printed circuit boards or in hybrid packages, specifically to hybrid technologies in which a printed optical circuit is formed on a substrate and emitters and detectors are coupled directly to the waveguide. A number of waveguide technologies have been assessed:

- polymer waveguides
- screen-printed glass waveguides
- deposited $SiO_2/Si_3N_4/GeO_2$ waveguides
- ion-exchanged waveguides.

The lowest loss obtained was 1 dB/cm on SiO2 guides. Wavelength division multiplexers have been demonstrated using dichroic filters into multimode Y-junctions.

Task D: There have been two main areas of investigation in this task. The first has been concerned with detector and emitter devices and the interfacing of these to waveguides, and the second with the computer architecture implications of optical interconnection.

The requirements for detector and emitter devices, the performances that might be expected from these devices and the integration of them with standard silicon VLSI processing have been considered. On the architectural side, various types of advanced processor systems have been considered. The Single Instruction Multiple Data (SIMD) array processor has been identified as a particular application in which optical interconnect has been assessed.

The overall conclusion of this project is that planar optical interconnect is useful where track lengths exceed - 10 mm, track densities exceed - 10 mm^{-1} and bit rates exceed - 100 Mbit/s; upper limits to these parameters are roughly one order of magnitude higher. At the lower end of the range, at least miniature microstrip offers comparable performance. Whilst fixed interconnect is likely to be the only viable option at chip and board level for a number of years, the data transparency of optical switching makes reconfigurable interconnect a very interesting area for future research.

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Start Date	**Duration**	**Status**
21-DEC-85	*24 months*	*Finished*

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MULTIVIEW VLSI-DESIGN SYSTEM ICD

PROJECT NUMBER: 991

The objective was to develop a complete, integrated, open and cost-effective design system usable from a large variety of intelligent workstations. The system was to be capable of mastering the complexity of the design of large integrated circuits by:

- Exploiting their geometrical and functional hierarchies in a logical and intelligent environment
- providing sophisticated synthesis and verification tools.

The work is an extension of project MR-09-DFT under the Microelectronics Programme 3744/81. The main topics to be covered are: functional data modelling, distributed data management, verification of submicron structures, advanced multilevel simulation as well as self-testing/fault-tolerant synthesis techniques, and the provision of tools for the verification of manufactured ICs.

Finally, the project had the explicit goal of providing an open system geared to the needs of independent designers (although it will be equally useful in a larger design environment). The system will therefore provide foundry interfaces at the various design and test levels. It will be capable of running on intelligent, but inexpensive workstations, produced in Europe, and will provide a gateway to the increasingly sophisticated VLSI technology for electronic and system designers.

In its first half, the project made great strides towards achieving its objectives. The functional 3D modelling problem were essentially solved, the silicon compilation tools made available were capable of handling not only classical gate-array and macrocell designs, but also the newer sea-of-gate structures and there have been on-going releases of the cell generation system (ASTRA) and the SPIRIT system. ASTRA is a development of BTMC, which has been incorporated into the system, whilst SPIRIT is a commercially available package based on the work carried out in the previous project and the first part of this. A new workpackage was added to the project to take care of generating and incorporating test data with the hierarchical verification tools developed.

The project aimed to achieve its objectives by the clever and extensive use of internationally accepted software and designs standards which would allow the design system to meet its objective to run on a large variety of commonly available work stations. This was to be done by employing new concepts in database design (specifically the use of a new semantic data model) and by tailoring design tools (verification as well as synthesis or compilation tools) to fit into and make efficient use of the optimally structured data.

Furthermore, the system was to offer newly conceived design tools fitting the trend towards close-to-micron or submicron circuits, especially in the area of

artwork-verification, layout-to-circuit extraction and redundancy-design for wafer scale integration.

The ICD project has now reached a state where its goals have been generally achieved. Its main output will be a prototypical system dubbed "ICD Release I", which incorporates all the major contributions of the partners, integrated around a common database frame. This system is already present in prerelease form and has been the subject of international attention and recognition. Specifically it received the first prize at the floorplanning competition of the 1988 IEEE Workshop on Placement and Routing. It pioneered a novel open-frame concept which was well received at the 1988 DAC conference, it succeeded in providing solutions to major problems in silicon compilation, 3D layout verification, fault modelling and testing, and last but not least, it was instrumental in pioneering novel parallel architectures for time-critical data processing.

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Start Date	**Duration**	**Status**
01-JAN-85	*39 months*	*Finished*

0.5 MICRON X-RAY LITHOGRAPHY: SOURCES, MASKS, RESIST AND TRANSFERRED IMAGE

PROJECT NUMBER: 1007

The project aimed at a technology compatible with X-rays from 7 Å to about 13 Å, so that resolution down to 0.25 micron may be eventually achieved.

The main tasks of this project were: Masks, Resist and X-ray Lithography Process.

Masks:

Nonhydrogenated SiC membranes are fully operational on 2-inch wafers. Transfer of the process to 4-inch wafers was shown to be feasible.

In pattern transfer, <0.5 micron resolution was achieved by two techniques:

- A subtractive technique, consisting of tungsten R.I.E. involving a trilevel resist process. It was shown to be fully compatible with <0.5 micron dimensions. The technique was analyzed in relation to stress, e-beam patterning and quality of image transfer.
- Electroplating of Au by a single-layer resist process was achieved. The process was fully consolidated and characterised. Furthermore, a new process was presented allowing the use of thinner absorber structures (3-4000 Å). Finally, experiments of mask copying by X-ray lithography were carried out.

Resists:

The development of an original positive fluorinated resist was optimised. An original negative resist (PVS) was tested and compared with the silicon negative resist from TOYO SODA and negative MES-E resist from Japan synthetic rubber.

X-Ray Lithography Process:

The MX 1600 X-Ray stepper from Micronix was operational within the project. Furthermore, the development work of the laser plasma source provided the project with the most promising alternative source to compact synchrotrons.

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Start Date	**Duration**	**Status**
01-JAN-86	*30 months*	*Finished*

ADVANCED MASK AND RETICLE TECHNOLOGY FOR VLSI SUB-MICRON MICROELECTRONICS DEVICES

PROJECT NUMBER: 1043

The fabrication of masks and reticles forms a key step in the manufacture of integrated circuits. As VLSI circuit complexity increases, the role of mask-making becomes increasingly demanding and the quality criteria even more exacting, so that improvements in high quality mask technology directly affect the competitiveness of Europe's semiconductor industry.

This project addressed specific areas of both E-beam and optical mask-making processes to develop new equipment, materials and processes. The objective was to combine such developments to create an enhanced mask and reticle technology to satisfy the wafer fabrication requirements for advanced and complex devices.

The development plan, where significant advances were made, included:

- the production of 5X reticles containing 2 micron minimum feature size
- laser pattern generation of 5X reticles
- control of 1 micron dimensions at 1X to a tolerance of + /- 0.1 micron
- microedge acuity of chrome oxide films to + /- 0.05 micron or better
- the development of chemical processes compatible with E-beam and UV optical resist technologies
- the manufacture of high yield/low defect density masks and reticles at 1X and 5X
- the development of new and existing resists for E-beam and optical microlithography
- the establishment of European suppliers of high quality materials and superior equipment.

A working prototype of a 2-laser Pattern Generator (PG), the basic machine for the production of these advanced masks, was installed and tested. Valuable experience was gained on laser exposure of resists, though improvements in the PG exposure rate could still be made. Studies on chrome blanks, resist technology and wet etching, both for E-beam and optical processes, were successfully assessed.

Prototype equipment, in the form of a 2-laser illuminator for optical pattern generators, advanced masks and reticle cleaning station, novel dry etch chrome

mask equipment and a new electron beam resist, were evaluated within this project.

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Start Date	**Duration**	**Status**
17-DEC-85	*36 months*	*Finished*

ULTRASENSITIVE IMPURITY ANALYSIS FOR SEMICONDUCTOR STRUCTURES AND MATERIALS

PROJECT NUMBER: 1056

The objective of the project is to develop an advanced physical analysis technique which will be of great importance for the European microelectronics industry as a diagnostic and control tool for contamination detection and doping profile determination. The new technique is based on a fundamental improvement of the standard Secondary Ion Mass Spectroscopy (SIMS) technique through the use of resonant laser excitation of sputtered atoms into Rydberg states, followed by electric field ionisation. Hence the appellation LASIMS (Laser Assisted SIMS).

Following the initial planning and feasibility study stages, the project entered, in 1988, into an intensive construction phase carried out by IMEC and Cameca, with a consequent reduction of the involvement of Siemens and Philips.

Given the budget and time scale of the project, it was decided to use a modified commercial SMI-300 Cameca instrument, instead of constructing a totally new one, to experimentally verify the LASIMS concept.

The original SMI-300 was fitted with a new spectrometer resulting in a system very close to the latest Cameca-3f configuration, which has the advantage of easy transferability of the LASIMS approach to already existing commercial systems.

A new UHV-compatible chamber has been constructed, while the LASIMS source and secondary ion optics have been conceived and detailed manufacturing drawings have been executed. Work has also started on the pulsed primary column. Particular attention has been paid to the necessary electronics.

By 1990, a functioning preprototype will be constructed and conclusions regarding the performances of a full prototype will be reached. It is the intention of one of the partners to develop a product based on the preprototype and of another partner to organise a service facility.

This laser assisted SIMS technique (LASIMS) is expected to achieve great improvement in sensitivity over standard SIMS, and to practically eliminate matrix effects. It will be particularly suitable for multilayer structure profiling.

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Start Date	**Duration**	**Status**
03-APR-86	*48 months*	*Running*

KNOWLEDGE-BASED DESIGN ASSISTANT FOR MODULAR VLSI DESIGN

PROJECT NUMBER: 1058

The objective is the production of an interactive knowledge-based system for verification of electrical, functional and timing correctness of flexible VLSI modules as generated by silicon compilers.

This is a complementary project with project 887.

This objective is to be met by the two major work packages of the project. Firstly, an interactive user interface and open system architecture which allows for a fluent and fast interactive communication between intelligent application tools and VLSI module designer will be produced. Secondly, intelligent application tools which are built using knowledge-based concepts for allowing timing and electrical verification by analysis and intelligent simulation, will be provided.

A rule-based expert system is to control the floorplanner's module assembly; it will be ported from an advanced LISP machine to a high performance engineering workstation for use in the project.

A waveform-based analysis technique will allow for "real time" user interaction supported by an advanced multiwindow user interface. The adaptation of a register-transfer-functional switch level simulator to the hardware accelerator will be investigated. A knowledge-based circuit extractor will provide a link to symbolic/procedural module layout generators.

The structure procedure interface (SPI) standard is a key concept in this system architecture. It is a dynamic data-passing concept to let programs communicate with each other on structural items. The SPI definition has been set up and implemented in a number of demonstrator applications, where programs are directly linked in one executable module via the SPI procedures. This illustrates that using SPI, programs can interactively communicate on structural information in order to e.g. directly highlight schematics or the symbolic layout frame within the timing verifier. More programs are to be interfaced to SPI.

Further extensions have been done on the timing verification program. The pattern recognition syntax has been redefined. The verification of modules (as realised in ESPRIT project number 97) is possible. The checking of the logical equivalence between two logic equations (tautology check) can be done. This is a basic function needed to compare logic behaviour at two levels of abstraction.

The rule-based electrical verification system has been extensively documented and its efficiency increased by two orders of magnitude; this was done by directly compiling the rule base in LISP code. The rule bases are to be generalised.

The algorithms used in the waveform-based circuit simulator have been documented and a prototype version has been implemented and tested on the available parallel processing hardware.

A flexible, technology-independent link between verification and symbolic layout has been made so that circuit extraction for use in the verification comes directly from the symbolic layout. The extracted information is formalised in the technology description language (TDL).

A verification speed of 20 000 transistors/h is projected. A novel waveform relaxation switch-circuit level simulator implemented on a multiprocessor hardware accelerator embedded in the system, will lead to 100 to 300 times, the SPICE performance. This will be achieved by exploiting a new explicit event-oriented integration scheme and by exploiting parallelism. The research done on a SEQUENT parallel processing machine will allow for efficient and accurate simulation of 4000 transistor circuits.

The project is currently working on a two-phase integration of all the CAD tools. In Phase 1 a prototype design system will be assembled around SPI. Phase 2 will use evaluation results of Phase 1 to improve and make a solid final version.

As the tendency in the CAD for VLSI is moving more and more towards the concept of a platform on which CAD tools can be built and interchanged, and as this is one of the goals of ECIP, the complementary nature of this project and ECIP could result in a very competitive European approach.

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Start Date	**Duration**	**Status**
01-JAN-85	*48 months*	*Running*

LARGE-DIAMETER SEMI-INSULATING GAAS SUBSTRATES SUITABLE FOR LSI CIRCUITS

PROJECT NUMBER: 1128

GaAs integrated circuits use an n-type active layer prepared by ion implantation of donors directly in semi-insulating wafers, followed by an annealing to cure the implantation damage. In order to realise LSI circuits, one must control accurately the properties of each individual FET transistor. This can only be achieved if the active layer is itself under perfect control.

This project developed an industrial approach for the preparation of large diameter (75 mm and 100 mm) semi-insulating GaAs substrates which can allow the preparation of very homogeneous active layers by ion implantation and then, by mapping the relevant properties of each individual micro-FET made on it, for feedback on the growth conditions.

Three different goals have been addressed:

- Methods to define material homogeneity for ingots of large diameter, by correlation between results of physical characterisation made on bulk material and of device measurements on processed wafers cut from it.

- Techniques to improve crystalline quality.

- Growth of ingots of large diameter of suitable quality for LSI manufacturing using the recipes worked out previously.

There has been good progress towards these goals:

- The parameters of the thermal model developed by UCL have been adapted to the pullers available in this project.

- 75 mm and even 100 mm diameter ingots have been grown successfully and made available to other ESPRIT participants to further check their suitability for IC manufacturing.

- Best yield in 1K SRAMs has been obtained on wafers grown during this project.

- It has been shown that fully undoped GaAs wafers obtained by using special conditions and post-growth annealing treatment can meet the LSI grade specifications, and can even be better than In-alloyed dislocation-free substrates.

The results of this project have a direct and major impact in the capability of one of the partners in supplying the best LSI-grade GaAs crystals in the world. At the end of the project 75 mm diameter semi-insulating GaAs crystals have been made

available under normal commercial conditions and 100 mm are expected in the near future.

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Start Date	**Duration**	**Status**
01-JAN-86	*36 months*	*Finished*

ADVANCED PROCESSING TECHNOLOGY FOR GAAS MODULATION DOPED TRANSISTORS AND LASERS

PROJECT NUMBER: 1270

The primary objective is the establishment and demonstration of molecular beam epitaxy (MBE) structures of heterojunctions, superlattices and GaAs device field-effect transistors based on combined laser-MBE processing.

The efforts in laser-MBE processing of GaAs MBE layers and laser processing of thin film diffusion barriers are directly applied to process field-effect transistors as test structures, which are tested both for electrical performance and reliability. These results are extended to a range of gallium arsenide integrated circuit technologies based on GaAs MESFET, high electron mobility transistors (HEMT/TEGFET) and heterojunction bipolar transistors (HBT) as the circuit elements.

Some impressive results have already been achieved:

- GaAs HEMTs, grown by MBE, have shown 50% power efficiency at 26.5 dB output power level and 26.5 GHz.

- Other HEMTs (0.7 - 1 micron gate) have operated at 20 GHz with 1.3-2.0 dB noise figure.

In addition, some GaAs on Si hetero-epitaxial wafers have been grown and were used to fabricate MESFETs which have a best transconductance of 180 ms/mm.

This project will have explored some new techniques for III-V semi-conductor processing, evaluated them and demonstrated their usefulness, together with developing adapted equipments (i.e. excimer lasers).

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Start Date	**Duration**	**Status**
01-DEC-86	*36 months*	*Running*

ADVANCED MANUFACTURING SYSTEM (AMS)

PROJECT NUMBER: 1551

The manufacturing process of ICs has special requirements concerning the establishment of long term strategy on software and hardware packages for its full automation. The objective is to satisfy those requirements within an advanced integrated manufacturing system concept. In particular, attention is to be given to problems associated with increased fabrication complexity, small device geometries, large chip size, flexibility (process, product, equipment, facility etc.), increased yield (maintenance concept, process stability, people and process-production interactions), increased wafer diameter, new process concepts, automation, and fast cycle time for material.

These topics will be addressed in particular:

- production information system
- networking, communication, interfaces
- automation island definition and experiment
- facility monitoring system
- material handling systems
- manufacturing line integration
- manufacturing requirements with emphasis on quality, service and production cost issues.

The system demonstration is expected around two automation islands, photolithography and diffusion.

The project has now passed its mid-term (2.5 years).

During the first year of the project, comprehensive studies and requirement analyses have been carried out and reports have been delivered primarily on the following:

- application model and functional architecture of the production information system
- statistical process modelling
- definition of network requirements and evaluation of software packages
- connection of equipment with host computers

- linkage of equipment in the photolithography area
- analysis and requirements for material handling systems
- software and hardware flexibility for automated VLSI manufacturing.

An initial demonstrator has been set up in the photolithography area.

In the second year and the first half of the third year work has been devoted mainly to the definition of a common model of CAM system, equipment interfacing, automation island, software and sensors for facility monitoring, wafer storage and transportation, wafer marking, modeling and fab simulation.

Process line integration/automation has now become one of the key factors of success in the manufacturing of commodity or specialised (ASIC) ICs.

It is anticipated that successful completion of the project and subsequent exploitation of its results will help the Community IC manufacturers concerned to improve their manufacturing capabilities. Within the activities of this project a special interest group on VLSI manufacturing standards has been set up which other Community organisations are invited to attend. In this way it is expected to ensure harmonisation and further increase the impact of the project.

This is a 4-year project, and full demonstration is envisaged for the last year (1990) to be followed by implementation.

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Start Date	**Duration**	**Status**
09-DEC-86	*48 months*	*Running*

AUTOMATIC CONTROL OF AN ASIC FABRICATION SEQUE (ACAFS) AS DEMONSTRATED IN THE PLASMA ETCH ARE

PROJECT NUMBER: 1563

The objective of the project is to develop a methodology and acquire know-how for a wafer fabrication sequence control system. Because of its critical nature the Plasma Etch area has been the one chosen in which to implement the methodology. The work will involve several domains such as optical sensor integration for "smart" information collection, plasma etching process modelling for control and supervision purposes, communication between equipment manipulators and computers, as well as hardware and software for real-time processing. Recent powerful techniques in model identification, multivariable process control and artificial intelligence will be used to address efficiently the various control, supervision, and decision-making problems related to the proposed hierarchical control structure.

Specification of the "controller" which forms the core of the system has been produced defining a common starting point for the project. This controller will implement the features needed to reach the project objective, namely automatic etch process control and equipment supervision. The controller has been extensively tested on a station which uses a computer to simulate the etching process behaviour.

An evaluation of various automated product tracking and transfer approaches was made in the first two years.

Work has been completed in extracting yield affecting parameters and in developing statistical models to predict etch process results from process parameters. The necessary studies have been realised on appropriate test structures.

At the end of the first two-year period, one of the partners, Leybold AG, decided to cease its participation in the continuation of the project. With some technical modifications (the most important being the dropping of the construction of the wafer-handling system) the project will go on with the remaining partners. Based on the experience of the first two-year period, the highly sensitive metallisation etching was chosen as the process to be used in the final demonstrator of the whole automatic control concept. This will be implemented on the production line of one of the participants. Over the last two-year period added emphasis is being put on enhancing the fault detection and machine maintenance scheduling capabilities of the system.

An evaluation of various sensors best suited for measuring selected process parameters has been made. In particular, optical emission spectroscopy for general plasma analysis purposes and various interferometric techniques for on-line etch rate determination have been looked at in detail. Appropriate sensor

have been installed and interfaced on industrial etchers at partner sites. More advanced sensor concepts are being looked into over the last two years of the project.

The project is expected to have significant impact in three main domains:

- improvement of chip yields as a result of the utilisation of the methodology
- realisation of more competitive equipment and systems
- implementation of standards.

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Start Date	**Duration**	**Status**
01-APR-87	*48 months*	*Running*

ESPRIT II PROJECTS

DEVELOPMENT OF EUROPEAN MAGNETO-OPTICAL DRIVES

PROJECT NUMBER: 2013

Market research undertaken by the consortium confirmed the main results obtained by other market surveys (Consultronique, Dataquest). The erasable optical data storage market will escalate in 1991/92 and will be substantial by the mid-1990s (1.5 BECU), with mainframe back-up and CAD/CAM as key applications.

These markets should exceed 150 MECU each in 1991/92 with a large part of them presently in hands of overseas competitors, and will increase exponentially after this.

In the case of CAD/CAM, a data capacity greater than 1 Gbyte is required to cope with the higher resolution pictures of up to 30 Mbytes per page which will be used. Access time of less than 50 ms and data transfer rate of at least 20 Mbits/s are also required.

The objective of this project is to establish the technologies to develop two erasable optical drives and to give to European companies new opportunities to restore their position in the mass storage area:

- the first is a removable drive enabling European industry to quickly enter the CAD/CAM and back-up memory markets

- the second is an advanced fixed-disc multiplatter drive for later release in the same market.

General objectives are as follows:

Medium-Term (3 years)

- Development of a new formatted 5.25" disc on a glass or polycarbonate substrate, with a user capacity of 1 to 1.5 GByte.

- Development of a prototype of an erasable optical drive with:

  - removable cartridge
  - access time from 25 to 50 ms
  - average data transfer rate higher than 4 Mbits/s
  - standard SCSI interface
  - SCSI maximum burst transfer rate higher than 32 Mbits/s.

Longer-Term (5 years)

- Improvement of the 5.25" media for "direct overwriting" and for a 10 year projected lifetime.

- Completion of an integrated optical head.

- Mockup of a improved long life (10 years) erasable optical drive with the following features:

  - use of novel light integrated magneto-optical heads
  - fixed discs in a 5 Gbyte multiplatter drive
  - access time from 20 to 40 ms
  - average data transfer rate higher than 16 Mbits/s
  - standard SCSI interface
  - SCSI maximum burst transfer rate higher than 32 Mbits/s

Systems demonstrations of both types of drives prototypes should confirm that they are compatible with a large range of computers.

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Start Date	**Duration**	**Status**
01-JUN-89	*60 months*	*Running*

BIPOLAR ADVANCED SILICON FOR EUROPE (BASE) - TIP

PROJECT NUMBER: 2016

The goal of the project is to develop and fully integrate technology expertise in the deep submicron range as well as design and CAD achievements.

The development plan proceeds in two phases yielding interim (Y1) and final (Y2) process versions after year 3 and year 5, with the following target specifications:

Process Characteristics	*Process (V1)*	*Process (V2)*
emitter width (mininum)	*0.7 micron*	*0.3 micron*
gate delay	*50 ps*	*40 ps*
power delay product	*40 fJ*	*10 fJ*
no. interconn. layers	*3*	*4*
via pitch (minimum)	*3.5*	*2*
transit frequency (maximum)	*15 GHz*	*25 GHz*
transit count (maximum)	10^5	$5x10^5$

The process versions V1 and V2, which are oriented to a high level of maturity, are complemented by experimental processes yielding values as high as 40 GHz for the maximum transit frequency, CML gate delays of no more than 30 ps and power delay products below 10 fJ. For comparison, present pilot production processes worldwide and also at the partners are characterised by 1 to 1.5 micron emitter widths, around 80 to 100 ps gate delays, 3 interconnect layers at around 5 micron minimum via pitch and maximum complexities of up to 4.10^4 transistor functions.

Very high speed bipolar technology fills a very important area between the lower performance but higher complexity per chip, provided by MOS technology, and the extreme device speed but lower complexity per chip, higher cost per function, and limited availability of gallium arsenide. Bipolar technology is best suited for high precision, high complexity and high speed systems of future information technology because its analogue features are best, its intrinsic speed is excellent, its transconductance (driving capability) is best and availability as well as future perspectives are excellent. Higher data processing rates, broader bandwidth communication and increased use of digital signal processing techniques all demand the use of advanced bipolar technology.

During the project execution several product prototypes will be realised. These prototypes will complement the demonstrators of the performances of the processes (which constitute the normal deliveries of the project) in order to further illustrate their relevance to the Information Technology industry, notably for applications in the field of consumer, telecom electronics, fast data and signal

processing, high speed ASICs and USICs and instrumentation. A wide range of possible products has been considered. These include:

- ultra high speed circuits of low complexity such as pre-scalers and synthesisers at 10 GHz and above
- optical communications circuits (MUX, DEMUX, mixer etc.) in the 2.4, 4.8 and 9.6 GHz bands
- specialised gate arrays incorporating memory
- complex multiplier - 16x16 with 1.5ns multiply time
- telecommunication circuits such as the 4.8 Gbit/s (600 Mbit, 8x8)
- asynchronous switch, and circuits for 10 Gbit/s transmission systems, needed in RACE
- RGB Video DAC for high resolution graphics controller
- ultra high speed and high resolution ADCs for digital radio and low cost civil radar
- sub-nanosecond static RAM.

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Start Date	**Duration**	**Status**
01-FEB-89	*60 months*	*Running*

ADVANCED GAINAS-BASED DEVICES FOR HIGH-SPEED INTEGRATED CIRCUITS

PROJECT NUMBER: 2035

This project, involving 5 major European companies, will examine the high speed performance of a number of GaInAs-based devices and is expected to produce state-of-the-art circuits for IT systems using those devices showing the greatest performance potential and suitability for integration. GaInAs-based material structures were chosen (a) because of their considerably superior transport properties (high electron mobility, high saturation velocity) to GaAs leading to a new generation of high speed devices and (b) because the basic fabrication technology of transistors made in these material structures should not be vastly different from GaAs MESFETs. The programme is built on the technological achievements of previous ESPRIT I compound semiconductor projects and it is hoped that this will lead to an early realisation of devices and circuits with superior performance to those existing at present.

The material growth techniques to be employed on this project are MOCVD and MBE and the growth conditions will be optimised in the light of initial device results. Device fabrication techniques such as lithography, contacting, dry processing, and ion implantation will be developed for the realisation of the following demonstrator devices:

- pseudomorphic HEMTs: GaInAs channels grown strained on GaAs substrates
- lattice-matched HEMTs: AlInAs barriers and GaInAs channels grown lattice matched on InP substrates
- GaInAs junction FETs
- pseudomorphic GaInAs channel SISFETs on GaAs or InP substrates.

The performance of these demonstrator devices will be compared for their use in the following circuits, which later could form the basis of the building blocks for specific IT subsystems:

- a broadband 30 GHz amplifier
- a 1-2 GHz pulse regenerator circuit
- a 30 GHz divider
- inverter and ring oscillator circuits.

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Start Date	**Duration**	**Status**
01-JAN-89	*36 months*	*Running*

ADVANCED PROM BUILDING BLOCKS (APBB) - TIP

PROJECT NUMBER: 2039

The objective of this TIP is the integration of a new generation of re-programmable, read-only memory devices (PROMs) into advanced CMOS processes for the application specific market. To do this, the necessary CAD tools required to support non-volatile memory designs will also be developed. The work is divided into two phases, the first from years 1 to 3 and the second from years 3 to 5, with an overlap in year 3. In phase one, existing and new memory devices will be evaluated and developed. Suitable cells will be incorporated into one-micron and low voltage (1.5 V, 2 micron design rule) CMOS processes. In phase two, advanced devices will be integrated into increased density low voltage (1.5 V, 1.5 micron) and sub-micron (0.7 - 0.8 micron) CMOS processes.

Many technical problems will need to be solved. In fact, in addition to the normal ones relating to making everything smaller, faster, cheaper and lower power, there is a major incompatibility between the drive to thinner oxides and lower voltages in standard CMOS and the need for the rather high programming voltages in EPROM and EEPROM circuits. This will require significant advances in either the reduction of programming voltages or in the addition of high voltages handling to the CMOS or both, while at the same time maintaining or improving reliability. These problems are particularly severe in achieving compatibility with 1.5 V CMOS, and the generation of the programming voltage from such a low supply is a major challenge.

Furthermore, cell libraries and CAD tools for non-volatile memory are virtually non-existent today. During the project cell libraries will be created for EPROM and EEPROM blocks and distributed memory together with all the support circuitry such as decoders, sense amplifiers, high voltage generators etc. CAD tools to design and correctly match memory blocks of arbitrary size will be developed, as well as routing tools to handle the special high voltage requirements.

The ease of use and the flexibility of the CAD, design and test tools will be particularly important in making this technology available to small and medium enterprises (SMEs). The establishment of several design centres in small companies, institutes or universities is planned, where staff can be trained in the use of the design tools and who can then act as an interface to the wider SME community.

The programme is divided into eight main packages which will:

- review applications and identify the technology, circuit techniques and CAD tools required for each of them

- evaluate memory devices by fabrication and modelling

- develop process steps for CMOS-compatible PROM fabrication

- optimise processes to a level suitable for the demonstrators
- provide the CAD tools necessary for the exploitation of the non-volatile programmable memory functions
- construct the building blocks for system designers (the "customers")
- develop appropriate test methods and programmes
- construct demonstrators to show the process and design capabilities.

In particular, the successful execution of each of the two phases is to be proven by product oriented demonstrators, containing everything from small, distributed memory registers to large embedded memory blocks. They will cover a broad range of industrial applications.

In the first phase, a micro-controller chip incorporating both EEPROM and EPROM (or an equivalent complexity circuit such as a smart card), a circuit for "chip tagging" (containing a moderate to high density of transistors but a smaller amount of non-volatile memory), and a low voltage custom chip using EEPROM cells will be provided.

The purpose of the second phase is to demonstrate, at sub-micron, a transistor density in the range 200 to 500 K, the capability for a larger density of building blocks (up to 64kbits of EEPROM in a chip), and the flexibility for different applications: EEPROM with a single polysilicon layer for low cost applications, EPROM and EEPROM in double poly for high density circuits. At 1.5 microns, low voltage, low power circuits with increased complexity will be demonstrated.

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Start Date	**Duration**	**Status**
15-DEC-88	*36 months*	*Running*

DEEP UV LITHOGRAPHY

PROJECT NUMBER: 2048

The overall objective is to develop the equipment and basic processes required for a high-throughput pattern definition capability with 0.25 micron resolution, that can be applied in the manufacturing process of all types of semiconductor devices. A modular concept is envisaged, which can be configured to meet the production needs of the full range of devices from high volume memories to low volume ASICs.

More specifically, this project will develop the equipment, materials and techniques necessary for delineation of sub-halfmicron patterns. Included are a deep UV wafer stepper, compatible photoresist systems, and a study into the necessary resist processing, automation and environmental aspects with the goal of process integration in mind.

The project comprises three interdependent work packages covering the development of:

- a deep UV wafer stepper with excimer laser (248 nm) illumination

- deep UV photoresists, compatible with 248 nm illumination

- automation and environmental engineering for the integration of equipment, and especially of the deep UV stepper, in the clean room.

The planned deep UV stepper will have 5X reduction all-quartz optics with narrow band excimer laser illumination. A new alignment system will be incorporated to meet the overlay requirements for sub-halfmicron device technology. Two resist systems will be developed, the first a high resolution single layer positive photoresist, the second a high contrast, multi-layer resist. Studies on how to integrate the deep UV wafer stepper with respect to environmental control (contamination, temperature) and interfacing (reticle management, automation) will be performed.

The total system, stepper and resist, will be capable of printing sub-halfmicron feature sizes. With enhanced resist processing techniques the feasibility of 0.25 micron structure printing will be investigated. These results are envisaged at the end of the three-year project (end 1991).

Presently, the European integrated circuit industry is preparing for production of devices with minimum feature size near 0.8 micron, with the 4 Megabit DRAM as a typical example. In order to remain competitive, the European industry must have production capability for minimum details below 0.5 micron in the early 1990s, with the potential to extend down to 0.25 micron in the mid-1990s. Extrapolating present trends, the microcircuits will then have the complexity of 64 Mbit DRAMs. Many production requirements must be addressed for this increased integration,

but central among these is the lithography and pattern transfer, since these strategic techniques define the minimum feature size and packing density of the new devices. It is precisely in this area that the present project expects to have a major impact.

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Start Date	**Duration**	**Status**
15-NOV-88	*36 months*	*Running*

ADVANCED PACKAGING FOR HIGH PERFORMANCE (APACHIP)

PROJECT NUMBER: 2075

The APACHIP project covers the field of work in advanced VLSI packaging. It is addressing advanced packaging solutions for multichip modules as well as for single chip package applications.

The project will provide packaging solutions for highly integrated bipolar circuits requiring liquid cooling, but will also present solutions for packaging of even more integrated MOS VLSIs for which air-cooling techniques can still be applied.

The VLSIs, whether bipolar or MOS, will be assembled using Tape Automated Bonding (TAB). The necessary corresponding TAB tape will be developed in the Project and introduced to the European market.

The efficient interconnection of the VLSIs requires the availability of high density, high performance substrates. Two different approaches of high density substrate realisation are included in the project. One proceeds from printed circuit board-like technology to achieve very dense interconnection and miniature laser formed vias; the other approach uses thin film deposited and electrolytically reinforced copper lines separated by polyimide layers. This copper-polyimide structure is applied on large size ceramic substrate, also developed in the project.

The multichip or single chip substrates populated with TAB chips are to be tested and connected into the systems. This requires the availability of a new connector concept which will be defined in the project.

Electrical modelling in order to precisely anticipate the electrical signal behaviour in a real packaging environment, as well as reliability aspects and new inspection methods are included.

Most of the innovations will be applied into representative test vehicles which will be provided as the proof of the existence of more advanced technology within the partners' companies. They will be the basis from which products shippable to the market can be generated with only a limited additional development effort.

The marketable products will be not only packaged electronic sub-assemblies within electronic systems, but also packaging material supplies (TAB tapes, ceramic packages, etc.) necessary for an advanced European electronic industry.

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Start Date	**Duration**	**Status**
01-DEC-88	*48 months*	*Running*

ELECTRO-THERMAL RIBBON (ETR)

PROJECT NUMBER: 2125

The development of a dot printing technology, considering the very high quality obtainable on all kind of paper and the relative low cost of the printing mechanism, can constitute a good solution for typewriters and high quality printers to be attached to personal computers. Accordingly, dot printing systems may have a widespread use in workstations, word processors, high and low end typewriters and printers.

ETR is a dot-type printing system without impact (and therefore silent), able to print in both alphanumeric and graphic mode at very high resolution, with an excellent quality on every kind of paper.

It is a thermal printing technology, using a solid ink deposited on a ribbon, softened by heat and then transferred to the paper. It can be considered as an evolution of the conventional thermal systems.

As a first step, in order to fully exploit the potential of this technology, the project will address every key element both from the theoretical and practical point of view. This should enable the consortium to reach the most up-to-date level in the present technology and to increase its know-how for further improvements. Some new ideas concern the development of a completely different system for the deposition of the metallic layer, used as a return current path in the ribbon. The use of a base layer with a completely different structure will be investigated as well.

At the same time a different printhead should be developed taking into account the requirements for a higher printing speed, such as resistance to wear and thermal dissipation.

The last step should be the development of a prototype using a ribbon without the presently used metallic layer. In this case, the printhead may also have to be completely redesigned.

The project also plans to investigate new ideas and to implement known technological processes (such as Direct Current Magnetron sputtering of thin metallic layers on polymeric substrates) not yet used in the thermal ribbon production.

All the components of the present and future technology are or can be made by European companies (parts for ribbon and printheads, electronic drivers, printing mechanism). All the know-how, including all the processes needed to achieve the whole structure of ribbons and heads, will be owned by the European partners and then should allow them to strengthen their market position.

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MANCHESTER POLYTECHNIC	*UK*	*P*
AEG OLYMPIA	*D*	*P*

Start Date	**Duration**	**Status**
01-MAR-89	*36 Months*	*Running*

ANALOGUE/DIGITAL CMOS ICS (ADCIS)

PROJECT NUMBER: 2193

The integration of analogue and digital functions on a single chip is necessary for the development of new systems for information technology for data communication, industrial and consumer systems.

During the proposed project a 1 micron CMOS process will be adapted and characterised for mixed analogue-digital function and an electrical parameter of a submicron CMOS technology will be extracted. The devices from the digital CMOS technology and the necessary analogue-adapted process modules will be defined and characterised.

At the same time, the development of design tools will be started, with the goal of building a system capable of being used to produce silicon compilers involving digital and analogue cells. The CAD tools will be tested and demonstrated, analogue cell library and analogue basic converter functional blocks will be developed, and one industrial demonstrator circuit will be designed and processed.

The circuit considered for the demonstration of the analogue-digital CMOS technology is a component for the ISDN new telecommunication system.

The circuit will integrate, on a single chip, the S interface function (SIC, "S" loop controller) and the dual protocol controller (DLC). The developments carried out in this project will make possible the integration in one chip of two circuits DLC + DPC, offering low cost and clean hardware/software partitioning between the ISDN card and the host processor.

To manage properly the line interface precise analogue functions need to be integrated such as:

- analogue reference for both emission and reception
- switch capacitors filters for signal reception
- amplifiers and comparators for both reception and line driving.

The complex data processing is controlled internally to the chip by an 8-bit microcontroller core emulating the 80C31 instruction set.

The chip size will be around 50 mm and the chip will integrate more than 120 000 transistors.

The manufacturing cost will be evaluated by comparing the number of steps in the process flow of the wafer fabrication with other process techniques currently used to manufacture mixed analogue/digital circuits at the same integration level.

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NMRC	*IRL*	*P*
UNIVERSIDAD DE SEVILLA	*E*	*P*
MIETEC	*B*	*P*
INSTITUTO SUPERIOR TECNICO	*P*	*P*
CNET	*F*	*P*

Start Date	**Duration**	**Status**
01-JAN-89	*36 months*	*Running*

PROCESS MODELLING AND DEVICE OPTIMISATION FOR SUBMICRON TECHNOLOGIES (STORM)

PROJECT NUMBER: 2197

The objective is to develop a tool capable of simulating CMOS and bipolar device processes. The end product will be a simulation environment, called the "Project Code", which will incorporate advanced modules for process and device simulation, optimisation algorithms, and user interface. Incorporated within the code will be a set of more accurate models for the simulation of newly developed processes such as rapid thermal annealing, impurity diffusion from polysilicon and silicide, trench isolation, high energy and multilayer ion implantation, non-planar lithography, chemical vapour deposition, and glass reflow.

The design of semiconductor devices is a complex task which has a strategic role in IC design and manufacturing. The performance of electronic systems is strongly related to the design of the technological processes which determine the basic performances of the ICs used. Given the soaring costs of manufacturing complex ICs and the ever intensifying competition toward higher performances, it is imperative for IC manufacturers to have efficient and accurate simulation tools that will allow process optimisation at the design stage. This will reduce process runs to a minimum, thus saving time and money.

Three versions of the project code will be produced:

- A first (prototype) version will simply integrate the different state-of-the-art simulators (or modules of them) which are already available amongst the partners. This prototype will be released 12 months after the start of the project and will be demonstrated at the first annual review meeting.

- An intermediate version will merge the new or the improved models for process simulation, sensitivity analysis according to a significant list of process parameters, and first tentative optimisation algorithms. This version will be released 30 months after the start of the project.

- The final version will include consolidated models and optimisation programmes and will be released at the end of the project.

All three versions of the project code will be validated, starting from the second year of the project, on CMOS and bipolar technologies which are under development by 4 partners. The continuous feedback between validation and software development is essential in order to assure the necessary reliability and robustness of the environment.

STORM is organised around three main work packages. The first one will develop improved models for process simulation. For management reasons, it is divided in three sub-packages, dealing with Dopant Diffusion, Thermal Oxidation and Topography, and Ion Implantation, respectively. The second work package will

address optimisation techniques for device design with the aim to set up an automatic optimisation tool. The third work package will address Software Integration.

The Project Code aims to satisfy the needs of the IC industry in the years to come. In so far as it will simulate both CMOS and bipolar basic technologies, it will be able to handle the optimisation of future BICMOS processes as well.

By its nature, STORM is related to ESPRIT project numbers 554 (SPECTRE), 243, and TIP 2016 (BASE), in which some of the STORM partners are also involved. It is intended that all results developed in the course of the project will be made rapidly available to the European projects for CMOS and bipolar optimisation.

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PLESSEY UK Ltd.	*UK*	*P*
IMEC vzw	*B*	*P*
FRAUNHOFER INSTITUT (AIS and IMT)	*D*	*P*

Start Date	**Duration**	**Status**
01-FEB-89	*48 months*	*Running*

INTERACTIVE SILICON COMPILATION FOR HIGH-PERFORMANCE INTEGRATED SYSTEMS (SPRITE)

PROJECT NUMBER: 2260

The goal of this project is the development of a CAD system for the interactive synthesis of complex integrated systems as required for the realisation of real-time information processing subsystems such as image and graphics processing, post ISDN home and business peripherals, HDTV, coprocessors, data compression, etc.

The behavioural specification of a system is described in a mixed functional/procedural language. The synthesis system will compile the specifications into a chip layout using a mixture of knowledge-based and algorithmic techniques. It will be oriented towards a set of three high throughput target architectures with a variable degree of microcode programmability and parallelism. These three architectures are cooperating data paths, multiprocessor architectures and regular array architectures. A formalised knowledge base will be extracted from design of demonstrator chips.

Interactivity will be based on the pragma concept allowing for a fast exploration of the design space and the evaluation of quality factors such as power and area for a required throughput as a function of the architectural choice. This will automatically determine hardware-microcode trade-offs. In addition, CAD software for both on- and off-chip interprocessor communication will also be developed.

As the project is addressing data rates in the order of 10-50 Mbyte/sec and algorithms requiring in excess of 1000 MOPS, substantial effort will also be spent on performance optimisation techniques at the silicon module generation level. Efficient memory management and algorithmic transformations will be based on novel formal specification and verification techniques.

The project is furthermore based on experience resulting from actual cooperation between the partners in on-going projects.

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SIEMENS AG	*D*	*P*

Start Date	**Duration**	**Status**
01-DEC-88	*60 months*	*Running*

DRY DEVELOP OPTICAL LITHOGRAPHY FOR ULSI (DRYDEL)

PROJECT NUMBER: 2265

The work covered by the DRYDEL project is aiming at the development of a deep-UV sensitive photoresist with the purpose of extending the DESIRE (Diffusion Enhanced Silylating Resist) process to the 0.5 - 0.3 micron range.

This will be achieved through the following technical tasks:

- resist development
- processing, containing silylation, dry development and dry transfer of the resist pattern in the underlying layers
- a deep UV demonstrator to prove the applicability of the newly developed resist for the sub-halfmicron region.

An additional evaluation of the DESIRE process on GaAs will be carried out within the project.

In making available a new deep-UV sensitive photoresist optimised to the 0.5-0.3 micron range this project is expected to stretch the application range for optical lithography to the 0.3 micron critical dimension required for the next technology generation.

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PHILIPS GLOEILAMPENFABR.	*NL*	*P*
PLESSEY COMPANY PLC	*UK*	*P*
SIEMENS A.G.	*D*	*P*
UCB	*B*	*P*

Start Date	**Duration**	**Status**
01-DEC-88	*24 months*	*Running*

COMBINED ANALOGUE/DIGITAL INTEGRATION (CANDI)

PROJECT NUMBER: 2268

The project aims at the development of the main technologies and implementation techniques needed for the fabrication of complete analogue/digital (A/D) systems on silicon. This includes the development of a 0.8 micron bipolar-CMOS merged technology exploiting the specific advantages of both bipolar (high speed components, high driving capability and high precision analogue circuitry) and CMOS (high integration density and low power consumption) technologies. The associated design techniques and the appropriate CAD tools covering both analogue, digital and mixed A/D applications, as well as effective low-cost tools for complex A/D circuits testing, are also to be developed. The final objective is the full integration of technology, design and CAD tools implemented in the fabrication of prototype system components for major fields of applications such as consumer electronics and telecommunications.

The project has two phases. The first phase will last 18 months, starting with an adaptation of the main partners technology to provide an intermediate 1.2 micron process. This common 1.2 micron process will not only stand as an intermediate technical step, but will also form the basis of the 0.8 micron process and of the definition of the main CAD tools.

Three demonstrators are planned as a result of this first phase:

- A digital luminance and chrominance to analogue RGB components decoder suited for Improved Definition TV. Circuit complexity is around 35K transistors.

- A mixed A/D array for the integration and testing of the main parts of the receiver of the pan-European cellular radio. First estimations of process complexity result in approximately 13K gates and 350 UHF devices.

- A 16-channel bit-shuffler, consisting of about 8000 active devices, for 2.5 Gbit/s data transmission.

The second phase of the project will last two years, including a 6 months overlap with the first phase, and will lead to the development of the 0.8 micron process. Based on this, two final demonstrators will be provided:

- A videoprocessor for High Definition TV receivers (108 MHz operating frequency). The chip complexity can be evaluated at about 60K transistors.

- An enlarged mixed A/D array with the implementation of additional advanced functions with respect to the 1.2 micron version, for the pan-European cellular radio. In total 25K gates are to be customised together with 500 UHF devices.

Major system houses are associated in this project and will collaborate in the elaboration of a common cell library and to the design of the demonstrators. Part of the work will also be done in collaboration with universities and research institutions, in order to develop closer links between the research and industrial communities in Europe.

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UNIV. PARIS SUD	*F*	*A*
LER/LAB. ELECTRONICc DE RENNES	*F*	*A*

Start Date	**Duration**	**Status**
01-DEC-88	*36 months*	*Running*

INTEGRATED DESIGN AND PRODUCTION SYSTEM (IDPS) - TIP

PROJECT NUMBER: 2270

The project's aim is to provide to the European IT industry the basis of a full service for designing systems integrated on silicon, and for producing them in various foundries.

IDPS is aiming to achieve a total turnaround from the behavioural specification of a system to the corresponding tested working chip in approximately one month.

It will explore appropriate techniques for the creation of a design and fabrication environment for highly complex integrated circuits with the capability for fast turn around. This includes the development of appropriate CAD system architectures, advanced tool bases, interfaces and methods of integration to ensure optimisation of system performance. The generation of common library components represents a central part of the project and serves as a basis for advanced technology and process development and finally the silicon supply.

The project is based on the following set of concepts:

- portability of designs through silicon compilation techniques
- portability of tools between various CAD systems
- fast turnaround achievement through fine tuning and optimisation of standard pilot lines, rather than using very expensive dedicated prototype lines.

Three consecutive phases are envisaged in the project:

Phase 1, of one year duration, intends to validate the basic concepts underlying the project and prove its viability. Decision for continuation for four more years will be taken at the end of this first phase.

Phase 2, of two years' duration, will lead to the ability to turnaround a one million transistor circuit, starting from a structural description.

Phase 3, also of two years' duration, will lead to the ability to turnaround a circuit, partly defined at the behavioural level, and a with complexity of two million transistors.

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NIXDORF COMPUTER A.G.	*D*	*P*
PLESSEY COMPANY PLC	*UK*	*P*
SIEMENS A.G.	*D*	*P*
THOMSON-COMPOSANTS (TMS)	*F*	*A*
CNET/CNS	*F*	*A*

Start Date	Duration	Status
01-DEC-88	*12 months*	*Running*

TECHNOLOGICAL FEASIBILITY OF HIGH-VOLTAGE SMART POWER ICS FOR LIGHTING APPLICATIONS

PROJECT NUMBER: 2272

The goal of this project is to develop a high-voltage integrated circuit technology suitable for lamp ballast applications.

The main reasons calling for electronics in lamp ballast applications are:

- the energy saving obtained by the accurate control of the electrical parameters applied to the lamp
- the possibility of generating new light sources that need accurate control of electrical (voltage, current)
- the addition of features like dimming or remote control or flicker suppression or temperature colour control, which enhance the life of the lamp and optimise the light source to the needs of the user
- the fixing of the working point of the lamp (in terms of frequency, temperature, voltage, current) in the range where the lifetime is maximised.

The final objective of this project is to develop and evaluate integrable components and circuits (test vehicles) for applications in a wide variety of lamp circuits up to 650 V.

The following tasks are to be addressed:

- development of high voltage IC process and development of models for circuit simulation
- identification of any critical behaviour related to high voltage in standard packaging structures and evaluation of materials for high voltage packages
- design of macrocells and test vehicles dedicated to lampcircuits and evaluation of their behaviour in lamp driving application.

Within each of the above-mentioned activities the reliability evaluation of the circuits and the packages will be addressed.

The technology developed within the proposed project will contribute to establishing the know-how required to integrate high-voltage devices with control circuits of moderate complexity. The study of materials will provide a standard procedure to evaluate and compare the characteristics of different materials used in packages that have to withstand 650 V under severe ambient conditions. This is expected to increase the potential of the European semiconductor industry in high

voltage ICs and open clear opportunities for exploitation in the field of lamp ballast applications.

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UNIV. OF PISA	*I*	*A*
ALCATEL STANDARD ELEC.	*E*	*A*
NMRC	*IRL*	*A*
CSIC	*E*	*A*

Start Date	**Duration**	**Status**
01-JAN-89	*36 months*	*Running*

HIGH-T_C SUPERCONDUCTING THIN FILMS AND TUNNEL JUNCTION DEVICES (UNITED)

PROJECT NUMBER: 2281

Superconductivity above liquid nitrogen in $YBa_2Cu_3O_7$ family (YBCO), and more generally in high-Tc superconducting oxides (HTSO) allows the development of superconducting electronics working at reasonable temperature. Subsequent improvement of electronic properties, such as very fast circuits, may be of importance for information technology in particular and microelectronics in general. The fundamental building-block of most superconducting microelectronic devices involved in information technology is the Josephson junction.

The goals of this project are:

- The fabrication of reproducible superconducting HTSO thin films using promising and complementary techniques (Sputtering, Electron-beam coevaporation, Molecular Beam Epitaxy and laser ablation); high level characterisation will be used for the optimisation of the growth process.

- The fabrication and high level characterisation (structural and electrical properties) of intrinsic Josephson junctions.

- The demonstration of simple devices using intrinsic Josephson junctions and a Superconducting Quantum Interference Device (SQUID).

This demonstration of devices using intrinsic junctions together with the fabrication and characterisation of high-quality thin HTSO film will be a very important step towards a European capability to produce devices based on controlled HTSO layers junctions.

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UNIV. OF CAMBRIDGE	*UK*	*P*

Start Date	**Duration**	**Status**
15-JAN-89	*18 months*	*Running*

ACTIVE MATRIX LIQUID CRYSTAL DISPLAYS FOR TV AND OFFICE SYSTEMS

PROJECT NUMBER: 2283

Europe has held for a long time a distinguished record in the development and fabrication of liquid crystal materials. Today, the three companies Merck (D), BDH (UK) and Hoffman La Roche (CH) almost control the complete world market for these materials. Nevertheless, the European position on LC devices, components and sub-assemblies for panels is less favourable, and Japanese suppliers dominate the global market, with large sales in Europe.

There are, however, a number of European companies with the technical capabilities to produce LCDs and to compete in the worldwide arena, provided that production investments are mounted on an appropriate scale for a well-defined technology.

The objective of this project is to establish a fully validated technology for the production of active matrix LCDs for use within TV and office systems.

Investigation of the different technological requirements for the production of a large complex flat-panel display will be completed on the basis of results already obtained in ESPRIT I Projects 833 and 491. Such a display, compact and operating at low voltage, must be able to show colour and grey scale with high resolution and should be less bulky than current CRT devices in order to fulfil the office systems requirements in the near future. Present conventional twisted nematic LCDs show, when multiplexed addressing is used, less colour capabilities and image quality than required for high-resolution, full-colour office terminal displays. Even the "supertwist" displays recently developed cannot meet this kind of demand.

The approach, which is now widely recognised as the most promising, is to deposit a matrix of switching transistors on an inner wall of the LCD. Three of the partners have demonstrated their technical know-how in the field of active matrix panels by the realisation, at the laboratory level, of displays with viewing areas of approximately 10 x 10 cm and resolution up to 256 x 256 pixels (ESPRIT I project 833).

Although applications for such displays can already be envisaged in small portable equipment, it seems to be necessary to develop larger (A4) high resolution panels to meet the key requirements of office terminals. The main goal of the project is therefore to validate technologies for the production of active matrix LCDs up to A4 in size.

The work involves the preparation of direct view flat-panel displays using amorphous silicon with external ICs drivers in the short-term, or using polycrystalline silicon with integrated drivers as an alternative in the longer-term.

During the first three years of the programme the realisation of an A4 amorphous silicon AMLCD should be carried out, and in parallel a polycrystalline silicon process with integrated drivers and A4 glass compatibility, including A4 specific equipment, should be developed (6" diagonal demonstrator).

During the remaining two years of the program the most promising technology (a-Si or poly-Si with integrated drivers) should be implemented. In both cases a pilot line development should be started with A4 demonstrators of about 10 x 6 pixels and TV or office system standard compatibility, but with a smaller number of colour for the poly-silicon displays.

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IMEC	*B*	*P*

Start Date	**Duration**	**Status**
01-FEB-89	*60 months*	*Running*

OPTOELECTRONICS WITH ACTIVE ORGANIC MOLECULES

PROJECT NUMBER: 2284

Future optical processing and computing systems will require new materials exhibiting faster and more efficient non-linear optical properties than presently available. The purpose of this project is to exploit the vast potential of organic molecular and polymeric materials for applications such as frequency conversion, parametric amplification and emission, optical bistability, electro-optic modulation, real-time holography and beam steering.

The aim of the project is basically twofold: firstly, it aims at enlarging the exploration of candidate materials for non-linear optical devices. This would allow full advantage to be taken of the virtually unlimited possibilities of modern organic synthesis and require modellisation and synthesis capabilities well represented in the consortium. Secondly, organic molecules are to be adequately shaped into materials, either in bulk or thin film configurations, so as to be further incorporated in devices meeting the specifications of advanced optical information processing systems, both in terms of efficiency (essentially large bandwidth, low attenuation losses, low driving voltage and/or optical pump power) and long term stability.

Two demonstrator devices are expected by the end of the project:

- a waveguide frequency doubler
- electro-optic waveguide modulator.

Beyond these precise goals and in keeping with a growing worldwide trend, this project should contribute to the promotion of a new sector of the European industry, still very much in its infancy, located at the boundaries of the chemical and electronic industries.

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FUNDP	*B*	*P*
CEA/LETI	*F*	*P*

Start Date	**Duration**	**Status**
24-JAN-89	*36 months*	*Running*

OPTICAL INTERCONNECTIONS FOR VLSI AND ELECTRONIC SYSTEMS (OLIVES)

PROJECT NUMBER: 2289

The overall objective of this project is to develop optical interconnections for use between VLSI chips in advanced electronic computer and processor systems which demonstrate significantly improved performance compared with the electrical alternative. The project links four of Europe's leading optical, semiconductor and computer companies with a chemical company and five universities and is aiming towards commercial exploitation in high performance processors from the mid-1990s onwards.

The project focuses on the development, construction and assessment of a set of demonstrators which act as test-beds for two- and three-dimensional optical interconnects. These demonstrators cover the application of optics to both clock and signal distribution at the chip, board and inter-board levels. Of paramount importance in both their initial selection and their realisation is compatibility with electrical technology, so that future systems may make best use of both optics and electronics.

To provide the components required for these demonstrators a significant technological effort will be required in the fields of holography, guided wave components, receiver circuitry and optical modulators. In addition, precision alignment and hybridisation techniques for both the mounting of the optoelectronic components, and the registration of the boards themselves, will be developed.

In view of the present state of the art of monolithic integration of active optical components and silicon circuitry, hybrid optoelectronic integration will be used throughout the demonstrator construction. However, monolithic integration may offer great potential advantages and, hence, in parallel with the demonstrator development, a study of the growth of III-V compounds on silicon will be undertaken. In addition, a small study of polymeric materials for optical modulators is included since these may offer significant advantages over alternative techniques.

In support of these experimental activities a critical assessment of the comparative performance of the optical interconnects and the electrical competition will be undertaken, in systems of interest to the partners. This will aim to provide a realistic assessment of optical interconnections in a variety of systems, which will provide both technical direction and further economic justification for follow-on work.

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AKZO INTL. BV	*NL*	*A*

Start Date	**Duration**	**Status**
01-JAN-89	*36 months*	*Running*

EUROPEAN VANGUARD EFFORTS ON RESEARCH AND ENGINEERING OF SYSTEMS FOR TESTING (EVEREST)

PROJECT NUMBER: 2318

During the last few years, the exploitation of the ever progressing fabrication technologies has resulted in increased complexity in the electronics products and hence an increase in the cost of testing them. In certain areas, this testing can account for up to half of the product cost. This can best be solved by treating the design and test of the new product as part of the same problem.

The EVEREST project aims at providing a consistent environment for checking the testability of products while they are being designed, and for generating the data which will ensure that the designs can be verified before construction and that the fabricated parts can be easily tested for manufacturing faults.

The project will develop a prototype new VLSI Verification Tester and an integrated suite of CAD tools which, if successful, will remove the bottleneck between CAD and CAT environments.

The most important targets are summarised below:

- a verification tester to provide a complete design-to-test solution for VBSs
- a CAE-ATE independent test specification format
- knowledge-based solutions for test planning and failure diagnosis at various levels
- tools for test generation, functional validation, test data analysis, and fault simulation
- design for testability methods for a silicon compiler environment
- integration of all functions in a user-friendly workstation environment.

At the end of the project, the European IT industries will benefit greatly from the availability of low-cost equipment (verification tester) and associated software with the resultant drop in the cost of testing. Furthermore, the products developed according to the proposed methods, using the tools generated in the project, should show less defects and should perform more reliably while remaining no more expensive to test.

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TELEFONICA INV. Y DESARROLLO	*E*	*P*

Start Date	**Duration**	**Status**
01-JAN-89	*48 months*	*Running*

ASIC MULTICHAMBER RAPID THERMAL PROCESSING WITH MICROWAVE ENHANCEMENT

PROJECT NUMBER: 2319

The growing pressure on manufacturers to obtain high yields from their wafer fabrication operations is leading a trend towards single wafer processing. Rapid Thermal Processing (RTP) has come to be viewed as the single wafer alternative to furnace tube processing. The project aims at developing a multichamber RTP machine with improved control of the on-wafer temperature and including novel microwave enhanced techniques for precleaning before oxidation or deposition processes.

The principal technical tasks of this project will involve:

- the identification of the requirement put on RTP for VLSI ASIC
- development of the RTP techniques and processes including precleaning, dielectric and polysilicon deposition
- evaluation of the new multichamber RTP machine in an industrial environment.

Such equipment is expected to give high yields in high temperature processes. Because of its greater flexibility, it is expected to be an important production tool for low-volume and fast-turnaround ASICs.

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STC TECHNOLOGY	*UK*	*P*
SGS-THOMSON	*F*	*P*
UNIV. OF EDINBURGH	*UK*	*P*

Start Date	**Duration**	**Status**
02-JAN-89	*36 months*	*Running*

DEVELOPMENT OF FERROELECTRIC LIQUID CRYSTAL DEVICES FOR INFORMATION TECHNOLOGY APPLICATIONS (FELICITA)

PROJECT NUMBER: 2360

The objective of this project is to develop ferroelectric liquid crystal (FLC) device technology to the point where the devices can go on to be produced competitively within Europe.

The project will concentrate on two types of devices: an A4 display suitable for an office terminal, and a xerographic printhead based on an FLC shutter array. The complexity of these devices will increase through the programme from an A4 monochrome 640 x 400 alphanumeric/graphic display to an A4 colour 1280 x 800 video rate display with 16 grey levels and from a 3-inch shutter array to a 7-inch, 600 dot per inch (dpi), shutter array in a printhead with a line write time of 154 microseconds.

The workpackages cover the areas of fundamental studies, development and evaluation of LC materials, electronics, colour and grey scale technologies, displays and light shutters fabrication technology. The fabrication work should develop the technology to ensure that high quality devices can be produced with high yield. The colour and grey scale workpackages must ensure that the display can compete effectively with other display technologies for the office terminal market. FLC materials should be developed, which enable both the displays and shutters to meet the market requirements for operating speed, temperature range and lifetime. Under the electronics workpackage the ICs needed to drive these complex devices will be designed alongside the development of the addressing schemes. Completed devices will also be built into modules under this workpackage.

Ferroelectric liquid crystals combine the well-known advantages of conventional liquid crystals with the additional advantages of very fast switching and bistable operation. This combination of properties offers the possibility of achieving high contrast, highly multiplexed flat-panel displays operating at videoframe rates. In addition, the technology can obviously be applied to produce high-density fast shutter arrays for use in a xerographic printhead.

The fundamental studies of the chiral smectic C phase and their application to fast flat-panel displays and light shutters, should lay the foundation for future development of FLC effects and ofnew devices with the potential to address new markets in the IT field.

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UNI. MADRID	*E*	*P*

Start Date	Duration	Status
01-FEB-89	*42 months*	*Running*

APPLICATION-SPECIFIC ARCHITECTURE COMPILATION (ASAC)

PROJECT NUMBER: 2394

The ASAC project will explore techniques for the creation of system-level design tools to ensure optimisation of hardware performance and optimisation of the hardware/software partitioning.

The goal of the one year definition phase is to achieve a joint understanding between all partners of system design problems which will form the basis upon which to define the requirements for CAD tools and systems at the system design level.

The final project goals are to develop a set of CAD tools to allow systems designers to:

- specify and design concurrent hardware/software systems
- build explicit models of the environment in which the target system will work
- support top-down methodologies (global architectural design, trade-offs, global performance model, etc.
- support bottom-up methodologies (performance verification, explicit building of system parts, etc).

The results of the ASAC project are to provide a tools bridge between the system design projects, the lower-level CAD tools and semiconductor process development.

The benefits aimed at by the final ASAC project will be:

- To provide a common framework for the exchange of system level CAD tools.
- To reduce lead-times and improve the quality of design decisions through the system design/capture process.
- To reduce the degree of specialisation required to use performance modelling tools, thus making them available to a wider group of designers.
- To improve the effectiveness of the system designers by improving both the tools they have available and the data with which they have to work.

The one year definition phase will produce the optimised plan for the achievement of the final project goals.

This optimised plan will be strengthened by study reports on critical issues identified on the path towards the final project goals.

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SIEMENS A.G.	*D*	*P*
OLIVETTI	*I*	*P*

Start Date	**Duration**	**Status**
01-JAN-89	*12 months*	*Running*

DEVELOPMENT OF A MULTI-CHAMBER BATCH REACTOR FOR THE PRODUCTION OF MULTILAYER INTERPOLY DIELECTRICS

PROJECT NUMBER: 2403

The objective of this project is the development of a multi-chamber batch reactor in which interpoly silicon oxide and silicon nitride films, combined in a so-called ONO configuration, can be produced in one reactor system.

In state-of-the-art devices, interpoly ONO films are implemented in the floating gate structure of EPROM and EEPROM devices. Following the development of higher circuit integration and the corresponding reduction in dielectrics thickness, it appears that the integrity of the interfaces between the various layers will soon become the limiting factor in the electrical performance (electrical defect density, charge retention) of future devices. It is thus important that the dielectric structure is deposited in one vacuum system, preventing the wafers coming into contact with air, before the capacitive structure is completed. In that case, in fact, the resulting uncontrolled growth of native oxide films combined with the exposure of the surfaces to chemical contaminants would lead to the degradation of the interface quality in an unreproducible way, thereby adversely affecting the electrical characteristics of the devices.

The reactor system is to be developed in two phases. In the Mark I (R&D) prototype, only the HF vapour phase pre-clean and the ONO dielectric film deposition are combined. In the second phase, an industry-oriented Mark II system will be manufactured in which the final deposition of the LPCVD polysilicon will take place in the same vacuum system as well.

To confirm the superior electrical characteristics of ONO films grown in such a reactor, state-of-the-art EPROM and EEPROM structures with a dielectric stack of typically 30 nm will be manufactured and tested. The capability to process advanced ONO films with reduced dimensions, i.e. with a dielectrics thickness below 20 nm will also be evaluated. For this purpose, a demonstrator designed in the first phase of the Advanced PROM Building Blocks TIP (project number 2039) and test patterns utilised to develop the demonstrator of the second phase of the same project will be used.

As a result of this project solutions are expected to some of the technological problems that will be met in the manufacturing of 0.3 - 0.5 micron non-volatile memory devices. Furthermore, although this type of reactor will be tested on ONO structures, the proposed system could be used to improve the electrical characteristics of other types of device structures as well. Additional advantages related to the elimination of waiting times in between successive process steps and to the implementation of cassette-to-cassette automation would further increase the industrial potential of this type of equipment.

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Start Date	**Duration**	**Status**
15-NOV-88	*48 months*	*Running*

VERY FAST IMPLEMENTATION OF COMPLEX SYSTEMS ON SILICON (IDPS) - TIP

PROJECT NUMBER: 2426

The project intends to provide the European industry with the basis for a state-of-the-art ASIC facility.

In R&D, existing 1.0 and 0.7 micron CMOS processes will be improved and industrialised in two production lines. One line (VQTA) will provide Very Quick Turnaround Times from design database to tested prototypes. The VQTA line will also produce small production quantities. The other line will offer Quick TurnAround time (QTA) for prototyping with follow-up volume production. The processes in the two lines will be compatible.

Included in the project is the development of two CAD systems - CAD1 and CAD2. CAD1 will be especially suited for EDP systems. CAD2 will be a general-purpose system for eg. telecom, consumer and automotive applications.

All partners will join in the development of a common library of fixed cells, complex blocks, generators and silicon compilation software. Analogue functions will be included as needed for telecom and automotive applications amongst others. Standardisation of views and formats will be part of the task.

Quality assurance will be a specific part of all work packages. In addition, general quality management will guarantee the vertical integration of quality through all elements of IDPS.

To validate (debug) all features of IDPS, the consortium partners will design real applications from the second year onwards when the first library and CAD tools are available.

Also, a number of external companies will be invited to become library associates and use IDPS at an early stage. They will be trained by the consortium and will receive full information on the agreed library standard format. This will enable them to design their own proprietary library blocks and use them along with the IDPS common library.

Library associates will thus help debug IDPS and report on their experience. In return, they will receive all services from the consortium at no cost. A training and support team will interface with the design teams of partners and associates working on applications.

During the first phase of the project (one year) a number of key deliverables are intended to prove the viability of the project. Decision for continuation for four more years will be taken at the end of the first phase.

The complexity of the target circuits (1 million transistors target in the second phase and 2 million in the third phase) requires large improvements in processing, library and CAD. The targets for complexity and turnaround time (in the order of one month for 2 million transistors (logic) circuits) can only be met by integrating the conditions for their achievement into all aspects of IDPS.

At the end of the project the partners of the consortium intend to make the results commercially available. This includes the documentation of library standards and CAD interface standards, the common standard library, the CAD system and access to the ASIC VQTA and QTA production lines.

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MARCONI ELECTRONIC DEVICES	*UK*	*P*
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Start Date	**Duration**	**Status**
01-DEC-88	*12 months*	*Running*

A HIGH PERFORMANCE CMOS-BIPOLAR PROCESS FOR VLSI CIRCUITS (BICMOS)

PROJECT NUMBER: 412/2430

The objective of project 412 has been the development of a VLSI technology combining, on a single chip, MOS circuitry of the highest density currently obtainable with bipolar circuitry of similar density, but better suited to specific tasks, such as analogue interfacing with the external world. The main effort has been on the technological side, in the development of methods which allow both bipolar and MOS transistors to be made in compatible process steps, and in dimensions comparable to those presently obtained in MOS-only technology. In parallel with the technological work, design methods for this specific type of circuit (mixing analogue and digital functions) have been under development along with studies to determine, for various types of application, the most appropriate division of sub-systems between the two circuit technologies.

During the first phase of the project a rather complex process, called BICMOS-1 (1.5 micron emitter width for bipolar devices combined with 1.5-1.2 micron CMOS transistors) has been developed. Application studies of the mixed process have been progressing quickly, resulting in the design of a number of digital and analogue functions. These functions have been first simulated and implemented on silicon in the already developed 2 micron process, BICMOS-0. Besides showing the strengths and weaknesses of the design tools in the analogue field, this has allowed the quantitative evaluation of the advantages of a mixed process over plain CMOS, notably for drivers and analogue functions. Successively, as a first circuit demonstrator, a microprocessor controlled "audio-centre" (of about 20K transistors complexity) has been successfully designed and processed at Philips in both BICMOS-0 and BICMOS-1. At the same time target specifications for the performance of BICMOS-1 (570 MHz for CMOS toggle frequency and 5.2 GHz for bipolar transition frequency) have been met at Siemens.

The work is presently progressing towards the development of BICMOS-2 (1.2 micron feature size in CMOS and 0.9 - 1.2 micron in the bipolar part). This is now being carried out within ESPRIT II Project 2430, which has, as a main objective, in a 3-year time-frame, the development of a more advanced process called BICMOS-3 (0.7 - 0.8 micron design rules). A number of circuits are planned to be designed and processed. Among them, a video A/D converter (of about 200K device complexity) which would not be possible to realise by CMOS only, and a 3K gate array with an on-chip 16k SRAM, both in BICMOS-2, are expected at the end of the first 18 month phase.

In the following 18 months several other demonstrators will be designed and processed including a high performance A/D converter (30K - 50K transistors), a FIR filter, a video A/D converter with added functionality and a fast data path unit (or alternatively a network for packet-switched applications) of 100K transistors complexity .

Fruitful synergy between skilful designs in universities and industrial technologies has been demonstrated and is expected to further strengthen in the continuation of the work.

Concerning the expected cost of such a complex process for volume production, the results to date are promising, since they indicate that the yield of the CMOS process is not affected by the additional process steps needed for bipolar transistor manufacturing. Furthermore some circuits, because of problems in performance and dissipation, cannot be realised in either bipolar or CMOS. Under certain conditions even the gain in area consumption is considerable. The attractiveness of the BICMOS-0 stabilised process is demonstrated as the process is now entering large volume production.

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TRINITY COLLEGE DUBLIN	*IRL*	*A*

Start Date of Project 412	**Duration**	**Status**
01-APR-85	*43.5 months*	*Finished*

Start Date of Project 2430	**Duration**	**Status**
15-NOV-88	*36 months*	*Running*

INDUSTRIAL CHARACTERISATION OF AN ADVANCED RESONANT ETCHER (ICARE)

PROJECT NUMBER: 2437

The goal of this project is the development and evaluation in an industrial environment of two industrial prototype etchers capable of producing the new generation of Ultra Large Scale Integration (ULSI) devices.

The project aims at the development of a new generation of etcher equipment based upon the use of two new reactor concepts, both operating with resonant coupling: the Resonant Inductive Plasma Etching (RIPE) and the Distributed Electron Cyclotron Resonance (DECR). The main characteristics of these reactors are:

- total independence of parameters controlling the plasma generation and those controlling its interaction with the surface to be processed
- low pressure
- large volume of quiescent homogeneous high density plasma
- no internal active electrode
- capability of processing large diameter wafers
- simplicity of realisation.

Three types of etching processes specific to Ultra Large Scale Integration (ULSI) technology will be developed to support this project: trench etching for isolation, contact and via etching, and fine-line polysilicon etching on thin gate oxide.

Demonstration will be made on 0.3 micron patterns.

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Start Date	**Duration**	**Status**
01-JAN-89	*36 months*	*Running*

RESEARCH INTO BOUNDARY SCAN TEST IMPLEMENTATION

PROJECT NUMBER: 2478

The testing of digital printed circuit boards (PCB) is going through a serious crisis caused by the increasing complexity of the integrated circuits which they contain. This complexity results in a very high cost for conventional electronic testing. About 40% of the total cost of the products comes from testing. The increases in complexity expected in the next few years will make test costs prohibitive, unless radical methods are used to improve these test techniques. "Boundary Scan Test" is one such method. Its effectiveness depends on adherence to standard test methods for components. A new standard, JTAG, promoted by the project partners, and about to become an international standard, forms the basis for this project.

The aim of the project is to provide the industry with the basic knowledge, tools and experience to incorporate Boundary Scan Test into their designs, and to interface with existing test equipment. The incorporation of another promising test strategy, "Built-in Self Test (BIST)", into the Boundary Scan method will also be investigated. The project will also entail, in the long term, the use of expert systems for test generation and diagnosis. Other activities will result in BST implementation tools on CAE and test equipment, and the development of an interface layer between these tools. A demonstrator board using the tools and components realised within the project will be specified, designed and built to check the performance of the BST implementation. Methods of minimising costs will be investigated.

The project will give European industry the knowledge and tools it needs to be early in the market with products incorporating the new standard, thus giving it a competitive edge.

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Start Date	**Duration**	**Status**
01-JAN-89	*36 months*	*Running*

WAFER AND EPILAYER IMPROVEMENT CORRELATED WITH DEVICE PERFORMANCES FOR INP-BASED OPTOELECTRONICS

PROJECT NUMBER: 2518

This project is a continuation for one year of the completed Esprit project 927.

On December 1988, during the course of project 927, the growth of high quality ternary GaInAs layers on semi-insulating InP has been demonstrated. The main objective of the present project is to demonstrate the reproducibility of MOCVD equipments and growth processes for ternary and quaternary epilayers (GaInAs and GaInAsP) suitable for optoelectronic integration.

The problem of growing 2" InP wafers and epilayers with uniform characteristics will be addressed. In order to test the substrate and the epilayer homogeneity, scanning photoluminescence and ellipsometry will be used.

The influence of the wafer defects and uniformity on the devices electrical performances will be studied on GaInAs MISFETs. The dynamic potential of the MISFET technology will be tested with high frequency/digital characterisation of discrete devices and ring oscillator circuits.

For the quaternary layers, which can be used in optical circuits, the transparency of the material in guided wave configuration is the most important parameter. This is critically dependent upon the wafer electrical quality, i.e. the doping level and the compensation ratio. The quaternary transparency will be tested using a simple channel waveguide structure, and the results will be correlated with the photoluminescence results.

The development of reproductible growth of InP substrates and InP-based multilayer structures undertaken in this project is a prerequisite to any further development of compound semiconductor ICs and is expected to enhance the industrial competitiveness of the partners in the field of MOCVD-equipment and InP-wafer fabrication.

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Start Date	Duration	Status
01-JAN-89	*12 months*	*Running*

MAGNETIC MEDIA FOR FUTURE ULTRA HIGH DENSITY INFORMATION STORAGE

PROJECT NUMBER: 2633

Magnetic tapes, especially for helical scan recording, are and will remain (for at least the next ten years according to market surveys) the information media offering the highest volume storage density, even when compared with optical discs. According to the present state of the art (streamers), the maximum volume storage density of these media is around 2×10^7 fc/mm^3. This density is, for the time being, suitable for digital home audio and for the corresponding data storage system (R-DAT).

Nevertheless, the emergence of new demands from the computer industry (for back-up) and from the consumer market (HDTV recorders, for instance) requires an tremendous increase in the volume storage density of tape media. The use of tape-recorders, coupled with buffer memories to reduce the inconvenience of long access time, remains the best way to achieve very high rates of transfer of huge amounts of data.

This new market requirement may be fulfilled by optical technologies, but magnetic tape represent the quickest answer to market demands, provided that some drawbacks of the present technology can be overcome.

The objective of the project is to develop a high resolution medium which offers an increase in volume storage density up to a factor of 4 and a reduced error rate with respect to the present state of the art. Manufacturing steps and components will be improved to achieve:

- tape substrates with lower thickness and improved quality with regard to dimensional stability, adhesion properties, surface smoothness and abrasivity (reduction of head-wear);
- magnetic coatings with lower particle sizes and higher homogeneity as well as an outstanding level of internal cleanliness.

The introduction of completely new processing technologies (like surface treatments) and the use of modern physical analytical methods (like surface spectroscopy) will be necessary steps for successful work.

Then the resulting tape should make it possible:

- to record HDTV video information with a transmission rate of about 100 Mb/s
- to increase volume storage density by about two orders of magnitude compared with present media, based on conventional oxide pigments.

The project represents an important complementary element to the corresponding hardware RACE project (DVT 1001) focusing on digital video recording systems, and the final tape will be a part of every highly sophisticated future system of digital recording for computer and video applications. From that point of view the improved magnetic tape, resulting from this project, will enable the European industry to maintain and to strengthen its position on the worldwide market.

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Start Date	**Duration**	**Status**
01-JAN-89	*48 Months*	*Running*

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