Esprit

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The Project Synopses

Advanced Microelectronics

Volume 2 of a series of 7

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The Project Synopses

Advanced Microelectronics

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LEGEND

Countries

Code	Country
B	Belgium
D	Federal Republic of Germany
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E	Spain
F	France
GR	Greece
I	Italy
IRL	Ireland
L	Luxembourg
NL	The Netherlands
P	Portugal
UK	United Kingdom

Roles

Code	Role
M	Main Contractor
P	Partner
S	Sub-contractor

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PROJECTS WITHOUT ACRONYMS CAN BE FOUND IN THE MAIN INDEX

ADVANCED MICROELECTRONICS

Introduction

Advanced Microelectronics in the context of this subprogramme, encompasses all research and development aspects concerning the provision of the physical elements for the acquisition, processing, storage, transmission and display of data required by modern informatic products. It is therefore the hardware foundation of the Information Technology (IT) industry.

This subprogramme concentrates on the priority areas needed to ensure that Europe maintains a competitive position regarding the supply of these essential ingredients for her IT manufacturing industry with the required capability, in sufficient quantity and at competitive prices.

OVERVIEW OF THE SUBPROGRAMME AREAS

The major thrust of the research and development programmes within Microelectronics is to push the silicon based technologies of MOS and Bipolar towards their limits of capabilities whilst pursuing the possibilities afforded by the compound semiconductor materials, such a Gallium Arsenide, which have potential capabilities in key areas beyond those possible using silicon.

Apart from a capability to produce high function count chips, it is also necessary to deal with the problems posed by the complexity of their design. Managing this design complexity effectively is the main goal of the work on Computer Aided Design (CAD) of VLSI Systems.

Optoelectronic devices offer many possibilities especially in the data transmission field, these will be investigated.

An investigation of advanced display technologies offers the possibility of replacing the ubiquitous CRT, as the main vehicle for large scale display, by more compact solid state based counterparts.

Research themes which are more innovative or longer term than those contained in the first six topic areas as well as critical areas of technology and techniques with a common thread are brought together under the heading of General Supporting Topics. These include packaging, device modelling and special processing materials and techniques.

SUBMICRON MOS

The requirement is to develop all the individual process steps to achieve submicron feature size in MOS (such as lithography, etching and doping). The target is a process capable of making several million components of logic and memory per chip. It is envisaged that below about 0.7 um tools other than

optical lithography will be used. Process and device modelling will be included.

The main objectives of the broad 5-year programme are :

- At 18 months: design and evaluation of test vehicle of more than 1000 transistors based on 1 um design rules with a pitch (metal plus spacing) of 3 um.
- At 3 years: first samples of demonstration circuit with 0.5 million transistors, 1 um design rules, with data on figure of merit and delay time.
- At 4 years: statistical data on homogeneity on a slice and yield for 1 um design rules; and test vehicle with more than 1000 transistors with 0.7 um design rules and a pitch of 2 um.
- At 5 years: first samples of circuits with more than 1 million transistors, 0.7 um design rules, with data on figure of merit and delay time.

SUBMICRON BIPOLAR

The overall objective is to develop specific bipolar submicron process steps, leading to a complete processing sequence for very high performance ICs.

To realize this objective the following developments are included in the project area:

- Overall circuit concepts which must evolve together with the technology.
- A vertical device structure appropriate to submicron lithography.
- A convenient multilayer interconnection technology.
- A suitable contact and multilayer interconnection technology.
- Appropriate high dissipation, high pin count, electrically matched leads, packages.
- Process and device modelling.

The critical techniques needed to support the submicron MOS and bipolar areas are covered in area of general supporting topics.

The main objectives of the programme over 5 years are :

- At 1 year: Initial process design; evaluation and choice of critical equipment.
- At 2 years: Establish final design rules at 1 um.

- At 3 years: Demonstrate 1 um 10/20K gates, 100 ps gate delay circuits.
- At 4 years: Establish final design rules for 0.7 um structures.
- At 5 years: Availability of first samples of 20/50K gate circuits in 0.7 um process.

COMPUTER AIDED DESIGN (CAD)

The two primary objectives are :

(a) To develop advanced CAD techniques to manage the ever increasing circuit complexities within microelectronics.

(b) To provide a capability for complex VLSI design which is widely accessible to the EEC IT community.

The overall aim is to develop within a common framework an integrated set of portable tools capable of handling VLSI circuits containing up to several million components. This set of tools should :

- Provide a fast response, user friendly design facility that is readily adaptable to changes in technology.
- Allow designers to achieve a rapid turnaround of valid and testable designs and associated test information.
- Provide facilities for reliability and performance optimisation of circuits.
- Include methodologies of cell-based design and libraries of adaptable building blocks.
- Assimilate relevant results of CAD projects under microelectronics regulation (EEC) 3744/81.

The strategy for this R & D area is that:

(a) A positive attempt should be made to encourage the emergence of an overall CAD infrastructure such that the majority of tools developed under existing programmes together with future tools can be combined to provide an integrated widely accessible tool capability.

(b) As far as possible, complex demonstrator chips will be used as a focus for each stage of the programme.

(c) Device and process modelling is not considered as part of the CAD projects but is included in the projects concerned with the development of new VLSI processes however compatibility with CAD is required.

(d) Care should be taken to promote cooperative development between

universities, industrial groups and research institutions in order to transfer know-how and make CAD available to a broader community.

(e) Care will be taken to interface with, support and employ the results of other ESPRIT activities.

(f) The application of knowledge engineering techniques to CAD should be emphasised.

(g) Dedicated CAD hardware should be incorporated where appropriate.

(h) There is a vital need to incorporate the results of current European projects which are in most cases difficult to quantify.

COMPOUND SEMICONDUCTOR INTEGRATED CIRCUITS

Integrated digital circuits in III-V compound semiconductor materials offer potential speed and/or speed/power product advantages over silicon circuits because of higher electron mobility. The degree of understanding of the technological complexity of these materials is less advanced than for silicon and considerable materials and process research is necessary. Because of the increasing market for high-speed, low-power circuits, many problems need to be tackled in order to bring forward knowledge in this area.

The technology encompasses GaAs circuits based on field effect transistors (FET's) as well as GaAs/GaAlAs heterojunction structures using high electron mobility transistors (HEMT) or the heterojunction bipolar transistors (HJBT's). Basic research is required in materials preparation, ion implantation, and IC process technologies.

The specific objectives of this programme are:

- At 1 year: Demonstrate feasibility of MESFET based circuits with 1000 gates and gate delay (tpd) of less than 100 ps. Also, demonstrate basic HJBT and/or HEMT circuits (other than ring oscillators).

- At 2 years: Demonstrate at least 1K memory (less than 1 ns access time, less than 500 mW dissipation) and/or equivalent complexity circuits.and demonstrate feasibility of 100 gates HEMT and/or HJBT circuits.

- At 3 years: Evaluate yield on a demonstrator circuit of 1K or equivalent complexity, on at least 10 wafers. Demonstrate feasibility of 1K HEMT memory and /or comparable HJBT circuit. Comparison of various technologies (if possible with the same circuit for each technology). Decision for selecting one out of them.

- At 4 years: Demonstrate 16K memory (or equivalent) in the selected technology.

- At 5 years: Demonstrate large circuit of 10 to 20K gates complexity, gate

delay of less than 50 ps with figure of merit less than 100 femtojoules. This demonstrator could be a 16K memory with an access time in the order of few nanoseconds or it could be defined during year 3 to fulfil needs of other ESPRIT areas (especially high speed data bus) or of telecommunication industry (signal processing circuits for instance).

OPTOELECTRONICS

Optoelectronic devices will be increasingly required for telecommunication type transmission ultra wide band image processing and switching. Future generations of mono-mode communications systems may use coherent detection and multi-channel wavelength multiplexing and may be phase modulated. This will provide improved performance and be compatible with integrated optical logic. It will allow processing, combining and routing at very high speeds. In semiconductor form it will also be compatible with III-V integrated circuits, providing a fast electrical interface. This programme is not aimed at optically-based computers, but rather at providing components and subsystems for large bit rate transmissions.

The total achievement of the objectives of this programme needs very large resources which may not be available within the framework of ESPRIT. On the other hand these objectives represent a minimum target to remain globally competitive.

The objectives are as follows:

(a) Integrated electronic and optical components on the same chip:

At 1 year: Demonstrate a monolithic photodetector with internal amplification.

At 2 years:Demonstrate a monolithically integrated receiver with bandwidth greater than or equal to 2.5 GHz.

At 3 years: Demonstrate an integrated transmitter with a bandwidth greater than 2.5 GHz.

After year 3, further optimisations of receiver, transmitter, and perhaps also repeaters have to take into account the progress and needs of the telecommunications industry and of the other ESPRIT areas.

(b) Wavelength multiplexing (WDM) with integrated optics:

At 1 year: Demonstration of DFB laser with threshold current lower than 50 mA; demonstration of waveguide fed photodetector; low loss monolithic waveguide (smaller than 1dB/cm).

At 2 years: Demonstration of 2.5 GHz bandwidth modulators in semiconductors.

At 3 years: Demonstrate an integrated transmitter with a bandwidth greater than 2.5 GHz.

At 4 years: Demonstrate integrated WDM transmitter and receiver modules.

At this point, some inputs from other ESPRIT areas and telecommunications industry are needed to implement a demonstration link at a several gigabit rate.

ADVANCED DISPLAY TECHNOLOGIES

In many product areas, eg workstations, electronic office equipment etc. there is an urgent need in Europe for new advanced display systems to replace and supercede the conventional CRT. Such displays would need to be of large size (A4 and above) and of medium to high definition. Colour capability would also be desirable/necessary.

Many approaches are currently being investigated. A technology definition effort in which major existing community practitioners would combine their knowledge and experience is required to define within a short time period the most adequate way to tackle this problem.

GENERAL SUPPORTING TOPICS

This area covers :

(a) Research themes not already identified in the previous microelectronics areas.

(b) Topics which support one or more of the other areas.

(c) Research themes which look forward beyond the early stages of the microelectronics programme towards the submicron goals.

HIGH LEVEL CAD FOR INTERACTIVE LAYOUT AND DESIGN

Project number : 10

The objective was to define and demonstrate a CAD system for the Design and Layout of VLSI integrated circuits from the initial specification to the masks. Circuit complexities of up to 1 million transistors were to be addressed. Reduced design times were the overall aim. The main topics under investigation included high level design methodology based on Petri nets, hierarchic floorplanning with a high degree of automation, analogue and general cell design, data modelling and data base management.

The project ended in March 1987.

A prototype system has been produced which allows a specification expressed as a Petri Net (type of flowgraph) as input and produces mask tapes as output.

- It incorporates a design methodology for analog cells which has circuit performance optimization properties.

- This system features a sophisticated interface to the circuit level simulation package and is technology-independent in its application. Tests of this system demonstrated its efficiency. The work on design rule independent description of cells has been completed. A translation procedure from a physical into a symbolic description of cells and back into a different physical representation has been described. The elaborated method has been applied to both NMOS, CMOS and bipolar circuit examples.

- Another major accomplishment was the verification of the operation of a multi-cache bus system by proving the correctness of the marking graph of its model. This model was described by means of high level Petri nets (RTPN) and proved by using a methodology that permits a fast formal verification in place of the more usual slow simulation. Unfolding of the RTPN to an ordinary Petri net then leads to a correct and easy (one to one) hardware synthesis.

- The final revision of the design manual of 200 pages in length has been carried out entitled: "Design of digital systems using Petri nets". It contains all the important results on the design methodology.

- The data requirements of each tool of the CAD system have been defined. A data model, which is adequate for the relational DBMS of the design system, has been established in a close liaison between the project partners. A graphic representation, which shows both how the attributes are associated to the relations and the access mechanism has been established.

- Software for placement of general cells has been developed. It is based

on constructive initial placement, using a mixture of rules and algorithms. A simulated annealing placement improver has also been developed. This software has been tested in a variety of technologies. The software has been integrated with the Oracle (tm) Data Base Management System on Apollo workstations, and with the PLESSEY MEGACELL (tm) Data Base Management System on DEC VAX. Studies have been made of the impact on future placement software on the power routing and hierarchy problems anticipated in future generations of technology.

Overall, the project has achieved its stated objectives in terms of the design and production of a CAD design. Its performance, however, has not been validated.

The feasibility of describing systems using the Petri Net notation and the description being automatically translated into circuits and layout has been demonstrated. This translation can substantially reduce the design time for complex chips.

The analogue work carried out has also made a valuable contribution to the state-of-the-art knowledge in this area especially as analogue in combination with digital functions on the same chip is gaining in importance.

Contact Point

Mr G. BOWN
GEC RESEARCH LABORATORIES
East Lane
Wembley
UK - HA9 7PP MIDDLESEX

Tel: +44-1-908 92 56
Tlx: 923429
Fax: +44-1-904 75 82

Participants	**Country**	**Role**
GEC RESEARCH LABORATORIES	*UK*	*M*
AEG A.G.	*D*	*P*
BULL S.A.	*F*	*P*
PLESSEY COMPANY PLC	*UK*	*P*

Start Date: *01-10-83*

Duration: *42 months*

ADVANCED INTERCONNECT FOR VLSI

Project number : 14

The objective of this programme was to develop high density interconnect compatible with one micron MOS and Bipolar VLSI technologies. This interconnect technology was to feature four levels of low resistivity metal interconnect with high electromigration resistance and stable, low resistance contacts to the underlying silicon circuit. The main milestones of the programme were :

- Demonstration of 3-layer metal at 5 um pitch in September 1986.

- Demonstration of 4-layer metal at 3 um pitch in December 1987.

The project finished in December 1987 but the final report is not yet available.

The first main milestone was reached on time and several variants of the developed structures for non nested vias and pillars were evaluated by means of the final test mask towards the final milestone.

However, a major technical difficulty was encountered while setting up the final process. Although good progress had been made with optimised aluminium for step coverage, it was discovered that these conditions did not fill small holes such as contacts and vias. The work was therefore restructured and new sub-tasks added in order to reach the final milestone with a 3 months delay.

Parallel work on contact systems has been completed, and tests on the reliability of polyimide and nitride has produced very good results.

All the partners intend to make use of the developed interconnect in their CMOS or bipolar processes. Plessey has notably transferred the 3 layer metallisation scheme to its CMOS process and will use the developed techniques to realize the final demonstrator of the Alvey C-MOS project.

Contact Point

Mr R.OAKLEY
PLESSEY COMPANY PLC
Allen Clark Research Centre — *Tel: +44-327-50 581*
Caswell - Towcester — *Tlx: 31572*
UK - NN12 8EQ NORTHANTS — *Fax: +44-327-534 10*

Participants	**Country**	**Role**
PLESSEY COMPANY PLC	*UK*	*M*
GEC RESEARCH LABORATORIES	*UK*	*P*
TELEFUNKEN ELECTRONIC GMBH	*D*	*P*
THOMSON CSF/DCI	*F*	*P*

Start Date: 06-09-84 *Duration: 36 months*

ADVANCED ALGORITHMS, ARCHITECTURE AND LAYOUT TECHNIQUES FOR VLSI DEDICATED DSP CHIPS

Project number : 97

The objectives are:

- To produce a set of methods, algorithms and CAD tools for the design of digital signal processing chips in state of the art CMOS technology using new advanced optimised circuit techniques and clocking schemes.

- To produce tools to support formal as well as interactive design from specifications down to chip layout. The CAD tools so produced should be capable of optimising chip area and power dissipation for given system requirements.

Design methodologies and the appropriate design tools for several specific digital signal processing architectures are to be developed. The architectures are:

- Bit-serial

- Hardwired Bit-parallel

- Regular (systolic) array architectures

- Bit-parallel customisable multi-processor architectures.

The objectives for bit-serial architecture were met during the first half of the project. This has been achieved via the CATHEDRAL-I environment which is now being used by some of the partners. Efforts are proceeding to consolidate and professionalize the results obtained in this area.

Most of the recent effort has been put in the customisable multi-processor architecture. This CATHEDRAL-II system has already been mentioned in a lot of international publications. A prototype version, which has been implemented this year, was successfully demonstrated at the ESPRIT Conference 1987 in Brussels, in combination with the promising results concerning verification and structural procedural interface (SPI) of the ESPRIT 1058 project. A fine tuning of this system and an evaluation by the partners is planned. Philips, however, is already developing the CATHEDRAL-II system further within their company outside the ESPRIT 97 project.

In the area of hardwired bit-parallel datapaths, work is proceeding at IMEC in cooperation with Siemens. A first prototype of the silicon compiler CATHEDRAL-III has been implemented. Siemens is also doing some further investigations concerning the use of regular array architectures in the area of image processing.

Other important results which occurred recently were the realization of the

first prototype of the floor-planner and general cell layout system by Silvar Lisco and the redirection of the work of BTMC towards the synthesis tools (namely the generation and scheduling of microcode).

The results of ESPRIT 97 are proceeding better than originally planned. It will lead to a variety of implemented design methodologies in the area of digital signal processing resulting in faster, more performant chip production. At the moment the main effort is in audio and telecommunication applications, whilst some promising work in more performant video applications has already started. The realizations of the prototypes CATHEDRAL-II and in the near future CATHEDRAL-III are a very important step forward towards these goals.

Contact Point

Prof.DE MAN
IMEC V.Z.W
Kapeldreef 75
B - 3030 LEUVEN-HEVERLEE

Tel: +32-16-28 12 01
Tlx: 26152
Fax: +32-16-22 94 00

Participants	**Country**	**Role**
IMEC V.Z.W.	*B*	*M*
BELL TELEPHONE MFG. CO.	*B*	*P*
PHILIPS GLOEILAMPENFABRIEKEN	*NL*	*P*
RUHR UNIVERSITAT BOCHUM	*D*	*P*
SIEMENS AG	*D*	*P*
SILVAR-LISCO N.V.	*B*	*P*

Start Date: 01-09-83

Duration: 60 months

SUBMICRON BIPOLAR TECHNOLOGY I

Project number : 243

The overall objective of this programme is to develop specific bipolar submicron technology suitable for manufacturing very high performance integrated circuits, such as high speed circuits for Electronic Data Processing (EDP) and Digital Signal Processing (DSP).
Two main milestones are scheduled:

- End of year 3 (March 1988) ; demonstration of a gate delay capability of 100ps at a complexity level of 10 Kgates.

- End of year 5 (March 1990) ; demonstration of a gate delay capability of 50ps at a complexity level greater than 20 Kgates.

After year 1, two new research tasks were added to complement the work programme:

- Development work and processing schemes for sidewall base contact structures, providing very low base access resistance and enabling a good symetric performance of the transistor.

- Research and development of high performance polymers for insulation between metallic interconnection layers in a submicron technology. These performant polymers would be polyimide based resins.

At the half way stage, one micron technology has been set up and the final sequence of the process and first test mask completed. A first run of wafers was carried out. The measured performances are very satisfactory and consistent with device simulations and expected performances required for the first demonstration.

Twenty-one stage ring oscillators have shown that propagation delay times (Tp) lower than 100pS are reached and that a good figure of merit (power product x gate delay) of less than 100 fj is obtained for Tp = 115 pS.

The design of the first demonstrator circuit for the 1 micron technology is completed and first lots are being processed. Regarding the beginning of submicron studies, an objective sequence of a double poly self-aligned emitter base structure has been worked out. A second test mask with various emitter pattern and basic circuit elements has been designed.

Three of the partners intend to implement the developed technologies progressively following the achievement of the major milestones in 1988 and 1990. Likely applications are:

- Gate Arrays and Programmable ROM.

- Micro-cells for DSP ASICs and High Speed A/D-D/A converters.

- Very high speed ASICs for high bit rate telecommunications.

Contact Point

Mr M.DEPEY
THOMSON CSF/DCI
Centre St. Egrève
F - 38120 St. EGREVE

Tel: +33-76 58 30 49
Tlx: 204780
Fax: +33-76 58 30 00

Participants	**Country**	**Role**
THOMSON CSF/DCI	*F*	*M*
PLESSEY COMPANY PLC	*UK*	*P*
TELEFUNKEN ELECTRONIC GMBH	*D*	*P*
TECHNISCHE UNIVERSITAT BERLIN	*D*	*P*
THOMSON CSF/LCR	*F*	*P*

Start Date: 01-03-85 *Duration: 60 months*

SOI MATERIALS AND PROCESSING TOWARDS 3-D INTEGRATION

Project number : 245

The objective was to investigate new silicon technologies suitable for three-dimensional (3-D) integration in order to achieve the possibility of higher density integration, higher speed of operation and multi-functional signal processing. Three main technological steps were explored:

- The growth of SOI active layers having electronic properties needed for the realisation of high quality devices and circuits;
- The stacking of two active levels in a way that avoids any degradation of already built devices;
- The single level SOI processing for the fabrication of individual components and for their connection; also the development of a process incorporating two active layers.

The project finished in December 1987 but final reports have not yet been received.

The first two years experimental work demonstrated the capacity to fabricate mono-crystalline SOI layers compatible with the underlying bulk silicon layers and with limited influence of the first device level on the SOI characteristics. Specifically:

- An industrial E-beam equipment was built for SOI preparation and two different Research Laser Systems were optimised.
- Unified test structures and characterization methods were adopted for quantitative comparison of the crystallization techniques of E-Beam, Laser Zone Melting and CVD epitaxy.

In parallel, design options and product application studies showed two choices for 3-D circuits:

- Conventional applications (high density-high performance VLSI);
- System applications (specialized superimposed layers; performance independence of different functions).

One major conclusion of the application study was that 3-D SOI CMOS for VLSI is unlikely to provide sufficient benefit, in terms of packing density and circuit speed, to compete with single level technologies using bulk or SOI substrates. In contrast, the development of silicon technologies where devices of different types (e.g. CMOS, bipolar and power transistors) can be fabricated on a single chip, was demonstrated as an important application area for 3-D SOI. Such mixed technologies are difficult to produce in a single level of silicon as the requirements of the different device types

often conflict. However, using a 3-D SOI approach, the development of a mixed technology with individual optimisation of the separate device levels can be envisaged.

In the light of these findings, the orientation of the current project and the end of year 3 demonstrator has been focused on the development of a "smart power" technology using a 3 um CMOS SOI level to control medium current/voltage (1A/50V) LDMOS bulk transistors. The particular application considered is a stepper motor controller using a gate array design approach for both the CMOS and LDMOS levels. At this stage, a 'mezzanine' layout has been adopted where the SOI devices are displaced laterally from the underlying bulk devices.

On the materials development side, significant improvements in the SOI starting material, especially the use of selective epitaxial growth of silicon in the seed windows, together with refinements of the laser and electron beam re-crystallisation systems have allowed the production of device grade SOI compatible with the requirements of the end of project demonstrator. High quality SOI devices have been produced and fine geometry bulk CMOS devices which had undergone SOI re-crystallisation under similar conditions were found to be essentially unaffected by the process. These device results confirm the viability of the demonstrator production technique. Full demonstrator device batches were processed in December 1987.

The chosen SOI technique combined with the results of the design and layer processing studies were used to demonstrate 3-D integration. A representative MSI test circuit has been designed, fabricated and tested. In parallel with this, both a refractory interconnection capability and the ability to realise 1 micron devices in the SOI layer have been assessed.

The chosen demonstrator is a first step towards the integration of very different functions on the same chip in a way which allows the independent optimisation of each one and their complete dielectric isolation, thus opening the route for complex system integration on chips allowing more reliability and better performances.

Contact Point

Mr M.MONTIER
THOMSON-EFCIS — *Tel: +33-76 49 36 00*
17 Av. des Martyrs — *Tlx: 320226*
F - 38019 GRENOBLE CEDEX — *Fax: +33-76 49 36 47*

Participants	**Country**	**Role**
THOMSON-EFCIS	*F*	*M*
CNET	*F*	*P*
GEC RESEARCH LABORATORIES	*UK*	*P*
CEA/LETI	*F*	*S*

UNIVERSITY COLLEGE CORK	*IRL*	*S*
UNIVERSITY OF CAMBRIDGE	*UK*	*S*

Start Date: 01-01-85 *Duration: 60 months*

CAD METHODS FOR ANALOG GaAs MONOLITHIC IC'S

Project number : 255

The final objective is to make available a comprehensive CAD package, named MMIC-CAD, suitable for the design of GaAs ICs operating up to 18 GHz. The package will utilise the development of a full CAD library of theoretical models and experimental data for passive elements and active components required for the design of GaAs analog ICs.

The work starts by deriving physical models and equivalent circuits for different types of MESFET and passive elements both for lumped and distributed approaches. The next step is the CAD of groups of passive and active devices for the integrated implementation of elementary functions. Here, besides circuit analysis, coupling between adjacent elements and thermal distribution will also be simulated. In the successive phase, analog ICs, defined as high level functional blocks, have to be considered with special analysis programs. The final CAD program will include package effect evaluation and error-sensitivity analysis. Interactive optimisation will be organised in a user-oriented, transferable package.

The initial C and X-band investigation will be extended to 18 GHz. The CAD capability will be proven with different GaAs IC demonstrators, including submicron dimension devices.

After the first two years, the work was considered to be on target and generally in line with the original objectives.

However, following a major review and in the light of updated requirements for activity in this area, the work programme was re-organised towards a more focussed final objective.

The required negotiations have undoubtedly introduced some delays but the new work plan is geared towards achieving the final objective within the originally planned time-scale. Work is continuing according to the revised work plan and a further review is scheduled in the first quarter of 1988.

The results of this project are expected to have an impact on a small but potentially highly important application area, that of high frequency telecommunications. They will be available for possible exploitation in 1989.

Contact Point

Dr S.IANNAZZO
TELETTRA S.P.A
Via Trento 30
I - 20059 VIMERCATE

Tel: +39-39-6655 683
Tlx: 330630
Fax: +39-39-68 14 83

Participants	Country	Role
TELETTRA S.P.A	*I*	*M*
CISE S.P.A.	*I*	*P*
SIEMENS AG	*D*	*P*

Start Date: 20-12-84 *Duration: 48 months*

INTEGRATED OPTO-ELECTRONICS ON InP

Project number : 263

The general objective is to significantly increase the data rate in optical transmission systems, by the use of high performance devices with a variety of multiplexing techniques, mainly with the use of different wavelengths.

In the first three years, activity is focussed on achieving and utilising single mode discrete functions suitable for subsequent hybrid and monolithic integration. Full hybrid integration will be worked on in years three and four, followed by monolithic integration of some important functions in year five, e.g. an integrated light source with independent control of both output power and wavelength using electro-optic effect and/or current injection to tune a distributed feedback (DFB) laser.

The work on materials will be oriented towards reproducible growth of high quality, high homogeneity, large area heterostructures suitable for low threshold current density and well-controlled wavelength lasers for low doped photo-detectors and low loss waveguides.

The second part of this programme is aimed at the development of the technology needed for the fabrication of the electronic devices in a form which can be integrated with the optical devices. A range of devices will be investigated and compared. As a result of the importance of longer wavelength operations, all this work will be based on InP-based semiconductor compounds. An important additional potential benefit of the project is that these materials are also expected to yield very high performance in purely electronic applications. Thus the programme may lead to improved electronic functions as well as sophisticated opto-electronic circuits.

The first integrated structure, a DFB laser with a tuning section has been realized. Good control on laser manufacturing has been demonstrated (threshold current density < 1.5 $kA.cm^{-2}$, wavelength dispersion < 3 nm). Finite element techniques have been integrated into user-friendly packages to model optical integrated optic devices realistically, easily and precisely. These techniques have been applied to :

- The design of an optical demultiplexer.
- The evaluation of the guiding properties of the very low loss structure (0.04 dB/cm), previously demonstrated.

This is forging a strong link between the modelling and fabrication partners. The first results have been obtained on operating integrated receiver circuits. The sensitivity of an IC consisting an InGaAs PIN detector with a diffused JFET has been measured (-33 dBm at 140 Mbit/s). This is an encouraging result but integration has proved to be more difficult than originally expected indicating that developing such a technology is at least as demanding as developing each individual component. Consequently, some

delays have occurred in this specific task.

The capability to produce state of art discrete opto-electronic components, and especially lasers for high bit rate telecommunications has been demonstrated. Limitations found in InP based active device performances have triggered the start of a new project (Esprit project number 927) to notably improve the substrate quality.

This project, in debugging the opto-electronic monolithic integration which has been found more difficult to achieve than forecasted, is playing a pilot role in a wide range of projects, dealing with low cost optical systems, in the RACE programme.

Contact Point

Dr V.GHERGIA
CSELT S.P.A.
Via Reiss Romoli 274
I - 10148 TORINO

Tel: +39-11-216 93 01
Tlx: 220539
Fax: +39-11-216 95 20

Participants	**Country**	**Role**
CSELT S.P.A.	*I*	*M*
THOMSON CSF/LCR	*F*	*P*
CGE. LAB DE MARCOUSSIS	*F*	*P*
CNET	*F*	*P*
GEC RESEARCH LABORATORIES.	*UK*	*P*
HEINRICH-HERTZ INSTITUT	*D*	*P*
STANDARD ELEKTRIK LORENZ AG	*D*	*P*
STC TECHNOLOGY LTD	*UK*	*P*

Start Date: 15-12-84

Duration: 60 months

AUTOMATIC DESIGN VALIDATION OF INTEGRATED CIRCUITS USING E-BEAM (ADVICE)

Project number : 271

The objective is to produce a prototype system capable of automatically carrying out error diagnosis of VLSI devices. The chosen approach is to be based on utilizing the observability facilities of E-beam equipment. In order to achieve the objectives, the following programme is to be carried out:

- Interfacing to CAD software
- Pattern recognition for automatically positioning the E-beam
- The development of a global methodology to define the diagnostic strategy
- Development of new hardware for enhancement of E-beam performances.

Furthermore the following problems will need to be solved:

- Computer control of the E-beam system
- Identification of circuit elements
- Test pattern generation for electron beam debugging
- Design for electron beam test-ability
- Electron beam equipment development.

Following the completion of the first phase of the project which included the definition and preliminary investigation of all aspects for the design of a fully computer controlled E-beam testing system, the three industrial partners have installed at their premises core systems that are now fully operational.
Some of the key features already included in the core systems are:

- Interfaces between CAD and E-beam systems
- Pattern Recognition
- Hardware and software for computer control.

The results up until now satisfy all the realistic goals set at the beginning and following the first phase. These results are at least state-of-the-art as exemplified at the various presentations and demonstrations given by the partners.

The E-beam design validation and testing technique is a new and very promising one. Its impact and time horizon for industrial applications

depends strongly on the refinement of this or other competing techniques (e.g. scan design) that may emerge. Complete system is expected to be available by the end of 1989.

Contact Point

Dr M. MELGARA
CSELT S.P.A.
Via Reiss Romoli 274
I - 10148 TORINO

Tel: +39-11-216 94 89
Tlx: 220539
Fax: +39-11-216 95 20

Participants	**Country**	**Role**
CSELT S.P.A.	*I*	*M*
BRITISH TELECOM PLC	*UK*	*P*
CNET	*F*	*P*
IMAG	*F*	*P*
TRINITY COLLEGE DUBLIN	*IRL*	*P*

Start Date: 01-12-84   *Duration: 60 months*

SUBMICRON BIPOLAR TECHNOLOGY II

Project number : 281

The objective is the development of a bipolar technology for high speed data and signal processing products. The generation of bipolar technology, which was in production, at start of the project was characterized by minimum feature size of 2 um, a delay time of about 350 ps and an integration level for gate arrays of about 2500 gates.

The project aims at developing a technology with a minimum feature size of 1 um, a self-aligning transistor structure with delay times below 100 ps, a multilayer metallisation technique up to four layers, and an integration level of about 50K gates. In the area of high speed data processing, the developed technology will increase the performance by minimizing the number of inter-connection lines among the chips and by increasing the reliability. Both require an increase of the integration level and a reduction of the power delay product. The capacity of 10 Mips of present mainframe computers can be increased to about 40 Mips by means of this new technology. In the area of signal processing, the main advantage results from a reduction of the gate delay. The new technology will allow an increase of the signal processing speed of presently about 600 Mbits to more than 2 Gbits. It is intended to achieve the above objectives in three stages characterized by the following gate delay and power delay product: 200 pS and 0.4 pJ; 100 pS and 0.1 pJ; less than 100 pS and less than 0.1 pJ.

The first demonstrator, a 10k gate array, was available on schedule in mid 1986. The device is characterized by the following features: minimum structure size -mask dimension- 2 um, minimum metal pitch 6 um, 3-layer metallisation technique, self-aligned base-emitter structure, gate delay 200 ps, speed power product 0.4 pJ. The measurement results showed that both DC and AC parameters are meeting the specifications. Furthermore, the yield results indicated a sufficient state of maturity of the processing technology (OXIS III) to produce bipolar arrays with 10k gate complexity. The 2nd demonstrator, a 4k random access memory with an access time of less than 5ns the was demonstrated in March 1987, three months ahead of schedule.

The production of the ECL-Gate Arrays was started in a new pilot line at Siemens in the first quarter of 1987. These circuits are primarily intended to be used in advanced computers and will be available for all other European user companies. Siemens' investments for Pilot line are: 30 Million ECU for building and 64 Million ECU for equipment.

The results achieved with project 281 have enabled Siemens to start the development of a new family of gate arrays based on an improvement of the design rules previously used to assess the maturity of the developed technology (OXIS III) to produce bipolar gate arrays with 10K gate complexity. These new design rules enable a reduction of the speed-power product by approx 40% and an increase in the packing density of approx 30%

(OXIS III H). This new gate array family whose advanced specifications have already been announced, will provide a programmable speed-power product with 3 power steps where power dissipation will amount to 1W per 1000 gate functions. The complexity of these arrays will vary from 1.5K to 10K gate functions. First silicon is expected in May 1988.

Contact Point

Mr W.POLLER
SIEMENS AG
Balanstrasse 73
D - 8000 MÜNCHEN 80

Tel: +49-89-41 44 23 32
Tlx: 521080
Fax: +49-89-41 44 46 94

Participants	**Country**	**Role**
SIEMENS AG	*D*	*M*
RTC-RADIOTECHNIQUE COMPELECTR.	*F*	*P*

Start Date: 01-01-85

Duration: 60 months

ASSESSMENT OF SILICON MBE LAYERS

Project number : 305

The objective is to be better able to produce Silicon Molecular Beam Epitaxy (MBE) by adoption of existing equipment and techniques. The programme is as follows:

- Growth of silicon layers by Molecular Beam Epitaxy.
- In situ measurement of deposition conditions.
- Development and implementation of techniques for the characterization of MBE layers. This information will then be used to optimise growth conditions.

The project is on schedule.

Currently, Sb doped MBE and Solid Phase-MBE single layers have been grown and analyzed in detail and the results used for in situ doping control. Three and four layer structure for high frequency device applications have been made and assessed showing flat doping profiles and sharp transitions. Spreading Resistance has reached the resolution to profile multilayer structures and the correlation with SIMS quantitative measurement shows promising results. Results have also been presented on a method that allows separation of electrons from Si ions impinging on the substrate in order to improve the doping technique. A particle analyzer is being designed and constructed. This will be installed in an UHV chamber provided with an e-gun for Si evaporation.

Silicon MBE is potentially a key process in the production of future generations of Si and Si related devices. As a first approach, using the benefits of low growth temperature and precise control of layer thickness and doping profiles in any sequence, it is well suited for high speed devices and other integrated circuit applications. Furthermore, Si MBE also offers advantages for three-dimensional integration, because local epitaxial structures can be realized if a pre-patterned substrate is used.

Finally, utilizing the wide choice of material combinations and layer numbers made available, Si-MBE can open up a broader field of application for novel devices, e.g. metal silicides, SiGe heterostructures and superlattices, and hetero-junctions with III-V alloys. This project is contributing to these possibilities by producing an operational equipment to better enable the process to be used with confidence in future applications. Additionally, a range of characterization techniques for assessment of the MBE material will also have been produced which will find application in all Si device programs.

Contact Point

Dr E.KASPER
AEG A.G.
Sedanstrasse 10
D - 7900 ULM

Tel: +49-731-392 40 48
Tlx: 712723
Fax: +49-731-392 33 93

Participants	**Country**	**Role**
AEG A.G.	*D*	*M*
GEC RESEARCH LABORATORIES	*UK*	*P*
ISA RIBER	*F*	*P*

Start Date: 01-02-85

Duration: 36 months

PLASMA DEPOSITION TECHNOLOGY FOR MAGNETIC RECORDING THIN FILM MEDIA

Project number : 334

The objective of the project is to exploit the potential advantages of a significant increase of recording capacity when metallic thin films, instead of conventional oxide particles, are used as the basis for magnetic recording media. In order to develop such a technology, the interdependence of substrate materials, thin magnetic layers, overcoats, heads and drive systems need to be assessed, developed and produced accordingly. Leybold-Heraeus is to be responsible for the development of various deposition methods eg sputtering, evaporation and plasma-CVD for the magnetic layer stack. BASF is to be responsible for aspects of media fabrication and evaluation of differently prepared media, whilst the definition of the quality standards of the disks and their possible implementation into a disk drive system was entrusted, since October 1987, to SAGEM.

Among the different deposition methods, the sputtering has reached the most advanced status. At Leybold-Heraeus a sputtering system, suitable for study of production conditions, has been designed and built. The machine is a vertical in-line system for double-sided disk coating and provides the best conditions for a continuous production and for a high disk quality with a minimum risk of defects. The process technology for fabrication of disks with longitudinal recording has developed so far that the quality can compete with other good quality disks available on the market but the maximum storage capacity is expected to be achieved by vertical recording. For this purpose, complete layer systems were deposited, both in the above mentioned machine on hard disks and in a large roll coater on foils for the industrial production of floppy disks, with promising results.

Media studies by the partners clearly demonstrate the potential advantage (substantial increase in recording capacity) of thin magnetic layers over conventional oxide particles for high density recording. However, the switch-over to thin film media requires many modifications of the standard production technology. This new production technology of thin film is not yet fully developed but the leading position already achieved with respect to the longitudinal recording films is the first step towards the establishment of a complete process technology and the consequent beneficial fall-out for appropriate European I.T. industry and consumers by 1989.

Contact Point

Dr. P. WIRZ
LEYBOLD HERAEUS GMBH
Wilhelm-Rohn-Str. 25
D - 6450 HANAU 1

Tel: +49-6181-34 16 16
Tlx: 4152060
Fax: +49-6181-34 16 90

Participants	Country	Role
LEYBOLD HERAEUS GMBH	*D*	*M*
BASF A.G.	*D*	*P*
SAGEM	*F*	*P*

Start Date: 01-04-85 *Duration: 60 months*

PHYSICAL-CHEMICAL CHARACTERISATION OF SILICON OXYNITRIDES IN RELATION TO THEIR ELECTRONIC PROPERTIES

Project number : 369

The objective is to investigate the feasibility of implementing a process step using silicon oxynitrides by establishing:

- The relationship between the physical-chemical and the electrical properties of silicon oxynitride film.

- The relationship between the physico-chemical properties and the growth parameters.

The work is important in view of the likely applications of silicon oxynitrides in IC technology, for example in MNOS-based non-volatile memories and in submicron MOS devices.

A large number of the material characteristics of silicon oxynitrides have been determined. This knowledge is very important for the assessment of the improvement of the cost/performance ratio and the reliability of future generations of integrated circuits.

Studies into the basic understanding of the growth and characteristics of LPCVD and thermally grown silicon oxynitrides have enabled the following three technologically important conclusions to be made:

- The stress in the silicon oxynitrides is lowered upon introduction of oxygen in the nitride lattice, whereupon the oxidation resistance is comparable or even better than that for the nitride. Accordingly, the "bird's beak" length in the LOCOS process has been shown to be shortened by a factor of two, without any increase in the number of defects.

- For the application of oxynitride films in MNOS type devices, the oxynitride with the ratio of $O/(O+N) = 0.2$ appears to be the most suitable material. This is a trade-off between decay rates, which appear to decrease with increasing oxygen content, and other memory characteristics such as center of window and endurance.

- The hydrogen chemistry in the films is extremely important for various electrical and optical properties.

The results are applicable in the future production of non-volatile memories and sub-micron devices. Already a considerable reduction of the "bird's beak" in the LOCOS process has been demonstrated by use of oxynitride films. Both Philips and Matra are currently considering the exploitation potential of this within their respective environments.

Contact Point

Dr W.F. VAN DER WEG
UNIVERSITEIT VAN UTRECHT
Princetonpleinweg 5
Postbus 80000
NL - 3500 TA UTRECHT

Tel: +31-30-53 32 69
Tlx: 40048 FYLUT NL
Fax:

Participants	**Country**	**Role**
UNIVERSITEIT VAN UTRECHT	*NL*	*M*
AERE-ATOMIC ENERGY RES. ESTABL.	*UK*	*P*
IMEC V.Z.W.	*B*	*P*
MATRA HARRIS SEMI-CONDUCTEURS	*F*	*P*
PHILIPS GLOEILAMPENFABRIEKEN	*NL*	*P*

Start Date: 01-12-84

Duration: 48 months

SILICON-ON-INSULATOR SYSTEMS COMBINED WITH LOW TEMPERATURE SILICON EPITAXY

Project number : 370

The objective is to obtain single crystalline layers of silicon-on-insulator (SOI) with thicknesses from 0.5 micron to 30 micron, for a variety of applications. The results were potentially applicable both to silicon-on-insulator, for high performance integrated circuits, and as alternative to dielectric isolation (DI) processing. The project was completed on 1.12.87 but the final reports are not yet available. The results are as follows:

- A new system has been developed for the re-crystallisation of full wafers based on a focused high-pressure mercury arc lamp.
- Re-crystallisation experiments have been performed with focused laser beams and with the strip-heater system.
- A detailed study of the influence of all process parameters for both techniques is almost complete.
- Successful seeded and unseeded re-crystallisations have been performed with both techniques leading to good quality material. Strip-heater layers of between 0.5 micron and 10 micron have been directly re-crystallised with good success.
- Epitaxial thickening of thin SOI layers has been performed on limited area structures and is being continued on large area structures.
- A range of trench etching equipment has been evaluated and a system has been purchased and installed. Trenches up to a depth of 10 micron have been made without visible corner rounding. Oxide-polysilicon-oxide sandwich layers have been evaluated as trench fillers.
- The design of a Combined Insulator and Epitaxy equipment for the photo-chemical deposition of insulators and silicon has been completed.

The project has demonstrated that the methods used are technologically feasible but not, as yet, economically viable.

Contact Point

Prof. H. MAES
IMEC V.Z.W. — *Tel: +32-16-28 12 83*
Kapeldreef 75 — *Tlx: 26152*
B - 3030 LEUVEN-HEVERLEE — *Fax: +32-16-22 94 00*

Participants	Country	Role
IMEC V.Z.W.	*B*	*M*

GEC RESEARCH LABORATORIES	*UK*	*P*
MIETEC N.V.	*B*	*P*

Start Date: 01-12-84 *Duration: 36 months*

A HIGH PERFORMANCE CMOS-BIPOLAR PROCESS FOR VLSI CIRCUITS (BICMOS)

Project number : 412

This project aims at the development of a VLSI technology which combines, on a single chip, MOS circuitry of the highest density presently obtainable with bipolar circuitry of similar density, but better suited to specific tasks eg. the analog interfacing with external world. The main effort will be on the technological side: development of methods which allow both bipolar and MOS transistors to be made in compatible process steps, and in dimensions comparable to those presently obtained in MOS-only technology. In parallel with this technological work, design methods have to be developed for this specific type of circuit, a mixture of analog and digital functions, along with a study to determine, for various types of application, the most appropriate division of subsystems between the two circuit technologies.

Besides the definition and checking of the flow chart of a rather complex process, called BICMOS 1 (1,5 um emitter width for bipolar devices combined with 1.5-1.2 um CMOS transistors) including 13 ion implantations and 16 mask steps, the partners have agreed on a common set of design rules and have demonstrated the workability of this approach. Philips has successfully processed a Siemens design for a simple function (operational amplifier), demonstrating design portability between the developed processes. Application studies of the mixed process are progressing fast, resulting in the design of a number of digital and analog functions. These functions had been simulated and implemented on silicon in the already developed 2um process, BICMOS 0. These checks show the strengths and weaknesses of the design tools in the analog field but allow the quantitative evaluation of the advantages of a mixed process over plain CMOS, notably for drivers and analog functions. The main functions needed by the first demonstrator, a micro-processor controlled "audio-center" of about 20K transistors, had been successfully implemented and the first silicon of this circuit is now (December 87) in the Philips 150 mm process line. On the other hand, intermediate technical target performances (500 MHz for CMOS toggle frequency and 3 GHz bipolar f_t) will be reached on schedule in April 1988.

Fruitful collaboration between design skill in universities and industrial technologies has been demonstrated. Some patents for new circuit structures have already been applied for. The demonstrators of these BICMOS technologies, a micro-processor controlled "audio-center" followed by a video signal processor, are mainly aimed at the consumer market in their final stage. But other applications of BICMOS, in the field of fast computing, are also envisaged. Some questions arose on the cost of such a complex process for volume production. However, the results to date indicate that the yield of the CMOS process is not affected by the additional process steps needed for bipolar transistor manufacturing. The gain in circuit area obtained with the BICMOS process, when compared to CMOS, is such that a large increase in yield and an overall decrease in manufacturing costs were demonstrated in the

BICMOS 0 stabilized process which is now being used for large volume production.

Contact Point

Dr P.A. HART
PHILIPS GLOEILAMPENFABR. N.V.
Wag 1
P.O. BOX 80000
NL - 5600 JA EINDHOVEN

Tel: +31-40-74 20 22
Tlx: 35000
Fax: +31-40-74 46 17

Participants	**Country**	**Role**
PHILIPS GLOEILAMPENFABR. N.V.	*NL*	*M*
SIEMENS AG	*D*	*P*

Start Date: 01-04-85

Duration: 60 months

MOLECULAR ENGINEERING FOR OPTO-ELECTRONICS

Project number : 443

Optics and microelectronics will increasingly co-exist in the form of active or passive optical interconnects between microelectronic chips, mixed opto-electronic devices and purely optical devices as part of mixed opto-electronic systems. Furthermore organic electro-optic and non-linear optical materials can find application in logic elements, large band modulators, tuneable parametric amplifiers and emitters in transmission and signal processing systems. The objective is to provide a basis for the essential knowledge of the development of molecular based Information Technology devices.

Progress to date includes the following:

- The assembly of a reliable code for the prediction of molecular beta from atomic coordinates.
- The development of an efficient routine for searching the crystallographic data bases for active molecules of suitable symmetry for $X^{(2)}$.
- Knowledge of the effects of hydrogen bonding on hyper-polarizarability.
- A methodology to calculate the static polarizability and hyper-polarizabilities of molecules within the Routine Hartree Fock (RHF-Sum Over States and RHF-Finite Field frameworks).
- A methodology to calculate the static polarizability of infinite regular polymers within the RHF-Sum Over States framework.
- Identification of various bonding patterns capable of high electronic responses.
- Synthesis and demonstration of excellent properties in pyrazoline and polyene molecules predicted in the developed model.
- The setting up of relevant facilities for the characterisation of beta and $X^{(2)}$.
- The synthesis and dipping of a range of tailor made molecules from which high second harmonic generation has been observed.
- The attachment of active molecules to a polyester backbone to give liquid crystal phases. Addition of beta has been obtained by aligning under an electric field applied above T_g and cooling to the immobile phase vectorial.
- Quantification of the factors which govern the lattice symmetry for the

polar molecules of interest is now well underway and a number of effective routines have been written to model crystallization.

- The successes in L-B and liquid crystal techniques, motivated by the desire to construct planar waveguide arrays for integrated optics. L-B technology has highly benefited from Phase I of the project and the knowledge of deposition conditions, structural properties and nonlinear properties started from almost nil at the onset of the Project to reach a level where technological follow-ups are in view.
- The development of ultrafast ultrasensitive spectroscopic or I-R signal processing tools (PASS).

The progress detailed represents significant progress towards the objective of the project and hence the eventual production of devices for signal processing and optical computing. However, other specific aspects such as packaging, electrode deposition, integration of devices onto arrays etc. need to be addressed before such devices can be realized.

Contact Point

Dr J. ZYSS
CNET
196 Avenue Henri Ravera
F - 92220 BAGNEUX

Tel: +33-1-45 29 53 14
Tlx: 202266
Fax: +33-1-45 29 54 05

Participants	**Country**	**Role**
CNET	*F*	*M*
UNIVERSITE DE NAMUR	*B*	*P*
ICI PLC	*UK*	*P*

Start Date: 31-12-84 *Duration: 36 months*

MATERIALS AND TECHNOLOGIES FOR HIGH MOBILITY TFTS FOR LC DISPLAY BUS DRIVERS

Project number : 491

The objective of the project is the development of thin film materials and technologies for column-bus and line-bus drivers to replace external IC-chips for peripheral driver circuits of active matrix liquid crystal displays (LCDs). The main task is to develop a low temperature deposition process for the semiconductor thin film material compatible with the glass substrates used for the LCD. The main material to be used is poly-crystalline silicon. The deposition processes to be investigated are plasma-enhanced CVD and e-gun evaporation, whereas LPCVD is used to establish the Thin Film Transistor (TFT) process technology. Furthermore, elementary TFT circuits, suitable for bus driver shift registers, will be developed and investigated and driver prototypes of short length will be combined with LCD matrices and tested.

The main milestones so far have been achieved on time. Poly-crystalline Si films prepared below 600°C on boro-silicate glasses have been processed to produce TFTs. With PECVD and LPCVD, the capability exists to prepare PECVD Si_3N_4 transistors with field effect mobilities up to 35 cm^2/Vs. In this the Si is deposited at around 580°C. TFT's with e-gun Si-films deposited at 550°C were prepared by using a APCVD (atmospheric pressure CVD) SiO_2 which yields better TFTs than with plasma process gate insulators. These TFTs exhibit field effect mobilities up to 16cm^2/Vs. In all cases the costly process of ion implantation has been avoided. At the deposition temperatures mentioned above it is no longer necessary to use expensive quartz substrates for the Si deposition instead high quality glass can now be used but additional investigation is necessary to decrease these deposition temperatures further to values where cheap soda lime glasses can be used.
A new TFT equivalent circuit has been inserted into the "SPICE" simulation program. With it, the static TFT and a 5 level inverter can be simulated. Tests of the dynamic behaviour of this program are currently being undertaken.

It can be expected that at the end of the project (mid 1990) the driver circuits will be capable of addressing a 300 x 300 LCD matrix with a resolution of 4 pixels per millimetre. This will provide Europe with a state-of-the-art capability in large area display electronics.
This progress in the development of these thin film transistors is a key step towards the evolution of alternative display technologies which can replace, for example, the conventional cathode ray tube in applications requiring miniturisation or portability. In addition, this TFT technology will impact on other applications in large area electronics e.g. addressing of large area photo-conductor scanners.

Contact Point

Dr N. MARSCHALL
AEG A.G.
Goldsteinstrasse 235
D - 6000 FRANKFURT AM MAIN 71

Tel: +49-69-6679 232
Tlx: 414474
Fax: +49-69-6679 311

Participants	**Country**	**Role**
AEG A.G.	*D*	*M*
CNET	*F*	*P*
CSEE	*F*	*P*

Start Date: *01-06-85*

Duration: *60 months*

QUANTUM SEMICONDUCTOR DEVICES

Project number : 514

The recently developed methods of semiconductor crystal growth (MBE, MOCVD) have opened an era of new semiconductor devices which incorporate the principles of quantum mechanics in their design and operation. The objective is to provide new knowledge in this area by investigating new concepts in the promising field of "Quantum Semiconductor Devices" both experimentally and theoretically. The main efforts are to be devoted to one- and two-dimensional device operations and to perpendicular transport through multilayers.

Some of the results obtained so far are listed as follows:

- Two-dimensional electron gas and multi-quantum wells in the GaInP/GaAs.
- The demonstration of the two-dimensional hole gas in GaInAs/InP.
- The room-temperature demonstration of a super-lattice tunnel oscillator.
- Demonstration of ballistic motion of hot-electrons injected from graded-gap hetero-junctions.
- The highest reported electron density in a planar-doped GaAs structure.
- The observation of simultaneous electrical and optical bi-stability in a semiconductor multilayer structure.
- The observation of the Quantum Hall effect at the GaInAsP/InP hetero-junction.
- The observation of extremely low dark currents in graded parameter superlattices.
- Lasing in the GaInAs/InP system.

The theoretical work in support has achieved the following:

- A theory of high field transport in superlattices providing underpinning for the design of novel structures.
- The theory of graded parameter super-lattice structures giving rise to new design rules for photo-diodes.
- Detailed bandstructure calculations giving new insights with device implications.
- The simulation of delta doped GaAs structures allowing both electron states and transport.

During the first 30 months the partners have produced 85 scientific papers

relating to the project. Some of the results have been applied to other ESPRIT projects (522, 843, 971) on III-V devices.

In general, work on the new generations of optical and electronic ICs will certainly benefit from the work carried out in this project.

Contact Point

Dr M. KELLY
GEC RESEARCH LABORATORIES
East Lane
Wembley
UK - HA9 7PP MIDDLESEX

Tel: +44-1-904 92 80
Tlx: 923429
Fax: +44-1-904 75 82

Participants	**Country**	**Role**
GEC RESEARCH LABORATORIES	*UK*	*M*
THOMSON CSF/LCR	*F*	*P*

Start Date: 01-02-85 *Duration: 60 months*

DOPANT PROFILING FOR SUBMICRON STRUCTURES

Project number : 519

The objective is to establish measuring techniques for the accurate determination of shallow dopant profiles as used in submicron devices. To achieve this, the development of one electrical technique, i.e. Spreading Resistance (SR), is proposed, together with a comparison of this technique with other non-electrical methods, i.e. Secondary Ion Mass Spectrometry (SIMS), Neutron Activation Analysis (NAA) and Rutherford Back Scattering (RBS). The primary emphasis of the project will be put on the development and use of the spreading resistance technique with the other techniques being used primarily for comparison. A software package to this end will be produced. A major by-product of this approach will be the data enabling a better understanding of diffusion kinetics to be obtained. In addition the work will concentrate on profiling Boron, Phosphorus, Arsenic and Antimony and will also involve the use of and assessment of novel annealing methods such as strip heater and flashlamp annealing.

The capability to prepare small area probes has been demonstrated which is important for the accurate calculation of the doping profile in semiconductor junctions. An operating system software package has been completed in order to increase the throughput and the accuracy of SR and a first version of an improved software package for data conversion, including smoothing procedures has been released. Comparison data on MBE samples with sequences of thin layers with high and low doping and on a rapid thermally annealed samples obtained by SIMS or NAA, shows good correlation. A paper has been published describing these results.

IMEC has developed a first version of an improved software package for SR conversion including improved algorithms and a powerful smoothing feature. They intend either to make this first version available to interested parties and or to provide a complete SR service on their system using this technique. The experimental and theoretical improvements in the SR technique will be applied by AEG to the assessment of layers grown by MBE within Project 305, for high frequency (100 GHz) device structures, and, by GEC to the assessment of starting materials and profiles used in CMOS process development. Structures from other ESPRIT projects (e.g. SOI and Bipolar) are under analysis to test the validity of the techniques and enable its confidence to be established for wider applicability.

Contact Point

Dr M. PAWLIK
GEC RESEARCH LABORATORIES
East Lane
Wembley
UK - HA9 7PP MIDDLESEX

Tel: +44-1-908 90 00
Tlx: 923429
Fax: +44-1-904 75 82

Participants	**Country**	**Role**
GEC RESEARCH LABORATORIES	*UK*	*M*
AEG A.G.	*D*	*P*
IMEC V.Z.W.	*B*	*P*

Start Date: *15-02-85* *Duration:* *60 months*

INVESTIGATION OF ALL ASPECTS OF THE INTERCONNECTION OF HIGH PINCOUNT I.C.

Project Number : 544

The objectives were:

- The development of alternative methods of connecting the integrated circuit to its interconnection medium. This is seen to be particularly appropriate for devices fabricated according to the end users design with high pincount.

- The development of large area (30 x 30 cm) high density (250/125 um pitch) interconnect using multilayer polymer techniques (since polymers are very low in cost and layers can be superimposed quite easily).

- The development of medium area (17.5 x 12.5 cm) ultra high density (50/25 um pitch) interconnect based on a combination of thick film dielectrics and additive base metal electroplating methods.

It is the aim to realise all interconnect systems with just two signal layers, thereby achieving low cost through reduced handling and inexpensive materials. The project was completed at the end of 1987 but the final reports are not yet available.

The deposition of copper on silicon has been studied. The aim was to deposit high conductivity copper tracks on the passivation layer of an IC. Tracking of ten microns wide and 3 microns high copper with a conductivity close to bulk copper has been realised on the passivation of silicon ICs.

A system using screen printed polymer thick film material has given good results at 250 micron resolution in structures of at least two layers. It was found that the benefits of such a system lie not so much in high track density but rather in the realisation of a large area medium density interconnection on an organic substrate which cannot withstand high processing temperatures. For that reason the original target of 125 micron pitch was not further pursued.

The process for producing ultra high density interconnection patterns on aluminia substrates using a combination of copper plating technology and laser drilled vias in thick film dielectric has been established, with good results (25 micron pitch) achieved. This combines the advantages in reliability and thermal performance of thick film with the conductivity and line definition obtainable from electroplated copper. The process already developed yields tracking down to 25 microns in width with thickness up to 25 microns. Results of further optimisations for applications on large alumina boards (typically 150mm x 150mm in size) are expected in the final report.

The copper tracking has application for the distribution of power in VLSI and Wafer-Scale circuits where the areas and current requirements may impede

the use on conventional metallisations.

A new small dedicated processing equipment line based on thick dielectric films is being set up by BAe. The low cost multilayer polymer techniques are planned to be introduced into commercial applications during 1988 by Lucas Stability Electronics.

In addition, NMRC is applying the results of the 1st objective in WSI applications (Project 824).

Contact Point

Mr J. BARRETT
NAT. MICROEL. RESEARCH CENTRE
Lee Maltings
Prospect Row
IRL - CORK

Tel: +353-21-27 68 71
Tlx: 26050
Fax: +353-21-27 02 71

Participants	**Country**	**Role**
NAT. MICROEL. RESEARCH CENTRE	*IRL*	*M*
BPA TECHN.& MANAGEMENT LTD	*UK*	*P*
BRITISH AEROSPACE PLC	*UK*	*P*
LUCAS STABILITY ELECTRON	*UK*	*P*

Start Date: 01-08-84 *Duration: 36 months*

SUBMICRON CMOS TECHNOLOGY (SPECTRE)

Project number : 554

The objective is to develop the necessary building blocks for a 0.7 micron CMOS process, primarily dedicated to the production of high speed (within the limitations imposed by MOS) digital circuits. In order to allow the programme to proceed with the best chances of success, two main phases have been identified and organised. The first task refers to an intermediate step at the 1.0 um level, the second, to the final 0.7 um CMOS family. Two additional tasks were added to the original project at the end of the first year. Consequently, the programme is composed of eight tasks. These address the topics of architecture , optical and electron-beam lithography, MOS Structures, Isolation, Interconnect and refractory metal gates . The first task involves the arrangement of the Pilot-Line demonstration of the 1 micron and submicron demonstrators. The subsequent tasks provide the technology inputs for this.

Each task is on target for the three-year intermediate and for the five-year submicron demonstrators. The architecture for both has been defined. The detailed technical specifications have been postulated or are now being refined and, for the year three demonstrator, wafers are being processed by CNET.

The demonstrator circuit includes:

- A whole set of test patterns designed in such a way that not only the design rules but also their sensitivity to process variations can be demonstrated.

- Two 4K SRAM with a cell of 6 transistors all designed by IMEC and CNET (this being a reference circuit at CNET).

- An image processor (with about 80.000 transistors) designed by British Telecom.

In the area of lithography, several commercial units have been evaluated and one of these selected for the first demonstrator. Investigation of the available resists has indicated that a number of these are suitable for use in the first demonstrator when used in a "tuned" process. The reticle technology and methodology have yielded good results to date.

In MOS structure studies much progress has been made on the evaluation of basic 1 micron devices. Common definition of the test pattern, the comparison of simulation and measurement, and the exchange of wafers between laboratories have allowed more rapid progress in the definition of process steps to be realised than would otherwise have been possible.

At the end of 1987, experimental data of four approaches (conventional wells, twin-wells, refractory gate and retrograde well) will be available for

comparison providing a good basis to choose the best options for the final 0.7 micron technology.

As part of the isolation work, optimised LOCOS was used to process the 1-micron demonstrator, but comparison with twin-well plus SUPERPLANOX is still underway. Other processes are to be assessed (e.g.SILO, trench, mini-trench or box).

In the contact and interconnect work, two interconnect schemes have been assessed: the conventional double aluminium and the tungsten/aluminium system. Comparing performance achieved with W and Al, whilst taking into account the electromigration effect, it was concluded that the optimum interconnect scheme will use W at first level and Al at second level. For the 1-micron demonstrator, both sputtered and CVD tungsten are being investigated.

At the end of December 1987, the one micron CMOS process results were disseminated throughout eleven companies and research laboratories located in five European countries.

Additionally, Matra Harris successfully transferred the SPECTRE CMOS technology into its 64K fast static RAMs and microprocessor fabrication lines and selected process steps are being integrated in the fabrication process of a 1 MEGA EPROM by STM.

The above are early indications of the uses to be made of the technological breakthroughs which will be exploited as a result of this project. The objectives are in line with the world-wide state-of-the-art expectations for high density ICs.

Contact Point

Mr J.P. KLEIN
CNET CNS
Chemin du Vieux Chêne — *Tel: +33-76 51 41 09*
B.P. 98 — *Tlx: 980727F*
F - 38243 MEYLAN CEDEX — *Fax: +33-76 51 41 47*

Participants	**Country**	**Role**
CNET CNS	*F*	*M*
BRITISH TELECOM PLC	*UK*	*P*
BULL S.A.	*F*	*P*
IMEC V.Z.W.	*B*	*P*
MATRA HARRIS SEMICONDUCTEURS	*F*	*P*
SGS MICROELETTRONICA SPA	*I*	*P*
UNIVERSITE CATHOLIQUE LOUVAIN	*B*	*P*
CNR-ISTITUTO LAMEL	*I*	*S*
AERE-ATOMIC ENERGY RES.ESTABL.	*UK*	*S*
TELETTRA S.P.A.	*I*	*S*

AARHUS UNIVERSITY	*DK*	*S*
Start Date: *31-12-84*	*Duration:*	*60 months*

HIGH RESOLUTION PLASMA ETCHING IN SEMICONDUCTOR TECHNOLOGY- FUNDAMENTALS, PROCESSING AND EQUIPMENT

Project number : 574

The objective of this project is to gain a better understanding of the complex chemistry and physics involved in plasma etching by applying suitable diagnostics methods in order to make possible the use of its full potential. The knowledge gained is to be applied in improved equipment and process realization.

The first part of the work was devoted to the development of measurement instrumentation and equipment set-up. In particular, an optical emission spectrometer and a quadrupole mass spectrometer were installed in a reaction chamber in order to detect the chemical species created when the etching reaction is takes place. A reactive ion etching process has been successfully established for a 0.5 micron structure size.

A three chamber reactive ion etching machine has been developed by Leybold. A paper describing the equipment was presented at the ESPRIT 87 Conference in September.

It is widely recognized within the electronics industry that plasma etching will play a vital role in achieving submicron technology both in silicon and III/V semiconductor systems.

Knowledge of the plasma etching process combined with the participation of an equipment manufacturer are the basis of a new generation of etching machines together with the development of ancillary materials such as photo-resist. The study of the reaction kinetics paves the way for an improved etching process to be designed which can be utilized as a term of reference by other industries because of the wide-spread research work. Already, as a result of this project to date an advanced plasma etching machine has been produced by one of the partners. This equipment is capable of processing 200mm wafers with ICs designed with 0.5 micron structure size. A prototype has been recently shown at the Produktronika 87 Fair in Munich and commercialization is expected to follow in 1988.

Contact Point

Dr H. SCHEER
FRAUNHOFER IM
Dillenburger Strasse 53
D - 1000 BERLIN 33

Tel: +49-30-82 99 81 11
Tlx: 184821
Fax: +49-30-82 99 81 99

Participants	**Country**	**Role**
FRAUNHOFER IM	*D*	*M*
AERE-ATOMIC ENERGY RES.ESTABL.	*UK*	*P*
LEYBOLD HERAEUS GMBH	*D*	*P*

MONO LIGHT INSTRUMENTS LTD. *UK* *P*

Start Date: 01-01-85 *Duration: 48 months*

CAD FOR VLSI SYSTEMS (CVS)

Project number : 802

The objective is to implement an integrated CAD system capable of coping with the needs of the nineties, where the improvements of the semiconductor technology will allow the production of chips of about 1 million transistor complexity. Such a CAD system must lead to a factor of 10 improvement in design time, based on novel tools for automatic construction of designs at the level of system architecture by interconnecting cells representing parts of the total system which have themselves been constructed automatically from a set of given parameters.

The areas of work include therefore, architecture synthesis, digital cell building, analogue cell design, integration of tools and design of demonstration chips. The first prototypes of tools will be delivered by the end of 1989.

During the first twenty-one-month period the project has revised their plan for the work on architectural synthesis in response to the first project review, has completed the design of the tools and is part way through the implementation of the agreed tools and system.

They have selected an advanced signal-processing chip which is part of a new radio-telephone receiver as the vehicle to demonstrate the effectiveness of the tools developed. The rough architectural plan of this target chip has been agreed.

Such a CAD system is expected to lead to a factor of 10 improvement in design time. For chips which will not be sold in very large numbers, rapid and accurate design is of the utmost importance. The techniques of automatic construction of the designs, both at the architectural level and for analogue cell design, should be important elements in achieving this aim.

In order to have maximum impact on industry in general, in addition to internal use by the partners, it is agreed that the resulting software will be made available to third parties (e.g. software houses) for the marketing of the results. One company (ANACAD) in Germany has already taken steps to bring some of the results to the market place.

Contact Point

Dr L. LEPRONI
CSELT S.P.A. — *Tel: +39-11-216 93 22*
Via Reiss Romoli 274 — *Tlx: 220539 CSELT I*
I - 10148 TORINO — *Fax: +39-11-216 96 95*

Participants	Country	Role
CSELT S.P.A.	*I*	*M*

AEG A.G.	*D*	*P*
CIT/ALCATEL	*F*	*P*
BRITISH TELECOM PLC	*UK*	*P*
CNET	*F*	*P*
GMD-GES.F.MATHEMATIK & DATENVER.	*D*	*P*
ITAL TELMATICA SPA	*I*	*P*
MATRA HARRIS SEMI-CONDUCTEURS	*F*	*P*
SGS MICROELETTRONICA SPA	*I*	*P*

Start Date: 01-03-86 *Duration: 54 months*

WAFER SCALE INTEGRATION (WSI)

Project number : 824

The objective is to use the Wafer Scale Integration (WSI) approach to built systems up to 25 million transistors on a 10 centimetre wafer using a hierarchical approach to implement tolerance to manufacturing defects. Three demonstrators will identify the progress made in the project:

- A 4.5 MBIT Static Ram
  The main goal of the 4.5 megabit RAM memory (access time 100 nsec) is to examine the possibility of efficiently using switches in order to discard faulty elements and replace them with spares. Starting from cells of 64 Kword of 1 bit, the final interconnection network to be produced on a 10cm wafer will implement 18 blocks of 256K x 1 bit.

- A WSI Systolic Array
  Systolic arrays are well suited to WSI because all communications are between nearest neighbours. The approach is to define a general purpose architecture that is likely to cope with many application problems notably in processing video images, display graphic and advanced memory devices. The chosen architecture is a 128 x 128 array of processing elements.

- A 16 bit microprocessor
  The long-term goal is to integrate a fully dedicated system on a single chip using pre-defined blocks embedded in a flexible interconnection structure, for example, a sea of gates. Being the master block of the system the microprocessor has to be particularly adapted to the application, but its architecture must also be compatible with fault tolerance. The project is to develop a library of pre-defined and parametered elements as well as design tools to produce the layout of a 16 bits reconfigurable microprocessor. Such an approach is needed in order to guarantee short design times together with adaptation to the application constraints in both terms of functionality and speed.

After one year, the first silicon (WSI test mask) on Wafer Scale Integration has been processed successfully. Switches to reconfigure a wafer have been dispatched to every partner: either to blow fuse, or to correct with Laser Lithography and lift-off, or to charge and discharge floating gate FETs. The first results on the characterization of these switches are in agreement with the target. Blocks for building the Wafer Scale demonstrators have been designed and processed during the second year, they are:

- A 16 bit plus 1 spare bit application specific microprocessor (building block for a "big chip" with microprocessor, memory, peripherals.)

- A 2 * 2 and 8 * 8 systolic arrays (building blocks for a Wafer Scale systolic array).

- The extra hardware necessary to interconnect on wafer 72 static RAM of 64 kword 1 bit; in order to achieve a 4.5 Mbits SRAM.

Additionally, two WSI architectures, for a memory and a systolic array, have been proposed with solutions to the difficult problem of reconfiguration and test-ability.

The developed know-how in technology will allow correction of "end of manufacturing" defects and hence improve the ability to realize full custom, one million transistor chips for the ASIC sector.

From the system point of view, the developed systolic array as it is more compact and can contain more processors than any other available system, is opening up a whole new range of applications notably for signal processing functions in video applications.

Contact Point

Mr J. TRILHE
THOMSON-EFCIS
Av. des Martyrs 17
F - 38019 GRENOBLE CEDEX

Tel: +33-76 49 36 00
Tlx: 320226
Fax: +33-76 49 36 47

Participants	**Country**	**Role**
THOMSON-EFCIS	*F*	*M*
BRITISH TELECOM PLC	*UK*	*P*
TECH. HOCHSCHULE DARMSTADT	*D*	*P*
INPG	*F*	*P*
CEA/LETI	*F*	*P*
NAT. MICROEL. RESEARCH CENTRE	*IRL*	*P*

Start Date: 15-05-86 *Duration: 48 months*

PACKAGES FOR HIGH SPEED DIGITAL GAAS INTEGRATED CIRCUITS

Project number : 830

The various package design requirements being evolved to meet the requirements of the GaAs IC industry are to be investigated. The objective is the establishment of package standards, together with clearly defined design principles and methods of fabrication. The project will lead to the establishment of 4 package designs an 8,16,24 and 40 I/O lead package having the necessary operational characteristics for mounting and hermetically encapsulating GaAs ICs for use in high speed digital applications. Extensive use will be made of sophisticated computer-aided design and simulation modelling, the success of which has already been established in the case of the 8 I/O lead package.

Three technical approaches to package construction will be investigated: the use of direct-sealing techniques, glass joining fired ceramic and co-firing glass-ceramic. Associated topics to be investigated will include: materials, metallisation and heat dissipation.

Sample packages of the various designs will be made available for evaluation and qualification approval testing.

This project is complementary to project 958 as part of the "Advanced Packaging" work-programme.

The work is on schedule towards the principal objectives. During the first year, the direct sealing method of package fabrication, originally used at Thomson, has been established at M-O Valve. Samples of the 8 I/O original design have been supplied to Thomson and results are promising. Samples of 16 I/O fabricated under the fired glass joining approach have also been supplied. The green glass ceramic approach is progressing well, and prototype structures are now emerging. Within the second year, the redesign of the 8 and 16 I/O packages has been performed and samples, incorporating these design changes, have been made available for evaluation.

During the life of the project, sales of the 8 and 16 I/O packages are expected to commence both after the first two years and at the end of their evaluation programme. In the first instance potential customers are the collaborators of the ESPRIT GaAs IC projects (843 and 971). Following this, it is expected these packages will be exploited more widely.

Volume production of the full range of packages is expected to start in 1989/90 when the qualification exercise has been completed, building to a peak in the mid 1990's.

Contact Point

Mr C. EVANS
M.O. VALVE COMPANY LTD.
Brook Green Works
Hammersmith
UK - W6 7PE LONDON

Tel: +44-1-603-3431
Tlx: 23435
Fax: +44-1-602 33 65

Participants	**Country**	**Role**
M.O. VALVE COMPANY LTD.	*UK*	*M*
THOMSON CSF	*F*	*P*

Start Date: 31-01-86

Duration: 48 months

LARGE AREA COMPLEX LCDS ADDRESSED BY THIN FILM SILICON TRANSISTORS

Project number : 833

The project was completed in May 1987.

Liquid Crystal Displays (LCDs) have emerged to become the dominant flat panel display technology in recent times. Their low power and voltage requirements are advantageous, not only for portability, but also because they lead to unstressed highly reliable electronics which, when combined with the lack of inherent failure modes in LCDs, yield very thin lightweight displays with service lives orders of magnitude longer than Cathode Ray Tubes (CRTs). Thin-film transistor addressing of LCDs would allow an increase in display size and complexity to levels adequate for word processor and graphics displays.

The objective of the present project was to investigate a viable technology for the fabrication of large area (A5 to A4) and complex (up to 1000 addressable lines) LCDs based on poly-crystalline and amorphous silicon transistor active matrices. Silicon Thin Film Transistors (TFTs) show promise of higher yield and reliability than other TFT materials.

Extensive investigation of the following areas was planned:

- Optimisation of transistor characteristics, yield and stability over large areas
- Special high throughput, large area semiconductor processing equipment
- Special LCD fabrication techniques
- Colour systems
- Interactive displays
- Human factors.

A breakthrough in the technology of polysilicon TFTs on glass has allowed GEC to achieve, in a reproducible manner, and in small-geometry (10 x 10um) devices, on-off ratios in excess of 105, mobilities of 10 cm2/V-sec and threshold voltages as low as 8V. A new active matrix circuit has been patented which entirely eliminates line failures and this increases the yield enormously. These breakthroughs have been verified on test displays 6 x 4 cm in size with 96 x 64 pixels, which have been fabricated with less than 10 defects. 8.5 x 8.5 cm displays with 150 x 150 pixels are under development. In the amorphous Silicion (a-Si) area, in addition to the CNET proprietary technology, Thomson CSF has developed an alternative potentially high-yield process based on small-geometry (10 x 20 um) high-mobility (0.4-0.7 cm2/V-sec) TFTs and demonstrated almost defect free 6 x 8 cm displays with 256 x 320 pixels.

CNET has demonstrated an 8 x 8 cm colour display with 320 x 320 pixels based on a new RGB colour filter technology. A system based on capacitive interaction with resolution of 0.4 mm has been realised. AEG has achieved very low pinhole density (1 per cm2) sputtered silicon dioxide. Modulex has developed drive circuitry interconnections using high throughput tape automated bonding of chips on to flexible p.c. board. Significant achievement has also been made in the areas of plasma silicon nitride and large area display photo-lithography.

Following the end of the planned work schedule, a number of prototype displays were demonstrated at the ESPRIT conference in September 1987. A major follow up project is planned within RACE to exploit the results already achieved.

Some recent surveys have underlined the importance of new display technologies because of their potential for eventually replacing CRTs as the principal Visual Display medium for a range of informatics based products. The progress listed above has placed the collaborators in a strong position, even with respect to the Japanese competition, particularly because of the availability of both polysilicon and amorphous silicon technologies.

As an indication of their success, companies such as Hitachi and Seiko Instruments have sought contacts with the partners in this project. In view of the above competitive position in R & D, supported by a number of demonstrators and their well recognised production capability in LCDs, the industrial collaborators are now, for the first time, in a position to challenge the long standing Japanese supremacy in this field.

Contact Point

Dr M. CLARK
GEC RESEARCH LABORATORIES
East Lane
Wembley
UK - HA9 7PP MIDDLESEX

Tel: +44-1-908 90 00
Tlx: 923429
Fax: +44-1-904 75 82

Participants	**Country**	**Role**
GEC RESEARCH LABORATORIES	*UK*	*M*
MODULEX A/S	*DK*	*P*
AEG A.G.	*D*	*P*
THOMSON CSF/LCR	*F*	*P*
CNET	*F*	*P*
UNIVERSITY.OF THESSALONIKI	*GR*	*S*
UNIVERSITA DI BOLOGNA	*I*	*S*

Start Date: *10-12-85* *Duration:* *18 months*

COMPOUND SEMICONDUCTOR INTEGRATED CIRCUITS

Project Number : 843

This project involves six major European companies from three countries in an attempt to establish high speed GaAs VLSI circuits manufacturing capability. The availability of state of the art ICs will serve European system and equipment manufacturers in the IT and telecoms industry and help to provide them with the necessary worldwide competitive edge.

The programme will investigate in detail two active devices which are potential candidates for LSI/VLSI integration, namely MESFETs and HEMTs. They are presently in different stages of maturity, but many key technologies are shared, such as ion implantation, advanced lithography (E-beam, deep UV and DSW), dry processing and self-alignment techniques. They will be investigated in parallel, from device modeling to fabrication yield. During the four years of this programme, various key demonstrators of increasing complexity, such as counters, multiplexers, multipliers, A/D converters, SRAMs will be produced. They will provide the necessary feedback to design and technology and will help to steer the programme towards its VLSI goal.

In spite of some problems with the development of self-aligned gate technology and HEMT realization, good results have already been achieved in the design and fabrication, in more conventional technologies, of few demonstrator chips, for example:

- various designs of 1K SRAMs (1.5 ns typical access time)
- 4x4 and 8x8 multipliers (operating clock frequency > 600 MHz)
- fast multiplexer-demultiplexer. (>3 Gbits/s).

As an early result of this project, together with ESPRIT project number 232, one of the partners is engaged in the development of ICs for the next generation of super-computers. At its end, the project will demonstrate ICs of a complexity and speed that can be used as the heart of the next generation of very high speed systems (e.g. telecommunications: optical multi-gigabit links and super-computers with a cycle time of less than 2 ns).

Contact Point

Dr J. MUN
STC TECHNOLOGY LTD
London Road
Harlow
UK - CM17 9NA ESSEX

Tel: +44-279-29531 x 354
Tlx: 81151
Fax: +44-279-29531 x 3407

Participants	Country	Role
STC TECHNOLOGY LTD	*UK*	*M*

THOMSON-CSF/DCI	*F*	*P*
GEC RESEARCH LABORATORIES	*UK*	*P*
LAB DE PHYSIQUE APPLIQUEE	*F*	*P*
PLESSEY COMPANY PLC	*UK*	*P*
SIEMENS AG	*D*	*P*
FARRAN TECHNOLOGY LTD	*IRL*	*S*

Start Date: 01-01-86 *Duration: 48 months*

EUROPEAN CAD INTEGRATION PROJECT (ECIP)

Project number : 887

ECIP investigates the area of data exchange and infrastructure standards with the objective of defining and promoting standards within the European IT industry. The ability to readily interchange data and CAD tools between companies is a key area for bringing into practical reality many of the benefits of collaborative tool development in Europe and for making available the results of ESPRIT to the wider European IT community. The final goal of ECIP is the definition of a multi-layered open model for CAD systems with recommendations of rules and/or standards at each level.

Effective liaison between the ECIP project and all other ESPRIT CAD projects is being established ensuring transfer of experience in both directions. In particular, ESPRIT project 1058, which develops advanced tools, is complementary to the ECIP project. In this way it will be ensured that the standards developed in ECIP are based on a wide experience of requirements and should therefore be widely acceptable to developers of present and future CAD systems.

Following an analysis of the requirements and needs of the existing CAD systems of the partners, with particular reference to standard interfaces, together with a corresponding investigation of existing standards in the field of CAD for VLSI, the partners presented a summary of their preliminary recommendations at the first ECIP Seminar during the ESPRIT Conference in September 1987.

Although the partners represent a reasonable cross-section of the relevant European industry, importance has been attached to broadening the peripheral involvement to include other interests which cannot be directly represented. To this end, liaison has been established and joint meetings held with the other existing ESPRIT CAD projects. Representatives from many of these projects attended the first ECIP Seminar in Brussels in September 1987.

This project is central to the strategy of optimising the results of past, present and future work in the CAD Area. It will define standard interfaces which will allow tools from different projects to be interconnected and design data to be shared between a range of design systems and silicon manufacturers. In order to ensure the acceptance of such proposed standards by the appropriate industries, the results will be made widely available and potential users will be encouraged to comment on interim results.

The direct involvement of 6 major European Microelectronics Companies and the indirect involvement of many other projects will provide the basis to ensure the successful adoption of the standards on a wide scale. Some impact (adoption of interim recommendations) can be expected during the project but the main impact will be on later generations of CAD systems 5 years from now.

Contact Point

Mr H. FELIX
BULL S.A.
121 avenue de Malakoff
F - 75116 PARIS CEDEX

Tel: +33-1-45 02 95 83
Tlx: 614050
Fax:+33-1-45 02 93 07

Participants	**Country**	**Role**
BULL S.A.	*F*	*M*
CIT-ALCATEL	*F*	*P*
ICL	*UK*	*P*
PHILIPS GLOIENLAMPENFABR N.V.	*NL*	*P*
SGS MICROELETTRONICA SPA	*I*	*P*
SIEMENS AG	*D*	*P*

Start Date: 01-01-86 *Duration: 60 months*

ADVANCED INTEGRATED-CIRCUIT DESIGN AIDS (AIDA)

Project number : 888

The objective of the AIDA project is to master the complexity of VLSI chips (more than one million transistors within the next few years) by obtaining a drastic improvement in design methods. CAD tools, new methods and concepts will be defined, proved on experimental software and finally developed into industrial tools integrated into the existing CAD environments of the partners. AIDA intends to explore the application of modern programming techniques and knowledge-base engineering to CAD tool development. It will constitute a design assistant that proposes solutions rather than merely records and validates the designer's ideas. This will allow the designer to apply his creativity where it is most efficient, leading to improved design quality. Modern programming techniques will be applied (e.g. those developed for expert systems to VLSI-CAD tools). The potential contribution of these techniques is twofold :

- The basic techniques may be used to make new tools much more efficient than classical ones.

- The basic integrated circuit design knowledge may be recorded into the machine, and used by "expert" modules, under the control of a system designer.

The following seven work packages show the full span of problems tackled by the project: Data Management, Specification, Synthesis, Layout, Testing, Man Machine Interface and Evaluation.

The project started with an in-depth study and refinement of the requirements catalogues in each work area and the establishment of priorities in the different approaches towards implementation. In Data Management, particularly, the large volume and complex structure of the design data, together with the extensive range of necessary design tools and all their varied interactions, means that the requirements of CAD systems for VLSI design are probably among the most challenging of all database applications. Here the partners have concentrated on aspects of portability, exchange formats and interfaces and data security concepts, especially for CAD systems distributed over a range of interconnected computers.

During its second year the project has entered the implementation phase. In most of the work areas, the first prototype tools are expected around the end of the third year. Prompted by the need to share design data and tools between the three different corporate databases, the project has evolved a new standard for the presentation of conceptual data models.

This development is under consideration by the ECIP project (Esprit project number887) for a recommended standard.

All three partners have a large existing investment in CAD systems in house.

The project will have a significant impact on the ability of these companies to design complex chips of several million transistors. Furthermore, the partners are committed to marketing the results both as stand-alone tools and as integrated systems, thus making the results available to a much wider community. AIDA should also prove a useful test-bed for the proposed standards emerging from the ECIP Project.

Contact Point

Dr H. THONEMANN
SIEMENS AG
ZTI DES 26 — *Tel: +49-89-63 64 44 536*
Otto-Hahn-Ring 6 — *Tlx: 521092*
D - 8000 MUENCHEN 83 — *Fax: +49-89-63 64 83 22*

Participants	**Country**	**Role**
SIEMENS AG	*D*	*M*
ICL	*UK*	*P*
THOMSON SEMICONDUCTEURS	*F*	*P*

Start Date: 15-11-85 — *Duration: 48 months*

BASIC TECHNOLOGIES FOR GaInAs MISFETS

Project number : 927

Solid solution of InGaAs epitaxially grown on semi-insulating InP substrates is promising for high speed logic devices as well as for integrated opto-electronic circuits for 1300-1500 nm wavelengths. Insulated gate field effect transistors (MISFETs) can be realized on this material.

There are three objectives:

- To evaluate the influence of the InP substrate quality on the overlying devices and to improve accordingly this quality.
- To obtain a better understanding of the basic phenomena at the interface between the insulator and the InGaAs.
- To explore the possibilities of ion implantation, compared to MOCVD epitaxy for implementing active devices in this ternary compound.

Once these three aspects have been explored, technological processes for high speed logic devices and integrated opto-electronics will be optimised.

Full scale equipments for InP synthesis and for crystal pulling under magnetic field have been installed and are being tested. Large semi-insulating InP crystals (up to 3" in diameter) weighing more than 4kg have been successfully grown with low dislocation density (around 10^4 EPD.cm^{-2}).

Good progress has been achieved in growth uniformity on 50 mm wafers by MOCVD.

Besides the strengthening of European supply of InP wafers for integrated opto-electronics, this project will have investigated new active devices in the III-V family based on InP. This is of the utmost interest for the development of low cost optical communication systems.

Contact Point

Dr J. THEETEN
LAB DE PHYSIQUE APPLIQUEE
3 avenue Descartes
F - 94450 LIMEIL-BREVANNES

Tel: +33-1-45 69 96 10
Tlx: 203475
Fax: +33-1-45 69 40 88

Participants	**Country**	**Role**
LAB DE PHYSIQUE APPLIQUEE	*F*	*M*
AIXTRON	*D*	*P*
RWTH AACHEN	*D*	*P*

WACKER CHEMITRONIC		*D*	*P*
Start Date:	*01-01-86*	*Duration:*	*36 months*

HIGH DENSITY MASS STORAGE MEMORIES FOR KNOWLEDGE AND INFORMATION STORAGE

Project number : 957

The objective is to develop vertical and (reversible) magneto-optical recording technologies for mass storage of data on rotating discs. Compared with classical recording techniques, these technologies are potentially capable of providing much higher storage densities, as well as improved access times, higher storage reliability and more competitive storage costs. Vertical recording technology will be investigated and developed for both floppy and rigid discs. Topics to be addressed include media and substrates, as well as the read/write heads. Magneto-optical recording requires optical read heads and magnetic write heads. In addition to the development of basic components and technologies, work will be carried out for simulation of the mechanical dynamics, defining the internal coding of data including error correction and detection, and designing electronic interfaces to computing systems.

The specific technical objectives aimed at in the case of vertical recording are: a linear density of 70,000 fci and a radial density of 140 tpi for floppy discs, a linear density of 40,000 fci and a radial density of 1500 tpi for rigid discs. The magneto-optical system should provide a linear density of 20,000 bpi and a radial density of 10,000 tpi. In terms of the capacities, the objectives for 5.25 inch drives are 15 to 20 MB on a floppy disc, 150 to 200 MB for vertical rigid discs, and 400 to 500 MB for magneto-optical discs.

(Task I, Floppy Disks) - Despite encountering problems linked to Cr-Co tribology linear densities have been achieved as high as 120 Kbpi, however, the head-media interface still poses a major problem. Life time is still below expectation when compared with the emerging Ba-Fe technology.

(Task II Rigid Disks) - Optimization of composition is very close to the target. The main problem being in increasing the linear density from 20 Kfci to 40 Kfci. A new sub-layer has been developed and intermediate layers have been studied. Glass substrates have shown excellent mechanical and structural characteristics. 3380-like heads for vertical recording have been developed. Single pole type heads are under development.

(Task III, Magneto-optic media) - Work has been carried out on media (garnets and amorphous Rare Earth-Transition Metal alloys) and pick-up systems. Thin garnet films are regarded as possible competitors to Rare Earth Transition Metal alloys especially if they can be deposited by sputtering. Moreover the combination of a magneto-optical garnet film for read out and a ferrite layer for information storage looks very promising. Amorphous films have been shown to have suitable properties as storage media but aging occurs when the media are stored in a wet atmosphere. Optical components for a pick up system based on a new original concept have been developed and tested.

(Task IV, Simulation) - Specification of the head interface has been completed, and software tools for testing different coding schemes have been developed.

The above progress is consistent in meeting the stated objectives providing the problems indicated can be overcome.

The three major objectives of this project (vertical magnetic recording for achieving extremely high storage densities, reversible optical recording and the magneto-optic technology to achieve extremely high surface densities) are currently considered worldwide as strategic targets, and hence their achievement will place the partners in a strong, competitive position.

The first products are expected for the late eighties.

Contact Point

Dr J.P. TUAL
BULL S.A.
Rue Jean Jaures
F - 78340 LES CLAYES-SOUS-BOIS

Tel: +33-1-34 62 73 04
Tlx: 220898
Fax: +33-1-34 62 78 79

Participants	Country	Role
BULL S.A.	*F*	*M*
BASF A.G.	*D*	*P*
BOGEN ELECTRONIC GMBH	*D*	*P*
GLAVERBEL S.A.	*B*	*P*
CEA/LETI	*F*	*P*
SIMULOG	*F*	*P*
THOMSON CSF	*F*	*P*

Start Date: 01-02-86　　*Duration: 36 months*

HIGH PERFORMANCE VLSI PACKAGING FOR COMPLEX ELECTRONIC SYSTEMS

Project number : 958

The objective is to exploit the potential advantages of high density structures on which VLSI chips will be connected with very dense (100 to 125 um pitch) TAB (Tape Automated Bonding) interconnects on a high performance multi-chip substrate.

Electrical and thermal performance are to be measured to evaluate the capability of such a structure, which could be used as a basic building block of a very high performance system (1GHz clock or 20-50 ns system cycle time).

This project is complementary to Project No. 830 as part of the "Advanced Packaging" work-programme.

The first test vehicle with 125 pitch at chip and OLB (outer lead bonding) is being realised. It includes a specific non-functional chip, corresponding TAB lead frame, and substrate.

The general features of the substrate are: up to 36 chip sites, up to 8 layers, about 360 I/Os, power dissipation adjustable up to 360W, electrical non active fixtures (impedance and cross-talk measurement).

Bump topology and design rules have been established, preliminary tape design and specifications have been issued and all the necessary equipment for TAB are in place.

A method of simulation of electrical properties in high density substrate is developed in collaboration with the University of Bordeaux and of Grenoble.

The second functional test vehicle has been defined. It has been decided to build a test board using conventional packaging techniques in parallel with the advanced multi-chip substrate. Such an approach should allow the impact on the performance of the high density packaging to be measured directly by comparing results.

The main application areas for the TAB technology within the telecommunication and industrial segments are for high speed switches and processors, display drivers and high speed transmission systems. However, as the technology advances and becomes cheaper, it will probably find a wider range of applications.

For future information processing systems a packaging technique allowing the assembly of VLSI chips in compact modules, where electrical signals are closely monitored and heat can be efficiently evacuated, is needed. TAB offers these possibilities, for instance, the technology developed under this Project is planned to be used in future BULL computers.

Contact Point

Mr K. KURZWEIL
BULL S.A. | *Tel: +33-1-34 62 70 48*
Rue Jean Jaures | *Tlx: 696054*
F - 78340 LES CLAYES-SOUS-BOIS | *Fax: +33-1-34 62 78 79*

Participants	**Country**	**Role**
BULL S.A.	*F*	*M*
BRITISH TELECOM PLC	*UK*	*P*
GEC RESEARCH LABORATORIES	*UK*	*P*

Start Date: 31-01-86 | *Duration: 36 months*

THREE DIMENSIONAL ALGORITHMS FOR ROBUST AND EFFICIENT SEMICONDUCTOR SIMULATOR (EVEREST)

Project number : 962

The numerical analysis and prediction of the detailed behaviour of semiconductor devices is an important step in the development of a new process. With the advent of sub-micron feature sizes, this analysis is becoming increasingly difficult. For certain calculations one-dimensional or two- dimensional analysis is no longer sufficiently accurate. Three-dimensional analysis is only just becoming available inside certain major industries and is prohibitively expensive in computing time.

The goal of this project is to develop, for 3-D devices, a set of fully tested algorithms, initially for steady-state analysis and later for transient and small signal loading conditions. The interaction with the temperature of the crystal lattice will also be taken into account. Success in this aim implies crossing new research frontiers in non-linear numerical analysis techniques both to solve the problem reliably and within reasonable computing costs. As part of the drive to reduce computing costs, the applicability of computers with advanced architectures will be investigated. Following validation against measurements of real devices, the successful algorithms will be incorporated into computer systems in the industrial partners and in a common project research code.

On the basis of the first year's work, a reappraisal of priorities led to an effort to augment the work package which will produce the project research code. The definition of the plan for this work package has been greatly strengthened. This work culminated in delivery of the first release of the code for the solution of the initial target of the off-state 3-D problem which was demonstrated at the project review in December 1987.

Fully transient 3-D analysis at a reasonable computing cost is an ambitious goal. Even 2-D solutions of this problem are only to be found inside large semiconductor companies (predominantly US and Japanese) at this time, and it has been claimed that even these programs cannot solve all of the device problems in this category. The availability of such an analysis tool in Europe by 1990 would put Europe in a strongly competitive situation. In addition to the industrial use of the results by the companies in the project, the research project code will be available to other European research organisations for research purposes. The possibility of eventual commercial exploitation of the research code is also being examined.

Contact Point

Mr C. TROWBRIDGE
RUTHERFORD APPLETON LABORATORY.
Chilton
Didcot
UK - OX11 0QX OXON

Tel: +44-235-44 51 21
Tlx: 83159
Fax: +44-235-44 58 48

Participants	**Country**	**Role**
RUTHERFORD APPLETON LABORATORY	*UK*	*M*
ANALOG DEVICES BV	*IRL*	*P*
GEC RESEARCH LABORATORIES	*UK*	*P*
IMEC V.Z.W.	*B*	*P*
NAT. MICROEL. RESEARCH CENTRE	*IRL*	*P*
PHILIPS GLOIENLAMPENFABR. N.V.	*NL*	*P*
SGS MICROELETTRONICA SPA	*I*	*P*
TRINITY COLLEGE DUBLIN	*IRL*	*P*
UNIVERSITY COLLEGE SWANSEA	*UK*	*P*
UNIVERSITA DI BOLOGNA	*I*	*P*

Start Date: 10-04-86 *Duration: 48 months*

TECHNOLOGY FOR GaAs-GaAlAs BIPOLAR IC'S

Project number : 971

The general objective is to develop advanced aspects of GaAs/GaAlAs bipolar integrated circuit (HBTs) process technology.

Two bipolar logic technologies will be developed:

- Emitter coupled logic (ECL)
- Integrated injection logic (I2L).

Single hetero-junction (wide gap emitter, HBTs) and double hetero-junction (wide gap emitter and collector, DHBTs) will be investigated and compared. At the same time, efficient analytic switching models for these devices will be developed. A combination of numerical simulation and experimental verification will be used to ensure the validity of the analytic models for discrete devices.

The first two years will be spent on the development of high performance transistors (3 um emitter width HBTs with f_T exceeding 17 GHz) with good yield and uniformity on 2" diameter substrates. Simple integrated circuits (like divide by 2 and divide by 4 circuits) will be fabricated for operation at frequencies > 4 GHz.
During the following two years, simple front-end signal processing test circuits e.g. a 3 bit adder will be fabricated to determine applicability of HBTs for complex high speed ICs.

A divide by 4 circuit has been operated at 6 GHz. Good progress is reported for some of the advanced process steps. As a result of this project, an alternative approach for ultra high speed digital ICs could be offered to European industry.

Contact Point

Mr M. BON
CNET
196 Avenue Henri Ravera
F - 92220 BAGNEUX

Tel: +33-1-45 29 46 23
Tlx: 202266
Fax: +33-1-45 29 54 05

Participants	**Country**	**Role**
CNET	*F*	*M*
GEC RESEARCH LABORATORIES	*UK*	*P*
PLESSEY COMPANY PLC	*UK*	*P*
FARRAN TECHNOLOGY LTD	*IRL*	*S*
PLASMA TECHNOLOGY LTD.	*UK*	*S*

Start Date: 01-02-86 *Duration: 48 months*

OPTICAL INTERCONNECT FOR VSLI AND HIGH BIT RATE ICS

Project number : 986

The objective is to demonstrate the potential advantages of optical interconnection technologies over conventional electrical ones for high bit rate signals in electronic assemblies such as circuit boards and other assemblies of an equivalent integration level. To achieve this it is necessary to examine some of the technological and practical aspects of implementing optical interconnection. More specifically, the above is to be realized by the achievement of:

- A practical demonstration of optical interconnection applied to a real application providing hard data on performance, gate counts, power consumption etc. in the context of currently available technology.

- Assessment of the realistic bit rate limitations applicable to optical interconnection, the trade-offs between serial (TDM) and parallel (WDM or space diversity) and the problems encountered in transmission of unformatted data.

- The generation of practical performance data on the alternative transmission media suitable both for use in multi-mode waveguide OIC and for use in hybrid circuit assemblies.

- An evaluation of the performance and compatibility requirements for opto-electronic and VLSI device integration together with experimental assessment of selected techniques.

- Identification of application areas for optical interconnect and detailed assessment of selected options.

The design, manufacture and evaluation of an optical interconnect demonstrator comprising a significant circuit/processor function and utilising optical connection of data of up to 1GB/s is underway. This implementation is based on hybrid circuit technology, assembled on printed circuit boards and employing an optical fibre link designed to transmit data without any format restrictions (i.e. operation down to d.c.). Appropriate protocols for the signalling circuits have also been selected and interfaces to the processing functions constructed. The hybrid multiplexers and demultiplexers (16:1) have been built and have been evaluated at data rates up to 2 GB/s. Preliminary testing of the transmitters and receivers up to 1 GB/s has also taken place. Currently the modules are being assembled together and the demonstrator will shortly be evaluated as a complete entity.

Further increase of the transmission speed up to 5GB/s was investigated, the main impetus of this work being to examine the limitations on high bit rate optical links designed for operation with unformatted data. The results obtained so far indicated a limitation (less than 5 GB/s) arising from the substantial variation of the modulation sensitivity versus frequency which

makes the transmission of unformatted data very problematic. Introduction of the necessary formatting would further reduce the usable bandwidth by 1 to 2 GB/s and other solutions are space consuming and difficult to implement in the OIC context. It was therefore concluded that, except for special requirements, OIC is not attractive for bandwidths much above 2 GB/s and hence further work in this area was discontinued.

The evaluation of advanced optical interaction technologies is an important part of this project. To this end several planar multi-mode waveguide technologies (polymer, screen printed glass, plasma deposited SiO_2/GeO_2 and ion exchanged), suitable for hybrid technologies, have been assessed in detail and the demonstration of a printed optical circuit (including wavelength division multiplexing) formed using the most promising of these techniques, is to be carried out.

The inherent wide bandwidth and cross-talk immunity of optical transmission media can permit very high bit rate signals to be distributed by overcoming the transmission line and rf interference problems encountered currently with very high bit rate ICs. Additionally, many lower bit rate signals, each of which would conventionally employ a package pin, can be time multiplexed together to form one easily transmitted, high bit rate optical signal which leaves the package via one optical pin thus reducing the pin count for VLSI chips.

Contact Point

Dr S. GRATZE
GEC RESEARCH LABORATORIES.
West Hanningfield Road — *Tel: +44-245-73 331*
Great Baddow-Chelmsford — *Tlx: 995016*
UK - CM2 8HN ESSEX — *Fax: +44-245-75244*

Participants	**Country**	**Role**
GEC RESEARCH LABORATORIES.	*UK*	*M*
UNIVERSITY OF SOUTHAMPTON	*UK*	*P*
TELETTRA S.P.A	*I*	*P*

Start Date: 21-12-85 *Duration: 24 months*

MULTIVIEW VLSI-DESIGN SYSTEM (ICD)

Project number : 991

The objective is to develop a complete, integrated, open and cost effective design system usable from a large variety of intelligent workstations. The system is to be capable of mastering the complexity of the design of large integrated circuits by:

- Exploiting their geometrical and functional hierarchies in a logical and intelligent environment.

- Providing sophisticated synthesis and verification tools.

The work is an extension of project MR-09-DFT under the Microelectronics Programme 3744/81. The main topics to be covered are: functional data modelling, distributed data management, verification of submicron structures, advanced multilevel simulation as well as self-testing/fault-tolerant synthesis techniques, and the provision of tools for the verification of manufactured ICs.

Finally, the project has the explicit goal to provide an open system geared to the needs of independent designers (although it will be equally useful in a larger design environment). The system will therefore provide foundry interfaces at the various design - and test levels. It will be capable of running on intelligent, but inexpensive workstations, produced in Europe, and will provide a gateway to the increasingly sophisticated VLSI technology for electronic and system designers.

In its first half, the project has made great strides towards achieving its objectives. The functional 3-D modelling problem is essentially solved, the silicon compilation tools made available are capable of handling not only classical gate-array and macro-cell designs, but also the newer sea-of-gate structures and there are on-going releases of the cell generation system (ASTRA) and the SPIRIT system. ASTRA is a development of BTMC which has been incorporated into the system whilst SPIRIT is a commercially available package based on the work carried out in the previous project and the first part of this. A new work-package has been added to the project which will take care of generating and incorporating test-data with the hierarchical verification tools developed so far.

The project aims to achieve its objectives by clever and extensive use of internationally accepted software and designs standards which will allow the system to meet its objective to run on a large variety of commonly available work stations. This will be done by employing new concepts in database design (specifically the use of a new semantic data model) and by tailoring design tools (verification as well as synthesis or compilation tools) to fit into and make efficient use of the optimally structured data.

Furthermore, the system will offer newly conceived design tools fitting the

trend towards close-to-micron or submicron circuits, especially in the area of artwork-verification, layout-to-circuit extraction and redundancy-design for wafer scale integration.

As an indication of the impact made to date based on existing published work on the project, a recent study which compared different software frameworks for VLSI design, concluded that, of the well known ones on offer, the recommended model was the one developed within this project. (Study on Software Frameworks for VLSI Design by Queens' University, Kingston, Canada)

Contact Point

Prof. P.M. DEWILDE
TECHNISCHE UNIVERSITEIT DELFT
Mekelweg 4
NL - 2600 AA DELFT

Tel: +31-15-78 50 89
Tlx: 38151
Fax:

Participants	**Country**	**Role**
TECHNISCHE UNIVERSITEIT DELFT	*NL*	*M*
BRITISH TELECOM PLC	*UK*	*P*
TECH. UNIVERSITEIT EINDHOVEN	*NL*	*P*
ICS HOLDINGS B.V.	*NL*	*P*
INESC	*P*	*P*
PCS-PERIPHERE COMPUTER SYSTEMS	*D*	*P*
UNIVERSITY OF ESSEX	*UK*	*S*

Start Date: 01-01-85 *Duration: 36 months*

0.5 MICRON X-RAY LITHOGRAPHY: SOURCES, MASKS, RESIST AND TRANSFERRED IMAGE

Project number : 1007

The objective of this work is to achieve 0.5 micron x-ray lithography up to the actual demonstration of the lithography process. In particular, resist and mask technologies will be developed appropriate to 0.5 micron resolution while compatible with higher resolution limits. Hence, mask technology will utilize Si-based membranes which are appropriate for use with the softer (i.e. higher resolution) wavelengths.

The work is on schedule and consistent with meeting the above objectives.

Silicon Nitride membranes hare being produced of $1cm^2$ area size. Furthermore, triode sputtering has been set up for the deposition of non hydrogenated membrane materials (SiN and SiC). Since SiC appears the most promising because of its high Young's modulus, $1cm^2$ membranes have already being fabricated with 0.25 micron thickness.

High aspect ratio absorber patterns at 0.5 micron have been obtained by two alternative methods: a subtractive method and an additive method. The subtractive method is a tri-level process involving reactive ion etching of tungsten. the additive method is a single level resist process with final electroplating of gold. The two pattern transfer processes are characterized.

A novel x-ray positive resist is being finalized for production specifications. The project has the use of the two most advanced state of the art x-ray lithography systems: one based on linear fresnel zone alignment, the other on electronic elaboration of contrast image. Finally, a dedicated synchrotron radiation beam line is now operative which has also done extensive characterization of a laser plasma source.

Initial studies and demonstrations in the field of x-ray lithography have already been carried out in several R&D labs in USA and Japan but the advanced know-how from them is not readily available. At the end of this project, the potential of such a technique in terms of resolution and throughput in an industrial environment will be quantified and the know-how for a 0.5 micron process will be available.
The objectives of this project are in line with the goals of the work-programme in the silicon technology area towards sub-micron geometries in one of the most critical process steps.

Contact Point

Prof. A. TUCCIARONE
CNR/IESS
Via Cineto Romano 42
I - 00156 ROMA

Tel: +39-6-412 48 51
Tlx: 610072
Fax: +39-6-412 43 97

Participants	Country	Role
CNR/IESS	*I*	*M*
KING'S COLLEGE LONDON	*UK*	*P*
CNRS	*F*	*P*
SGS MICROELETTRONICA SPA	*I*	*P*
THOMSON CSF	*F*	*P*

Start Date: *01-01-86* *Duration:* *48 months*

ADVANCED MASK AND RETICLE TECHNOLOGY FOR VLSI SUB-MICRON MICROELECTRONICS DEVICES

Project Number : 1043

This project addresses specific areas of both E-beam and optical mask-making processes to develop new equipment, materials and processes. The objective is to combine such developments to create an enhanced mask and reticle technology to satisfy the wafer fabrication requirements for advanced and complex devices.

A prototype of a Laser Pattern Generator, the basic machine for the production of these advanced masks, has been installed and is under operational testing. Study on chrome blanks, resist technology and wet etching, both for E-beam and optical processes is proceeding successfully. Initials results on SEM inspection using low voltage equipment are very encouraging.

The work is now concentrating on the development of both wet and dry etching processes, and on the development of the suitable equipment for mask development.

Mask and reticle fabrication forms a first key step in the manufacture of integrated circuits. As VLSI circuit complexity increases, the role of mask-making becomes increasingly demanding and the quality criteria even more exacting, hence, improvements in high quality mask technology directly reflect on the competitiveness of Europe's semiconductor industry. Prototype equipment, in the form of a laser illuminator for optical pattern generators, advanced masks and reticle cleaning station, novel dry etch chrome mask equipment and possible development and production of a new electron beam resist will be made available as a result of this project.

Contact Point

Dr J. TURNER
FERRANTI ELECTRONICS LTD
Fields New Road
Chadderton
UK - OL9 8NP OLDHAM

Tel: +44-61-624 05 15
Tlx: 668038
Fax: +44-61-626 49 46

Participants	**Country**	**Role**
FERRANTI ELECTRONICS LTD	*UK*	*M*
PLASMA TECHNOLOGY LTD	*D*	*P*
BRITISH TELECOM PLC	*UK*	*P*
IMEC V.Z.W.	*B*	*P*
SIEMENS AG	*D*	*P*
VALVO BAUELEMENTE PHILIPS	*D*	*P*

Start Date: 17-12-85 *Duration: 36 months*

ULTRASENSITIVE IMPURITY ANALYSIS FOR SEMICONDUCTOR STRUCTURES AND MATERIALS

Project number : 1056

The objective is to develop an advanced physical analysis technique which is needed for the characterization of microelectronics fabrication technologies. An improvement of the standard Secondary Ion Mass Spectrometer (SIMS) will be developed, by the implementation of a laser resonator. This will result in a highly sensitive instrument suitable for multilayers profiling and free of matrix effects.

As part of the first year of work which was devoted to a feasibility study of the Laser Assisted SIMS, an extensive patent search was done by one of the partners (SIEMENS). This resulted in the knowledge that a patent had been filed in the US covering an analytical method using sputtering in combination with laser resonance ionization. Attention was then focused on finding a process that would not infringe this patent. It was concluded that if resonant laser-excitation into Rydberg states of the atoms was applied, followed by ionization due to an electric field, use of this process would probably not infringe the above or other patents. Hence this approach has been pursued.

A laser source has been purchased and is scheduled to be delivered in March, 1988. Work is progressing on the design of the chamber and in particular to define the source geometry, crucial for obtaining the best results.

Cameca has delivered a complete commercial system IMS-300 to IMEC so the latter could start immediately to evaluate the impact of the new technique.

The analytical instrumentation developed by the project will be of strategic importance for European industry as a diagnostic and control tool for contamination detection and doping profiles, both as a product and as a service tool. This instrument is not only an updating, but also a totally new conception in equipment of this type. Such an instrument is far more sensitive than those currently available and will result in a big improvement in semiconductor characterization and analysis. After a feasibility study, the machine is expected to be available in 1990. It is the intention of one partner to market the final instrument and another partner to organize a service facility.

Contact Point

Dr W. VANDERVORST
IMEC V.Z.W.
Kapeldreef 75
B - 3030 LEUVEN-HEVERLEE

Tel: +32-16-28 12 11
Tlx: 26152
Fax: +32-16-22 94 00

Participants	Country	Role
IMEC V.Z.W.	*B*	*M*
CAMECA	*F*	*P*
PHILIPS RESEARCH LABORATORIES	*UK*	*P*
SIEMENS AG	*D*	*P*

Start Date: 03-04-86 *Duration: 48 months*

KNOWLEDGE BASED DESIGN ASSISTANT FOR MODULAR VLSI DESIGN

Project number : 1058

The objective is the production of an interactive knowledge based system for verification of electrical, functional and timing correctness of flexible VLSI modules as generated by silicon compilers.

This is a complementary project with project P887.

This objective is to be met by the two major work packages of the project. Firstly, an interactive user interface and open system architecture which allows for a fluent and fast interactive communication between intelligent application tools and VLSI module designer will be produced. Secondly, intelligent application tools which are built using knowledge based concepts for allowing timing and electrical verification by analysis and intelligent simulation, will be provided.

A rule based expert system is to control the floorplanner's module assembly, it will be ported from an advanced LISP machine to a high performance engineering workstation for use in the project.

A wave-form based analysis technique will allow for "real time" user interaction supported by an advanced multi-window user interface. The adaptation of a register-transfer-functional switch level simulator to the hardware accelerator will be investigated. A knowledge-based circuit extractor will provide a link to symbolic/procedural module layout generators.

The structure procedure interface (SPI) standard is a key concept in this system architecture. It is a dynamic data passing concept to let programs communicate with each other on structural items. The SPI definition has been set up and implemented in a number of demonstrator applications, where programs are directly linked in one executable module via the SPI procedures. This illustrates that using SPI, programs can interactively communicate on structural information in order to e.g. directly highlight schematics or the symbolic layout frame within the timing verifier. More programs are to be interfaced to SPI.

Further extensions have been done on the timing verification program. The pattern recognition syntax has been re-defined. The verification of modules (as realized in ESPRIT 97) can now be done. The checking of the logical equivalence between two logic equations (tautology check) can be done. This is a basic function needed to compare logic behaviour at two levels of abstraction.

The rule-based electrical verification system has been extensively documented and its efficiency increased by two orders of magnitude; this was done by directly compiling the rule base in LISP code, the rule bases are to be generalized.

The algorithms used in the wave-form-based circuit simulator have been documented and a prototype version has been implemented and tested on the available parallel processing hardware.

A flexible, technology-independent link between verification and symbolic layout has been made so that circuit extraction for use in the verification comes directly from the symbolic layout. The extracted information is formalized in the technology description language (TDL).

A verification speed of 20,000 transistors/hr is projected. A novel wave-form relaxation switch-circuit level simulator implemented on a multi-processor hardware accelerator embedded in the system, will lead to 100...300 times SPICE performance. This will be achieved by exploiting a new explicit event oriented integration scheme and by exploiting parallelism. The research done on a SEQUENT parallel processing machine will allow for efficient and accurate simulation of 4000 transistor circuits.

As the tendency in the CAD for VLSI is moving more and more towards the concept of a platform on which CAD Tools can be built and interchanged and as this is one of the goals of ECIP, the complementary nature of this project and ECIP could result in a very competitive European approach.

Contact Point

Prof.DE MAN
IMEC V.Z.W. — *Tel: +32-16-28 12 01*
Kapeldreef 75 — *Tlx: 26152*
B - 3030 LEUVEN-HEVERLEE — *Fax: +32-16-22 94 00*

Participants	**Country**	**Role**
IMEC V.Z.W.	*B*	*M*
INESC	*P*	*P*
PHILIPS GLOEILAMPENFABR. N.V..	*NL*	*P*
SILVAR-LISCO N.V.	*B*	*P*

Start Date: *01-01-85* — *Duration:* *48 months*

LARGE DIAMETER SEMI-INSULATING GaAs SUBSTRATES SUITABLE FOR LSI CIRCUITS

Project number : 1128

GaAs Integrated Circuits are using an n-type active layer prepared by ion implantation of donors directly in semi-insulating wafers, followed by an annealing to cure the implantation damage. In order to realize LSI circuits, one must control accurately the properties of each individual FET transistor. This can only be achieved if the active layer is perfectly under control.
This project is aimed at developing an industrial approach for the preparation of large diameter (around 75 mm) semi-insulating GaAs substrates which can allow the preparation of very homogeneous active layers by ion implantation and then, at mapping the relevant properties of each individual micro-FET made on it for fast feedback on the growth conditions.

Three different goals have to be reached:

- Methods to define material homogeneity for ingots of large diameter. This will be done by correlation between results of physical characterisation made on bulk material and of device measurements on processed wafers cut from it.

- Techniques to improve crystalline quality. Two parallel and complementary approaches (iso-electronic (In) doping and/or thermal gradient flattening), will be investigated.

- Growth of ingots of large diameter of suitable quality for VLSI manufacturing using the recipes worked out previously. The target is to obtain FET threshold voltage dispersion < 15 mV over 80% of the wafer.

There has been good progress towards goals 1 and 2:

- The parameters of the thermal model developed by UCL have been adapted to the pullers available in this project.

- Ingots of 7.5cm and even 10cm diameter have been grown successfully during the first year of the project and made available to other ESPRIT participants to further check their suitability for ICs manufacturing.

- Best yield of 1K SRAMs has been obtained on wafers grown during this project.

Coupled with the large industrial experience and capability in supplying semiconductor wafers of one of the partners, this project will provide a strong European source of improved GaAs crystals. Already 3" diameter semi-insulating GaAs crystals are available in limited quantities under normal commercial conditions.

Contact Point

Dr.G.MARTIN
LAB DE PHYSIQUE APPLIQUEE
3 avenue Descartes
F - 94450 LIMEIL-BREVANNES

Tel: +33-1-45 69 96 10
Tlx: 203475
Fax: +33-1-45 69 40 88

Participants	**Country**	**Role**
LAB DE PHYSIQUE APPLIQUEE	*F*	*M*
UNIVERSITE CATHOLIQUE LOUVAIN	*B*	*P*
WACKER CHEMITRONIC	*D*	*P*

Start Date: 01-01-86

Duration: 36 months

ADVANCED PROCESSING TECHNOLOGY FOR GaAs MODULATION DOPED TRANSISTORS AND LASERS

Project number : 1270

The primary objective is the establishment and demonstration of molecular beam epitaxy structures of hetero-junctions, superlattices and GaAs device field effect transistors and laser layers based on combined laser-MBE processing.

The efforts in laser-MBE processing of GaAs MBE layers and laser processing of thin film diffusion barriers will be directly applied to process field effect transistors and lasers as test structures, which will be tested both for electrical performance and reliability. These results will be extended to a range of gallium arsenide digital integrated circuit technologies based on GaAs MESFET, high electron mobility transistors (HEMT/TEGFET) and hetero-junction bipolar transistors (HBT) as the circuit elements.

Some impressive results have already been achieved :

- GaAs HEMTs, grown by MBE, have shown 50% power efficiency at 26.5 dB output power level and 26.5 GHz.

- Other HEMTs have operated at 10 GHz with 1.4 dB noise figure and 11.5 dB associated gain.

These results are better than available commercial transistors.

In addition, some GaAs on Si hetero-epitaxial wafers have been grown and are now being processed to evaluate their quality for devices.

This project will have explored some new techniques for III-V semi-conductor processing, evaluated them and hopefully demonstrated their usefulness, together with developing adapted equipments (i.e. excimer lasers).

Contact Point

Dr.A.CHRISTOU
CRETAN COMPUTER INSTITUTE — *Tel: +30-81-23 50 14*
Tlx: 262728
GR - IRAKLIO — *Fax:*

Participants	Country	Role
CRETAN COMPUTER INSTITUTE	*GR*	*M*
CNET	*F*	*P*
ELLTEC SA	*GR*	*P*
PLESSEY COMPANY PLC	*UK*	*P*

UNIVERSITY OF WALES ABERYSTWYTH *UK* *P*

Start Date: 01-12-86 *Duration: 36 months*

ADVANCED MANUFACTURING SYSTEM (AMS)

Project number : 1551

The manufacturing process of ICs has special requirements concerning the establishment of long term strategy on software and hardware packages for its full automation. The objective is to satisfy those requirements within an advanced integrated manufacturing system concept. In particular attention is to be given to problems associated with increased fabrication complexity, small device geometries, large chip size, flexibility (process, product, equipment, facility etc.), increased yield (maintenance concept, process stability, people and process-production interactions), increased wafer diameter, new process concept, automation and fast cycle time for material.

These topics will be addressed in particular:

- Production Information System
- Networking, communication, interfaces
- Automation Island definition and experiment
- Facility monitoring system
- Material handling systems
- Manufacturing line integration
- Manufacturing requirements with emphasis on quality, service and production cost issues.

The system demonstration is expected around two automation islands - photolithography and diffusion.

During the first year of the project, comprehensive studies and requirement analyses have been carried out and reports have been delivered primarily on the following:

- Application model and functional architecture of the production information system
- Statistical process modelling
- Definition of network requirements and evaluation of software packages
- Connection of equipments with host computers
- Linkage of equipments in the photo lithography area
- Analysis and requirements for material handling systems

- Software and hardware flexibility for automated VLSI manufacturing.

An initial demonstrator has been set up in the photolithography area.

Process line integration/automation has now become one of the key factors of success in the manufacturing of commodity or specialized (ASIC) ICs.

It is anticipated that successful completion of the project and subsequent exploitation of its results will help the Community IC manufacturers concerned to improve their manufacturing capabilities. Within the activities of this project a special interest group on VLSI manufacturing standards has been set up to which other Community organizations are invited to attend. In this way it is expected to ensure harmonization and further increase the impact of the project.

This is a 4-years project, and full demonstration is envisaged for the last year (1990) to be followed by implementation. However, intermediate results could be used by industry as early as 1988.

Contact Point

Mr J.MONNIER
THOMSON SEMICONDUCTEURS — *Tel: +33-1-45 24 17 20*
101 Bld Murat — *Tlx: 204780*
F - 75781 PARIS CEDEX 16 — *Fax: +33-1-46 51 15 80*

Participants	**Country**	**Role**
THOMSON SEMICONDUCTEURS	*F*	*M*
MARCONI ELECTRONIC DEVICES LTD	*UK*	*P*
SGS MICROELETTRONICA SPA	*I*	*P*

Start Date: 09-12-86 — *Duration: 48 months*

AUTOMATIC CONTROL OF AN ASIC FABRICATION SEQUENCE (ACAFS) AS DEMONSTRATED IN THE PLASMA ETCH AREA

Project number : 1563

The objective of the project is to develop a methodology and acquire know-how for a wafer fabrication sequence control system. Because of its critical nature the Plasma Etch area has been chosen in which to implement the methodology. The work will involve several domains such as optical sensors integration for "smart" information collection, plasma etching process modelling for control and supervision purposes, communication between equipment manipulators and computers and hardware and software for real time processing. Recent powerful techniques in model identification, multivariable process control and artificial intelligence will be used to address efficiently the various control, supervision, and decision making problems related to the proposed hierarchical control structure.

Specification of the "controller" which will form the core of the system has been produced to define a common starting point for the project. This controller will implement the features needed to reach the project objective, namely automatic etch process control and equipment supervision.

The project results will be important in 3 main respects:

- Anticipated improvements of chip yields because of utilization of the methodology.
- More competitive equipment and systems.
- Implementation of standards.

Contact Point

Mr F. LEONARD
SOCIETE BERTIN
Rue Louis Armand
B.P. 22
F - 13762 LES MILLES

Tel: +33-42 60 01 11
Tlx: 420729
Fax: +33-42 60 00 13

Participants	**Country**	**Role**
SOCIETE BERTIN	*F*	*M*
EUROPEAN SILICON STRUCTURES	*F*	*P*
LEYBOLD HERAEUS GMBH	*D*	*P*
MIETEC N.V.	*B*	*P*
PLASMA TECHNOLOGY LTD	*UK*	*P*

Start Date: *01-04-87* *Duration:* *48 months*

MORE INFORMATION ?

If you require more information, please contact:

DG XIII
Division A2
Esprit Information Office

on

Tel: +32 2 235 16 03
Tlx: 25946 JEPE B
21877 COMEU B
Fax: +32 2 235 06 55

and at the

COMMISSION OF THE EUROPEAN COMMUNITIES
DG XIII/A2
Telecommunications, Information Industries and Innovation
A25 -ESPRIT INFORMATION
200 Rue de la Loi
B-1049 Brussels

or

The External Relations Unit
COMMISSION OF THE EUROPEAN COMMUNITIES
DG XIII/E5
Telecommunications, Information Industries and Innovation
J37 1/20 -Ref: ESPRIT
200 Rue de la Loi
B-1049 Brussels