COMMISSION OF THE EUROPEAN COMMUNITIES

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COMMUNITY ACTIONS IN THE FIELD OF MICROELECTRONIC TECHNOLOGY

COUNCIL REGULATION (EEC) NO 3744/81

SECOND REPORT BY THE COMMISSION TO THE COUNCIL

COM(84) 567 final

EXPLANATORY MEMORANDUM

On 7 December 1981 the Council adopted Regulation No.3744/81 concerning Community projects in the field of microelectronic technology.

Article 9 of this Regulation stipulates that each year the Commission shall forward to the European Parliament and to the Council a report on the development of the activities in the Community falling within the scope of the Regulation.

This document, which is the subject of a written procedure, is the second report on Commission activities. It covers the second call for proposals and the results thereof, the progress made in the projects started following the first call for proposals, the work undertaken to coordinate national activities and the dissemination of the results.

CONTENTS

INTRODUCTION

On 7 December 1981, the Council adopted Regulation N° 3744/81 on Community actions in the field of microelectronic technology.

Article 9 of the Regulation stipulates that the Commission shall each year forward to the Council and the European Parliament a report on the development of the activities in the Community falling within the scope of this Regulation.

The first activity report on microelectronics, submitted to the Council in October 1983 (COM (83) 564 final), encompassed the actions for the introduction of the Regulation, the various phases in the first call for proposals and its results, the reasons which led to the Commission amending the list of projects benefitting from Community support under Regulation N° 3744/81 and publishing a second call for proposals, and the work carried out to coordinate national activities and the dissemination of the results. It also covered the links between the Regulation and the ESPRIT research and development programme.

This is the second activity report to the Council which describes the second call for proposals and its results, the progress of the projects launched through the first call for proposals, the work carried out to coordinate national activities and the dissemination of the results.

EXECUTIVE SUMMARY AND SUMMARY APPRAISAL OF THE PROGRAMME TO DATE

1. The first report to the Council was covering the activity period from the begin of the programme until July 15, 1983. This report, the second, is covering the period from July 16, 1983 until June 30, 1984. It is organized in 5 sections and 2 annexes.

   Sections I and II are covering the direct support actions (projects) of the programme. Specifically, section I covers the procedure followed for the evaluation of the proposals received in response to the second call, which led to the launching of 8 new projects (6 for equipment for manufacturing VLSI and 2 for Computer Aided Design for VLSI).
   Section II presents the progress, until end of June 1984, of the 7 projects (1 for equipment and 6 for CAD) which were launched as a result of the first call.

   The report also covers the actions on the coordination of similar activities at National and Community level (Section III) and the links of this programme with other Community programmes (section IV).

   In the last section (section V) the measures taken or to be taken for the dissemination of the results of the supported projects are described.

2. After approximately two and a half years of operation of the programme, the situation is somehow different according to the technical domain of activities considered.

In the equipment domain : due to the nature of the domain and of the projects launched, (and also considering that 6 of the 7 equipment projects were launched beginning 1984 and only one in the beginning of 1983), it is rather difficult at this stage to assess the impact that may be produced.
It is expected that the successful completion of these projects will contribute to the respective Community manufacturers being able to introduce equipment of increased competitivity in the world market.
Already now the bi-directional transfer of know-how between manufacturers and users (partners) in the projects will considerably upgrade the Community technological level in this domain.

In the CAD for VLSI domain : the situation already now looks promising. The response was greater probably because CAD does not require major capital investments and is therefore easier to tackle, attracts interest from both industry and academia, and is well suited tc form collaborative projects. The 8 CAD projects have absorbed 62 % of the funds of the programme and are involving 67 Community organizations including most of the major which are having some interest in CAD for VLSI.

Through the various actions currently being taken, at this moment and presumably for the next two to three years, the Community appears to be not falling behind in the CAD domain in comparison with US and Japan.

However, this situation may not last because it is alarmingly evident that there is a lack of human resources. Universities do not produce highly qualified people fast enough and industry cannot easily find the numbers they require. The problem is increasing (it is equally evident in the CAD as in the equipment and technology domains) and unless actions are taken to solve it quickly it may become one basic cause in preventing the closing of the technological gap between the Community and other advanced countries.

I. RESULTS OF THE SECOND CALL FOR PROPOSALS

The second call for proposals was published on 19 February 1983 (1), its closing date being fixed for 29 April 1983.

In reply to this second call, the Commission received twenty-one proposals from 70 applicants in eight Member States (Luxembourg and Greece did not respond).

Ten of the twenty-one proposed projects relate to CAD (2) and eleven concern equipment, by contrast with the first call when the majority of proposals were for CAD projects (nineteen compared with six for equipment projects).

The identical evaluation procedure to that used for the replies to the first call was adopted, i.e. the Commission carried out an initial assessment in order to establish the conformity of the proposals with the Council Regulation and the call for proposals.

This first phase was followed by a detailed evaluation during which technical experts meeting in Brussels examined and discussed all the admissible and eligible proposals.

Thirteen proposals were considered eligible for financial support and the Commission submitted the results of this appraisal to the Consultative Committee at its meeting in Brussels on 27 June 1983.

Since the estimated overall cost of the projects eligible for financial support greatly exceeded the residual budget available, it proved necessary to fix priorities for the allocation of funds. The first was that projects for equipment should be given preference over those relating to CAD.

(1) OJ N° C 49, 19.2.1983, p.2

(2) CAD = Computer Aided Design

This decision was motivated by the results of the first call for proposals, since only one project relating to equipment had received financial support in that instance.

In addition, the goal of the amendment of Council Regulation (EEC) N° 3744 (1) was to increase the number of objectives fixed for R & D activities in the equipment sector in order to enable the European microelectronics industry to achieve a satisfactory balance between design and production capacity.

As a second priority, preference was to be given to projects relating to aspects of CAD which had been weakly or not at all represented, either within the framework of the first call for proposals or during the pilot phase of ESPRIT.

The Consultative Committee agreed with these guidelines defined by the Commission following an initial discussion of the appraisal report submitted by the Commission.

The technical interest and importance of many of the proposals led to lengthy discussions between the Commission and the Consultative Committee in an effort to ensure optimum allocation of the available resources. It was decided to arrange for a phase of consultation between the Commission and the different participants in the projects to be offered Community support with a view to adjusting the estimated costs of the various projects and ensuring equitable financing of the proposals selected.

(1) Commission Regulation (EEC) N° 397/83 of 17 February 1983 amending Council Regulation (EEC) N° 3744/81 in respect of the list of projects to benefit from Community support and of the Annex thereto (OJ No L 47, 19.2.1983, p.13)

These contacts led to the adoption of eight draft Decisions in respect of Community support, pursuant to the provisions of Regulation (EEC) N° 3744/81. After the Consultative Committee had delivered a unanimously favourable opinion on these draft Decisions at its meeting in Brussels on 30 August 1983, they were transmitted to the Commission.

On 24 November 1983, the Commission decided to offer the grant of Community financial support in respect of each of these eight proposals, all of which were the subject of contracts signed in December 1983.

The appropriations committed in respect of the contracts covered by the second call for proposals amount to 12 821 000 ECU. The beneficiaries of this support are :

A. IN THE EQUIPMENT SECTOR

1. Manufacturer : ASM Europe BV, Bilthoven, Netherlands

   Users : MATRA-HARRIS SEMICONDUCTEURS, INSA Lyon, PLESSEY RESEARCH CASWELL LTD

   Title of project : "Development of a refractory metal deposition process and related equipment"

   Total Community support : 1 169 000 ECU

   Starting date : 16.12.1983

   Duration : 3 years

2. Manufacturer : M.O.VALVE Company Ltd, London

Users : UNIVERSITY COLLEGE OF CORK, MOSTEK IRELAND Ltd, CII-HONEYWELL BULL

Title of project : "Development and evaluation of manufacturing equipment for the production of low cost, high reliability packages suitable for hermetic protection of integrated circuits of high pin count"

Total Community support : 942 000 ECU

Starting date : 1.1.1984

Duration : 3 years

3. Manufacturer : ELEKTRONIK CENTRALEN, Hoersholm, Denmark

Users : BRITISH TELECOM, SGS-ATES, MATRA S.A.

Title of project : "Static and dynamic burn-in systems"

Total Community support : 1 841 000 ECU

Starting date : 20.12.1983

Duration : 3 years

4. Manufacturer : ELECTROTECH RESEARCH LTD, Bristol, United Kingdom

Users : SIEMENS AG, EUROTECHNIQUE

Title of project : "MINSTREL, the development of a production orientated plasma/reactive ion etching system for all major processes"

Total Community support : 1 140 000 ECU

Starting date : 1.11.1983

Duration : 2 years

5. Manufacturer : CAMBRIDGE INSTRUMENTS LTD, Cambridge

Users : SGS-ATES, CSELT Turin, Standard Elektrik Lorenz AG, SIEMENS AG

Title of project : "Electron beam testing equipment for VLSI"

Total Community support : 966 000 ECU

Starting date : 20.12.1983

Duration : 2.5 years

6. Manufacturer : N.V. PHILIPS GLOEILAMPENFABRIKEN, Eindhoven

Users : UNIVERSITY OF DELFT, BELL TELEPHONE, SIEMENS A.G., FRAUNHOFER INSTITUT BERLIN

Title of project : "High Resolution Electron Beam Lithography"

Total Community support : 2 224 000 ECU

Starting date : 1.11.1983

Duration : 3 years

B. IN THE CAD SECTOR.

1. Principal contracting party : UNIVERSITY OF DELFT

Associates : I.C.S. Rotterdam, T.H. Eindhoven, T.H. TWENTE Enschede, BRITISH TELECOM RESEARCH LAB., P.C.S. Munich, I.C.N. Enschede

Title of project : "The cooperative development of a hierarchical VLSI design system"

Total Community support : 2 260 000 ECU

Starting date : 1.12.1983

Duration : 2 years

2. Principal contracting party : CII-HONEYWELL BULL, Paris

Associates : G.E.C. London, PLESSEY RESEARCH CASWELL LTD, UNIVERSITY OF DUISBURG, UNIVERSITY OF AACHEN, AUTOMATION AND MICROELECTRONICS LABORATORY OF MONTPELLIER (LAMM)

Title of project : "A CAD system for VLSI testing"

Total Community support : 2 279 000 ECU

Starting date : 21.2.1984

Duration : 3 years

II. STATUS OF PROJECTS RETAINED WITHIN THE FRAMEWORK OF THE FIRST CALL FOR PROPOSALS

A. IN THE AREA OF EQUIPMENT

Manufacturer : SIEMENS AG

Users : EFCIS SA, GRUNDIG AG, ITALTEL SpA

Title : VLSI TESTER 764/780

Total Community support : 6 712 000 ECU

Expected duration : 36 months

Started : January 1983

Aims and Content :

The aim of this project is the development of VLSI Testers SITEST 764 and SITEST 780. It is planned to develop other VLSI Testers based on a similar technology in order to be able to offer to the Customers a whole family of VLSI Testers.

The two VLSI Testers SITEST 764 and 780 differ quite considerably in their performance. The essential features of VLSI Testers are the bit repetition rate with the related system accuracy and the maximum number of Pins per testhead. The corresponding figures are 12 MHz and 64 Pins for the SITEST 764 and 50 Mhz and 256 Pins for the SITEST 780.

Expected Deliverables :

The users will receive prototype equipment of VLSI Tester 764 in mid 1984 and prototype equipment of VLSI 780 in mid 1985. The users' experience, obtained through the use of the equipment for testing advanced VLSI circuits, will be documented (reports). It is expected that after completion of the project the testers will be fully commercialized.

Progress so far :

Three hardware prototypes of SITEST 764 are now operational and in the final stages of testing. The system software has been largely developed. The SW/HW integration is expected to be essentially done by mid 1984.

B. IN THE AREA OF C.A.D.

1. Prime Contractors : STANDARD TELECOM LABS

Participants : STANDARD ELECTRIC LORENZ, BRITISH TELECOM, G.E.C. TELECOM, LABORATOIRE CENTRAL DE TELECOMMUNICATIONS DE VELIZY

Title : VLSI verification and compilation

Total Community support : 677 000 ECU

Expected duration : 36 months

Started : January 1983

Aims and Content :

a. to reduce the time taken to produce correct and compact custom VLSI;
b. to formalise a conceptual framework in which designers can manage to think about the behaviour of VLSI systems;
c. to provide computer aids which will help designers to progress from the behaviours conceived for VLSI systems to circuits implementing those behaviours;
d. to establish the role of verification in VLSI design.

The intention is to apply techniques of programming and advances in the theory of computing to chip hardware design. The designer will specify the behaviour of the chip as a program in a 'behaviour language', simulate the behaviour to show that it conforms to what is expected of it, and transform the behaviour into a layout which correctly implements it. The layout will be formed from cells some of which may have been constructed by the designer in a 'layout language'.

Expected Deliverables :

a. specifications of languages, calculi and user interfaces to computer aids;
b. reports by the user firms on the trials of the computer aids;
c. published technical papers;
d. programs and related documents on which to base a program product.

Once initial versions of the languages, the calculus and the computer aids have been devised, their soundness and practical utility will be examined by trying them out on real VLSI systems and verification strategies. The reports on the trials by the users will be relied on in the production of revised versions of the languages, the calculus and the computer aids.

Progress so far :

The definition of the Behaviour Language "LTS" has been completed.

The system simulator for the behaviour language has been completed. It is based on the ML language developed at the University of Edinburgh.

Two manipulation tools have been developed. The first is an interactive tool which will partition a set of boolean equations into sets which have limited interconnection. The second is the verifying editor which allows behaviour descriptions to be transformed according to the rules of the calculus underlying the language. At present only a limited set of manipulations are implemented.

On the layout side of the project leaf cell generators have been developed for PLAs and Weinberger arrays. These can be driven directly from the behaviour language.

The hierarchical structure of the behaviour description is used to generate the floor-plan of the chip.

The floor-plan and the leaf cells are used as input by the chip-assembler which creates the final chip layout. The current chip assembler has not been created by the project. A prototype version of the "Astra" system has been loaned by one of the user firms (BRITISH TELECOM) and this will be used in the initial user trials.

The user trials have started and each participating firm is describing a chip.

2. Prime Contractor : RUTHERFORD APPLETON LABORATORY

Participants : G.E.C. HIRST RESEARCH CENTRE, UNIVERSITY COLLEGE OF SWANSEA, N.V. PHILIPS EINDHOVEN, TRINITY COLLEGE OF DUBLIN

Title : Three dimensional semiconductor device simulation including transient and thermal behaviour

Total Community support : 1 774 000 ECU

Expected duration: 36 months

Started : April 1983

Aims and Content :

The aim is to develop robust and efficient algorithms to simulate either static or transient behaviour of semiconductor (silicon) devices. The behaviour of the device is modelled by solving Poisson's equation, the electron and hole current continuity equations and the heat flow equation by numerical techniques. The model includes expressions for relevant physical phenomena, e.g. band gap narrowing, field dependent mobilities, recombination mechanisms. The equations are to be solved in up to three spatial dimensions.

As well as studying the formulation and discretisation of these equations effort is directed towards improvements in non-linear equations solving, linear equation solving for sparse systems of equations and adaptive meshing techniques.

Expected Deliverables :

The end deliverables for the project will be recommended sets of algorithms for the simulation of semiconductor devices. These algorithms will be tested by more than one partner on a range of typical semiconductor problems (benchmarks). The algorithms will be described using a pseudo-code language in sufficient detail for easy implementation by other users. The communication of algorithms at this level avoids problems of machine dependence of the deliverables and difficulties in modifying existing software to take advantage of ideas generated in the project.

Progress so far :

The initial four months period of the project saw the establishment of the communication pattern between the collaborators including the initial rules for comparison of benchmark tests between the collaborators. Technical progress has been made, all the partners have developed 2D offstate codes and 2D onstate codes are either complete or nearing completion at all sites. When these are completed comparisons of the different techniques, element types, etc., used by the partners will be made. A report on the comparisons will be produced during the current reporting period. Exploration of linear algebra techniques suitable for the fully coupled solution approach has lead to some novel preconditioners for the ORTHOMIN solution technique that are well suited for semiconductor problems. These are contained in a technical report.

3. Prime Contractor : ESAT LABORATORY, KATHOLIEKE UNIVERSITEIT LEUVEN

Participants : LABORATOIRE D'AUTOMATIQUE DE MONTPELLIER (UNIVERSITE DU LANGUEDOC), N.V. PHILIPS, EINDHOVEN, SIEMENS AG, SILVAR LISCO, BELL TELEPHONE

Title : Mixed-mode behavioural verification system for MOS VLSI design

Total Community support : 587 000 ECU

Expected duration: 36 months

Started : January 1983

Aims Contents and Deliverables of the Project :
The objective of this project is the development of a prototype system for the verification of behavioral correctness and testability of MOSVLSI design.

Both the top-down Boolean design phase as well as the bottom-up electrical and timing verification phase is envisioned.
New to this system is that an expert system (DIALOG) is used to reduce the enormous amount of simulation time traditionally used in design by zooming in into potential critical trouble spots in the design (guided simulation) based on good design knowlegde.

Therefore the expert system guides two Mixed-Mode simulators.
One for top-down Boolean design covering functional, gate, switch level including assignable delay modeling (LOGMOS).
Also switch-level fault-simulation is under development.

The other simulator is a new electrical/switch level simulator based on dynamic decomposition methods (DIANA) and on segmented waveform analysis (SWAN) whereby one to two orders of magnitude higher performance and same accuracy as SPICE is envisioned.

In order to communicate with this system a user interface including a procedural structural description language (HILARICS) and a symbolic, connectivity based graphics editor as well as compaction system is developed (LUDIEC) together with procedural PLA, ROM generator (PLASCO).
The deliverables thus are in the form of the set of programs LUDIEC, PLASCO, HILARICS, DIALOG, LOGMOS, DIANA, SWAN.

Progress so far :
First phase test versions of all programs have been built and are being tested by the industrial partners. DIALOG, LOGMOS, DIANA and PLASCO have been successfully used for debugging, simulation and designing of VLSI chips. DIALOG experiments show the feasability of an expert system for guided simulation while DIANA shows performance improvements of 15...250 with respect to SPICE. The underlying principles of SWAN have been tested successfully and now detailed transistor models are being entered in it. A first version of HILARICS is being interfaced to LUDIEC and new DIALOG whereby the knowledge base is built up using a PASCAL-PROLOG like language. Tests using PROLOG are also under way.

4. Prime Contractor : IMAG/MICADO

Participants : TMC Ltd, SGS-ATES, RTC, PHILIPS SA PARIS, PHILIPS TELECOMMUNICATIE INDUSTRIE HILVERSUM

Title : CERES (cascade environment for the realization of electronic systems)

Total Community support : 4 172 000 ECU

Expected duration: 30 months

Started : February 1983

Aim and Contents:

To develop an integrated CAD system of VLSI circuits, supporting all the design stages from the initial specifications of the circuits to the production of the layout, test and documentation.

Main parts of this system :

- mixed mode simulation with a unique description language covering all the modelling levels (systems, behavioring, register transfer, logical gates, switch and electrical levels)
- fault modelling and fault simulation at different levels
- test data generation for PLAs
- logic compiler and silicon compiler
- general command and control language with integration of all the parts of the system
- graphical editor for circuit description (at all modelling levels)
- floor planner and leaf block design
- electrical modelling

The main challenge of this program is to integrate everything together around a unique internal data structure

Deliverables :

A set of reports structured in several volumes covering the following :

1) the functional architecture of the overall system together with a short description of the individual tools and pointers to the volumes containing more detailed information.
2) A set of research reports including motivations, overview of the state of the cost, result of research and suggested revenues of attack and/or prototype specification when applicable.
3) Draft use documentation with exemples on the developed languages and tools.
4) Evaluation reports on aspects of the system.

Progress so far :

At the present time, the following results have been achieved:

- first mixed mode (rtl-electrical) simulation prototypes
- first concurrent gate level simulation prototype
- PLAs unfolder for test data generation
- specification of : switch level simulator, overall command system, simulation environment, temporal profile and input waveform, description languages, syntax and semantics at all standard description levels
- research has been pursued on: functional faults, parallel and concurrent simulation, decomposition methods at electrical level, formal proofs of assertion, logic compiler.

5. Prime Contractors : CNET, CSELT, FI-DARMSTADT

Partners : CII-HB, CIT-ALCATEL, CENG-LETI, IMAG, INRIA, THOMSON EFCIS, SGS-ATES, ITALTEL, OLIVETTI, AEG-TELEFUNKEN, STANDARD ELECTRIC LORENZ, THE UNIVERSITIES OF BOLOGNA, GENOVA, MILANO AND TORINO (University of Pisa withdrew from the project), THE UNIVERSITIES OF AACHEN, BREMEN, DARMSTADT, DORTMUND, KAISERSLAUTERN AND KARLSRUHE, GMD, FRAUNHOFER GESELLSCHAFT.

Title : CVT (CAD for VLSI for TELECOMMUNICATIONS)

Total Community support : 12 000 000 ECU

Expected duration : Beginning of 1986

Started : February 1983

Main Purpose and Technical Objectives :

The overall objective of the CVT Project is to implement an integrated CAD system to be used by system designers, with particular reference to the requirements of the Telecommunication field.

From the user point of view, the main features requested to the system are :

- to be simple, that is easily accessed by system designer

- to be fast and sure, providing system designers with a way to go from high level descriptions to silicon implementations either automatically (when possible) or with the help of an intelligent assistant suggesting solutions, providing tools and verifying and comparing results.

The system proposed has a modular structure for the following reasons :

- it has to take advantage of the existing tools;
- it has to be flexible, to cope with the foreseen evolution during the time of design methodologies, application tools and supporting hardware;
- it has to be multi-user, leaving to each designer (or Company) the opportunity to assemble the system in the way which best suits his (or its) needs and constraints.

Summarizing, the CVT Project is aiming at the following main objectives :

- to define and implement the kernel of the integrated CAD system that is the design data base system and the user interface;

- to originate a complete set of tools for description, analysis and synthesis, to aid the designer during the architectural design phase, going from the initial specifications to floor plans (this is a key item towards the VLSI devices design, establishing a link between the two previously separated worlds of system designers and circuit designers);

- to define a set of coherent criteria for designing complex fault-tolerant, possibly self-repairing architectures, easy to test with the aid of functional test generators;

- to develop symbolic layout tools, which are the VLSI way to layout (as a matter of fact, from one side they provide the circuit designer with an intermediate, easy to use description of the masks, and from the other side they make easier the task of developing tools for automatic placement and routing);

- to provide device models helping both, the technologists to produce the device structures which best suits the TLC application needs, and the circuit designers to obtain effective simulators for circuits manufactured using advanced VLSI technologies;

- to start the work on knowledge based system, which if successful and when successfully integrated with the previously defined system, will give rise to a second generation of integrated CAD systems.

Dissemination :

The first CVT workshop was organised in Torino (11,12 and 13 April) and attendees from all over the Community were invited. Two more workshops will be organized in Grenoble and Darmstadt (April 1985 and 1986 respectively). Parts of work done within CVT are also presented in each CAVE workshop.

Progress so far :

The project is progressing well with only some minor delays in very few of the 36 subtasks. A major review of the project was carried out in October 1983. The result of the review was positive. Until now, 110 technical reports have been delivered and more than 30 software packages are in the production phase.

6. Prime Contractor : UNIVERSITY COLLEGE OF CORK

Participants : MICROELECTRONICS LABORATORY OF THE QUEEN UNIVERSITY OF BELFAST, ANALOG DEVICES, GEC

Title : Two and three dimensional numerical modelling of MOS devices

Total Community support : 366 000 ECU

Expected duration: 36 months

Started : February 1984

Aims and Content :

The project entails the development and application of a suite of computer programs for numerical analysis of 2D and 3D M.O.S devices.

A hierarchical range of programs will be developed, namely :

a) quasi-analytical models (micro-computer)
b) 2D static and transient, finite element and finite difference models (super mini-computer)
c) 3D static, finite element and finite difference models (super mini-computer)

The aims of the project are :

a) to develop finite element and finite difference computer programs for the simulation of 2D and 3D M.O.S. devices
b) to develop computer graphics packages compatible with and complementary to (a)
c) to develop simplified quasi-analytical computer programs for use on micro-computers
d) to apply the above programs to a wide range of M.O.S devices.

Expected Deliverables :

The deliverables shall consist of a series of reports giving :

a) details of the software developed
b) the associated algorithms and numerical techniques
c) details of application to MOS devices of the suite of programs

Progress so far :

Due to contractual problems between the partners, the contract was only signed at the end of December 1983 and the work started at the beginning of February. So far the progress is on schedule.

III. COORDINATION OF NATIONAL ACTIVITIES

Articles 1 to 3 of Regulation N° 3744/81 make provision for the setting up of an information and consultation "system" between the Member States and the Commission. The system covers all information of a scientific, economic and financial nature concerning any activities under the authority of the Member States in progress on the date the Regulation enters into force or contemplated after that date.

Because of shortage of staff when the programme was launched, the Commission felt it preferable to give priority to the direct support operations covered by the Regulation. Only recently has the Commission submitted for discussion in the Consultative Committee a proposal for a systematic approach for cross-exchange of information and concertation of activities.

In order to facilitate the functioning of the "system" established in the Regulation 3744/81, the proposal envisages a series of actions at 3 levels.
The first and second levels of actions are intended to stimulate the exchange of information between the Member States and the Commission and to provide the basic mechanism through which coordination will be (as it is hoped) self-regulated at the third level of actions, with minimum efforts from the competent services of the Member States and the Commission.

The attached annex 1 is summarising national programmes currently under way or to be launched shortly.

IV. COORDINATION OF COMMUNITY ACTIVITIES

The Commission's proposal concerning the European Strategic Programme for Research and Development in Information Technologies (ESPRIT) has been adopted by the Council on 28 February 1984 (1). This programme includes a section on microelectronics which is described in the 1984 work programme for ESPRIT adopted on 28 February 1894 (2).

The work to be carried out on microelectronics within the framework of ESPRIT represents both a continuation and an expansion of the activities undertaken pursuant to Regulation N° 3744/81 and constitutes an indispensable complement to the developement of advanced microelectronics within the Community.

(1) O.J. L67 of 9.03.1984, p. 54

(2) O.J. L81 of 24.03.1984

V. DISSEMINATION OF THE RESULTS

1. Specific measures

The dissemination of the results for the CAD projects which are granted support under the Council Regulation 3744/81 is insured within the framework of the CAVE (CAD for VLSI in Europe) workshops.
The attached annex 2 gives an overall view of the work which has been done during the 3 first workshops.

For the dissemination of the results of the CVT project (the largest CAD project supported through 3744/81) a workshop was organized in Torino (12 and 13 May 1984), where attendees from all Member States were invited. Two similar workshops will be organized in 1985 and 1986.
The nature of the equipment projects involving higher users-suppliers relationship is somehow different and, specific measures for the dissemination of the results have not been adopted on top of those envisaged through the general measures described below.

2. General measures

It has been provided in all contracts that, upon completion of the projects, the contractors will produce a separate (from the final) report suitable for publication. Publication of papers in recognized technical journals and delivery of lectures (specifically in projects were there is university participation) are additional means envisaged for the dissemination of the results.
The contractors are obliged within one year from completion of the projects to exploit commercially the results either themselves or to make them available to third parties in the Communities.

ANNEX 1

SUMMARY LIST OF NATIONAL PROGRAMMES IN MICROELECTRONICS *

BELGIUM

There is no specific programme to promote R&D in microelectronics. The state, however, has provided in a few cases investment assistance for setting up manufacturing and designing facilities for semiconductors and recently for a sizable laboratory for R&D in advanced microelectronics.

DENMARK

Until recently there was no specific programme for microelectronics but some funds where available through the ministries of Education and Industry. In a recently announced programme in order to promote the information technologies with a total budget of 1525 MDKr over four years, there is provision for support to various activities in microelectronics.

FRANCE

In addition to support offered to specific organizations (industrial and research) for expanding or setting up new facilities or for specific long term projects, R&D work on microelectronics is supported through the programme "Plan composants II", which was initiated in 1982 (as a continuation of an earlier " plan composants I") with a total budget of 5.6 billion FF over 5 years (of which 2.3 billion FF are provided by the state).

GERMANY

Support is offered in specific cases to organizations for strenghtening their R&D or production capabilities in microelectronics. A major 3 years programme (budget DM 450 million) was announced at the beginning of 1982 for microelectronic applications.

* source : ITTTF intelligence unit

A further DM 500 million was recently allocated for the period 1984-89 to develop the capability of the microelectronic industry in submicron technology for integrated circuits. A smaller programme with a budget of DM 25 million is currently under way supporting development of Computer Aided Design for very large scale integrated circuits.

GREECE

There is no specific programme to promote R&D in microelectronics. Some funds however are available for research in universities and state research centres.

IRELAND

There is no specific programme for microelectronics. Some funds are available through general, industrial and service industry grant schemes and capital funding in whole or in part. Some research in microelectronics is supported through the universities and state research centres.

ITALY

Support for R&D is offered in specific organizations. A new development programme for microelectronics (1982-87, US$ 157 million) includes an allocation for the microelectronics industry.

NETHERLANDS

Support has been mainly in financing electronics centres and through university R&D

U.K.

Two main initiatives are currently supporting R&D.

- The Microelectronics Industry Support Programme (MISP) was introduced in 1978 (5 years, £55 million) and it was renewed in 1984 (up to 1990) with a further £120 million.
- A report published in 1982 ("Alvey" report) has resulted in the setting up of the Advanced Information Technology programme (1983-88) with funding of £200 million. Part of the budget is expected to be allocated for R&D in microelectronics.

  Support to the industry is also offered through specific projects.

ANNEX 2

REPORT ON THE CAVE WORKSHOPS

(Computer Aided design for Very large scale integration in Europe)

1. Background :

The special aim of the CAVE workshops, which are held twice yearly, is to be used as one of the vehicles for disseminating the results of CAD for VLSI projects supported under the Council Regulation 3744/81. Also, the workshops are used to foster personal relationships at a technical level in order to smooth the path of future collaboration in the Community in R and D in CAD for VLSI. This is rather different from many technical workshops. In order to be successful the CAVE workshops must attract a kernel of attendees who will attend regularly so that personal relationships can be built up. There is also a smaller percentage of different attendees at each workshop to ensure fresh input of ideas. Most of the CAD for VLSI topics are covered at each workshop. The location of the workshops is rotated amongst the Member States. A technical committee comprised of representatives from all Member States is assisting the Commission in the organization of the workshops.

2. First Workshop :

It was organized in l'Aquila, Italy, on 24-26 May 1983 and it covered 5 CAD topics :

- simulation and modelling
- CAD systems
- testing
- layout and
- design methodologies

Statistical informations on the participants is given in the attached Table 1.

3. Second Workshop :

It was organized in Villard-de-Lans, France on 12-14 December 1983, and it covered 4 CAD topics :

- VLSI design workstations
- VLSI testing
- compact MOS modelling and
- autolayout

For the first time a panel session on "collaboration in CAD R and D" was also held.

Statistical informations on the participants is given in the attached Table 2.

4. Third Workshop :

It was organized in Rungsted, Denmark on 14-16 May 1984 and it covered 4 CAD topics :

- specification languages
- expert systems for VLSI CAD
- multi-level simulation and
- silicon compilation

Two panel sessions on "Portability and compatibility of CAD tools" and on "EEC funded projects in CAD" were also held.

Statistical informations on the participants is given in the attached Table 3.

5. Comments :

- In each workshop about 60 % of the presentations are on work carried-out within projects funded through the Council Regulation 3744/81.

- The workshops are proved to be very successful until now. Many requests for participation are received but increasing the number (currently around 50) of the attendees does not appear advisable.

- In the light of the above it is the Commission's intention to ensure the continuation of the workshop till after completion of all the CAD projects funded through the Council Regulation 3744/81.

TABLE 1

FIRST CAVE WORKSHOP - MAY 1983

PARTICIPANTS

Countries	UNIVERSITIES	INDUSTRY/RESEARCH
BELGIUM	1	4
DENMARK	1	1
FRANCE	2	5
GERMANY	5	4
GREECE	2	-
IRELAND	2	-
ITALY	3	6
NETHERLANDS	1	3
UNITED KINGDOM	2	6
TOTAL	19	29 /48

TABLE 2

SECOND CAVE WORKSHOP - DECEMBER 1983

PARTICIPANTS

Countries	UNIVERSITIES	INDUSTRY/RESEARCH
BELGIUM	3	2
DENMARK	-	2
FRANCE	3	15
GERMANY	5	3
GREECE	2	-
IRELAND	4	-
ITALY	3	4
NETHERLANDS	2	4
UNITED KINGDOM	1	5
TOTAL	23	35 /58

TABLE 3

THIRD CAVE WORKSHOP - MAY 1984

PARTICIPANTS

Countries	UNIVERSITIES	INDUSTRY/RESEARCH
BELGIUM	2	5
DENMARK	-	2
FRANCE	2	5
GERMANY	5	4
GREECE	2	-
IRELAND	4	-
ITALY	2	4
NETHERLANDS	4	3
UNITED KINGDOM	2	9
TOTAL	23	32 /55