

CAMAC

bulletin

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ESONE Committee

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WHAT IS CAMAC?

CAMAC is the designation of rules for the design and use of modular electronic data-handling equipment. The rules offer a standard scheme for interfacing computers to data transducers and actuators in on-line systems. The aim is to encourage common practice and compatibility between products (both hardware and software) from different sources.

CAMAC was originally defined by the ESONE Committee, a multi-national inter-laboratory organisation of data-processing experts from nuclear institutes. However, CAMAC is concerned with data-handling problems that are not specific to nuclear research and is being applied already in many other fields. Working groups of the ESONE Committee are considering further hardware and software aspects of systems for measurement and control, and maintain close liaison with similar working groups of the USAEC-NIM Committee and also with the International Electrotechnical Commission.

CAMAC is a non-proprietary specification which can be adopted and used free of charge by any organisation and without any form of permission, registration or licence action.

The CAMAC Bulletin, a publication of the ESONE Committee, disseminates information on CAMAC activities, commercially available equipment, applications, extensions and explanations of the rules.

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November 1973

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2. The CAMAC Serial Highway. A Preview. R. C. M. Barnes.

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Application Notes, Development Activities, Laboratory Reviews and Software:

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* **DEADLINES FOR SUBMISSION (issue No. 12)**

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On the cover: Aerial view of the Geneva region, Switzerland. The Annual General Assembly of the ESONE Committee was held in October 1970 at CERN, the European Organization for Nuclear Research, in the centre of this view. The white broken circle—2.2 km in diameter—indicates the underground 300 GeV accelerator now under construction.

(Photo Swissair)

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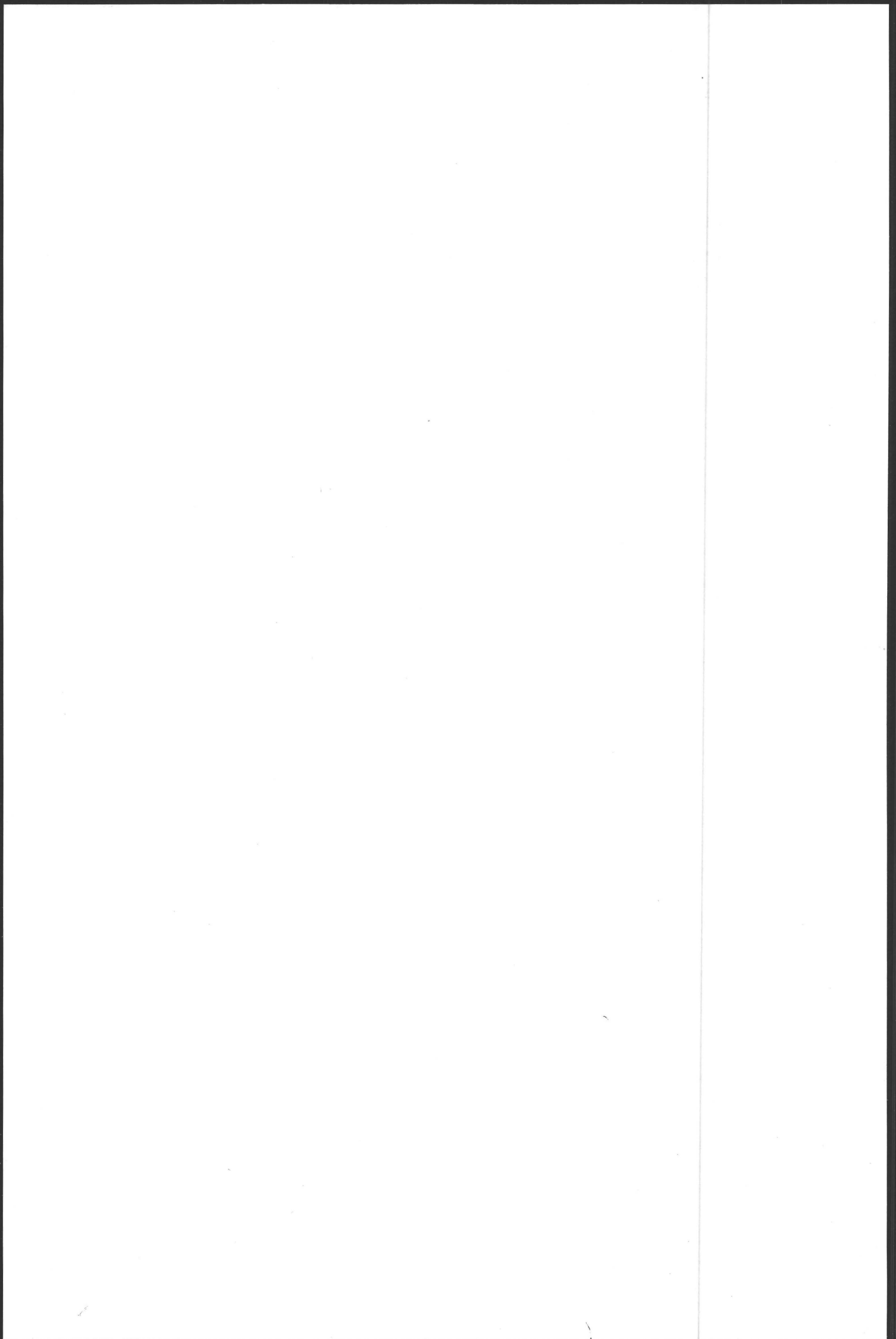
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CAMAC

bulletin

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NEWS

CAMAC FOR ENVIRONMENTAL CONTROL IN GERMANY

A large computer controlled air pollution monitoring system has been planned and prepared during the last years in Bavaria, F. R. Germany (*). The overall system will consist of one central station in Munich and eighty measurement stations situated in Bavaria's areas of urban-industrial concentration. The installation of the first fourteen measurement stations will be completed in autumn 1974.

Sensors and measuring instruments are interfaced via CAMAC at each measurement station to a mini-computer (PDP 11/10) for the acquisition and preprocessing of data and for control purposes. The measurement stations are linked via modems and the public telephone network to the central

station in Munich which is equipped with a more powerful computer (PDP 11/45) for on-line control of the overall system.

At each station the many polluting substances are measured together with meteorological parameters like wind direction and velocity, air temperature, humidity, atmospheric pressure, precipitation and solar radiation. In future also other parameters which are important for environmental control like, radioactivity, noise and water purity will be inspected by the system, being flexible and expandable due to the application of standardized hardware and software components.

* Bayrisches Landesamt für Umweltschutz, München.

FOUNDATION OF A EUROPEAN CAMAC ASSOCIATION

A European CAMAC Association (ECA) has been formed by interested people, associated with the use and supply of CAMAC facilities, at a meeting in Brussels on May 8-9, 1974. This Association will have a central role relative to more local roles of various regional CAMAC associations that are being discussed or in the process of formation, as in UK, FRG and France. The principal aims are to disseminate and exchange knowledge on CAMAC, to encourage the use of CAMAC in wider areas of application and to assist the ESONE and NIM Committees to maintain the CAMAC specifications.

An Interim Council for the ECA and working groups have been set up. The working groups are to study preferred practises in medical and industrial CAMAC applications respectively and to reinforce the activities of the CAMAC Information Working Group of the ESONE Committee.

For further information, available in the near future, contact:

Dr. H. Meyer
CCE, BCMN Euratom
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ESONE ANNOUNCEMENTS

BRANCH HIGHWAY LINES BV1-BV5, FREE LINES

In specification TID-25876 (EUR 4600e, 1972) the branch highway lines BV1-BV5 were reserved for future requirements. Various users have since found the need for additional lines, particularly in complex configurations with multiple branches and multiple sources of commands. The NIM and ESONE Committees have therefore authorized the use of lines BV1-BV5 as *Free Lines* for any use.

The specification of Crate Controller Type A (Appendix 1 to TID-25876 and EUR 4600e) is not affected by this change. No standard feature of CCA uses these lines, but they are linked between the two branch highway ports (Section 4.6). Additional features using these lines are virtually prohibited by Section A1.1.

Uses of the signal lines BV1-BV5 and their return lines BV1R-BV5R must conform to the requirements of TID-25876 (EUR 4600e, 1972). Hence,

signals on BV1-BV5 must conform to Section 7 (for example, these lines cannot be used for other types of signal or for power supplies). Any signal that is asynchronous with respect to the Branch Operation should be generated from a source that defines the transition time in accordance with Sections 4.3 and 4.4.1. It should be noted that the BV lines are terminated at one end of the highway (and preferably at both ends) as specified in Section 7.3 and Table VIII.

No standard uses are defined for BV1-BV5, and there may be conflicts between items of equipment using these lines in different ways. Designers and manufacturers with well-established conventions for the use of these lines are asked to inform the NIM Committee or the ESONE Committee, so that appropriate guidance can be given to other users.

INTERVIEWS

CAMAC APPLIED TO INSTRUMENTATION FOR ENGINE TEST BEDS

P. Claassen of AVL, Graz, Austria is interviewed by W. Attwenger

Please tell us briefly about your Company

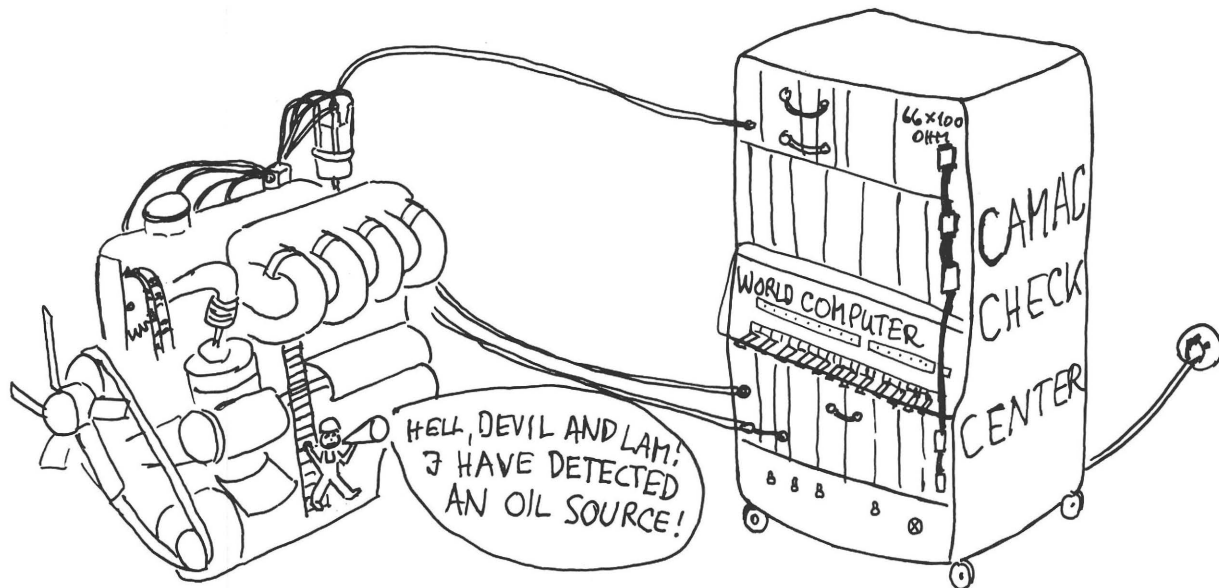
The AVL Company, of Graz in Austria, specialises in the design and development of internal combustion engines. Arising from this, we manufacture engine test systems for sale to industries and research organisations in this field. This test equipment is used for production testing (not for automating the production processes), and also in research and development.

Why did you decide to use CAMAC in your systems?

We regard computers and computer interfaces as only a means to this end of producing test systems. At first we tried to buy the computer complete with an interface to the test system. The first approach was to use the computer manufacturer's standard interfacing modules, but this

turned out to be quite difficult. Since we do not manufacture systems primarily for our own use we must be sure of a high technical standard. If it is necessary to change the computer in a couple of years we do not want to have the complication of changing the whole interface, too. Besides, we found that the computer manufacturer's standard interface modules were not always suitable for our applications, because of their techniques and costs.

Since we decided not to develop an interface ourselves, nor to accept possibly inferior facilities, CAMAC represents a good compromise. We were able to use available proved equipment, and therefore reduce the development costs of our systems. Because of the large number of CAMAC module manufacturers it is probable that we can find ready-made solutions to most problems that may arise. Of course, we have the choice of developing our



own modules, if that is appropriate. If we have to change the computer, for technical reasons or to meet the customer's requirements, it is very useful that there are crate controllers available for most well-known process computers.

For what problems do you use CAMAC?

Our main application is the testing of internal combustion engines. That involves fully automatic control and data acquisition with the help of a processor. The use of these systems for production inspection requires a very high standard of reliability.

Do you take full advantage of the modularity of CAMAC?

Since we develop systems that are generally similar, but very rarely sell standard systems, we design them in a basically modular way. So we can quite well use the modularity of CAMAC. We take advantage of the more flexible system building,

simpler servicing, and the possibility of progressive extension which the customer often needs.

Do you see advantages in a multinational system?

In a time of monetary crisis one of the reasons for deciding to use CAMAC was the advantage that it reduces our dependence on supplies from any single country. Through collaboration with SGAE we can refer to a wealth of local experience. On the other hand, customers all over the world are interested in making their own alterations to systems, and can find a wide range of compatible units on the market.

To give an example—in Eastern Europe they had experienced poor deliveries of spare parts and accessories from the West. Therefore, they like to use equipment of which there are compatible local equivalents, and may even want to change to a local type of computer. The fact that CAMAC is used in Eastern Europe is an undoubted advantage.

What are the costs of your CAMAC systems in comparison with a special solution?

The additional costs of the CAMAC system are due to the price of the crate, crate controller, and computer interface. But we cannot do without modularity, because the number of inputs and outputs varies by as much as 5:1 between different customers.

How do the initial costs of CAMAC affect its use in smaller systems?

There is a certain limit where CAMAC becomes unprofitable in small systems. On the other hand one cannot construct large systems with electronic units that are optimised for smaller systems. So we decided to stick to CAMAC as far as possible, because this simplifies the work of obtaining and using the component units of interface equipment.

Do you think that development of versatile modules is more important than development of special modules tailored for just one purpose?

This question cannot be answered in a general way. If it is economically justified it is better to develop special modules. Extreme versatility can be too expensive particularly if it increases the component count and if the modules are in quantity production.

Do you consider that the costs of meeting the full CAMAC Specifications are high (e.g. providing full decoding)?

The average cost of meeting the CAMAC Specifications in a module amounts to a quarter or third of the total, and this quite high. But we put up with these costs to achieve the flexibility of the system.

What sort of modules do you use, and what do you use them for?

Mainly we use modules for analogue and digital inputs and outputs, an interrupt module, control for a plotter, etc. We do not have well-defined tasks for modules, (they vary according to the applications).

Is the module the right size?

Yes.

Is the front-panel width a limitation for your applications?

Up to now we have had no problems, except perhaps with the single-width module which is rather narrow for some electronic components, (e.g. plug-in ICs). On the other hand one tries to avoid using double-width modules.

Would you prefer a plug for process inputs and outputs on the rear, rather than on the front-panel?

Since we construct our systems mainly for industrial applications, where changes are rare, we basically prefer wiring on the rear. This helps to avoid errors in handling and wiring. It has a better appearance, and saves the rack-height which is otherwise needed to take cables from the front-panel to the rear.

Do you think it sensible to develop special electronic components for CAMAC (e.g. for decoding and for generating S1, S2 and B)?

We would appreciate the development of components to fulfil the CAMAC Specification at a reasonable price, since this would reduce the cost of developing new modules.

How do you test your modules, by a manual controller, a computer, or special test equipment?

We test our modules in a computer system, with special test software. Besides that, the modules are tested at the limits of the temperature range.

What sort of computer do you use?

What is its size? What software do you use?

We use a 16k PDP-11, with teletype and a disc system. We have up to six displays, a plotter, paper-tape input and output, and a printer. We write our real-time software as far as possible in Assembler, thus optimising the use of the computer. This is only possible because of our small spectrum of applications. Software which need not be altered often and is not process-bound we write in FORTRAN.

Could you possibly use your CAMAC system without a computer?

At the moment we do not have any applications without a computer.

What disadvantages do you find with CAMAC?

We are of course conscious of the penalties of CAMAC. The flexibility and computer independency are obtained in return for some increase in complexity of the software and basic hardware. For our new analogue scanner, which scans and reads into the computer at 1MHz, we of course could not use CAMAC, but had to connect it directly to the Unibus of the computer.

What would be your main applications for a serial CAMAC system?

Suitable applications for serial CAMAC systems would be those where remote processes must be controlled by a central unit, and where data must be transferred with high reliability but rather slowly. But it is a question of costs whether it is cheaper to use serial CAMAC or a miniprocessor as an intelligent terminal which could relieve the load on the central unit.

What ways do you see of introducing CAMAC to a wider range of uses?

Reactions similar to ours might well be found in the so-called 'OEMs', as well as in major industrial concerns who construct their own processor systems. They therefore appreciate uniform technical standards and, particularly, supplies of compatible equipment. System manufacturers in industry could accept CAMAC more easily if the initial costs of a CAMAC system could be reduced by using more units that are in quantity production.

Would you choose CAMAC again for other problems?

As a result of our experience we would use CAMAC again.

APPLICATION NOTES

CAMAC APPLIED TO THE EVALUATION AND DEVELOPMENT OF MICROPROCESSOR SYSTEMS

1

by

D. L. Abbott and H. J. Ringel

Zentrallabor für Elektronik, KFA, Jülich, Germany

Received 14th February 1974

SUMMARY CAMAC is used as a flexible interface to develop systems based on microprocessor integrated circuits. A computer and CAMAC provide a tool for evaluating the microprocessor while it is connected to real I/O hardware, debugging microprocessor software and, finally, loading programmable ROMs. The work is aimed at developing a programmable crate controller for the CAMAC Serial System.

INTRODUCTION

As an initial step in the development of a programmable crate controller^{1,2} based on a microprocessor integrated circuit, techniques were developed for testing and evaluating microprocessor chips using CAMAC. This allowed us to gain experience in using these chips in an orderly, step-by-step manner.

HARDWARE

The system consists of an Intel 8008³ microprocessor, and its supporting circuitry, connected to a Borer type 1031 Input/Output Register.

Figure 1 is a simplified block diagram of the interface to the I/O module. The CAMAC crate is controlled by a PDP-11/40. The basic idea is to use the CAMAC computer system to 'emulate' the microprocessor's memory. In this way, much of the power of the PDP-11's software is available for developing and testing microprocessor programs. At the same time, a preliminary working system can be constructed and tested with a minimum of hardware assembly. In contrast to pure software simulation, this permitted connection to real CAMAC hardware at a relatively early stage.

Operation consists of the microprocessor issuing a 16-bit memory address, including two bits for cycle control, which is strobed into the I/O register by the EXTERNAL STROBE signal. This raises a LAM which results in the input register being read by the PDP-11. The program in the PDP-11 decodes the cycle control bits to determine whether a read memory, write memory, or I/O cycle operation is requested.

In the case of read memory, the requested byte is read from a buffer containing microprocessor code

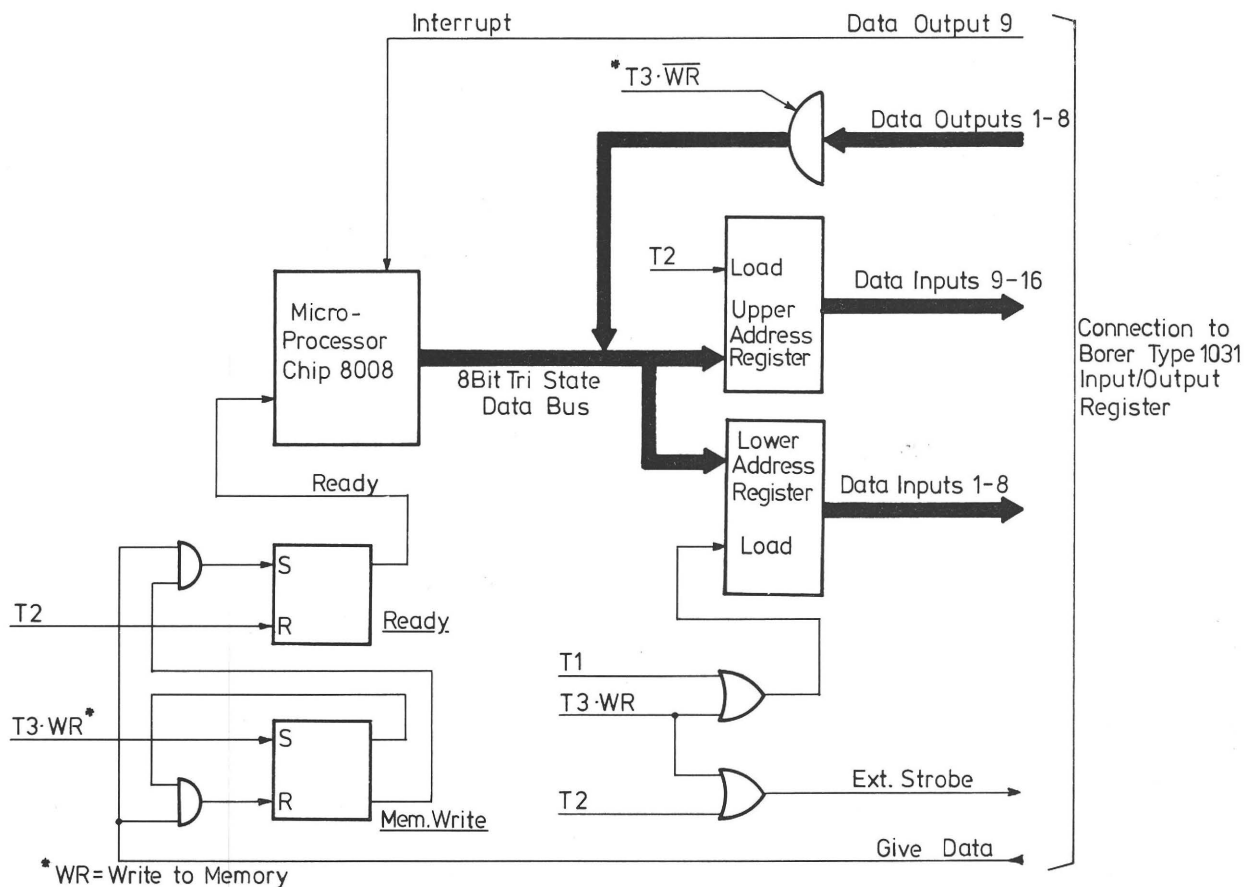


Fig. 1 Intel 8008 Interface to CAMAC I/O Module

and data, and written to the 1031 output register. A GIVE DATA command notifies the microprocessor that the requested byte is available. For writing to memory, the program issues a GIVE DATA command immediately after decoding the write cycle. The microprocessor then loads the byte into the input register, causing another LAM. The PDP-11 program reads this byte and stores it in the buffer at the requested address.

Input/Output instructions are handled in the same basic way. The program decodes the cycle as an I/O instruction and transfers a byte of data as required to or from the appropriate I/O buffers in the PDP-11.

An interrupt facility is provided by using bit 9 of the output register as the interrupt request, mainly for starting the processor from the halt state.

The whole procedure is based on the fact that the Intel microprocessor chip is able to operate asynchronously with respect to memory³. During phases T1 and T2 of a memory cycle, the processor outputs the memory address. If, at the end of T2, the READY input is not asserted, the processor enters a WAIT state until READY is once again asserted. It then completes the remainder of the cycle (T3, T4 and T5) and starts again. This also makes it relatively simple to implement a single cycle or single instruction execution mode for testing.

The CAMAC controlled set-up is also useful when a semiconductor memory is added to the microprocessor board. Bits 9, 10 and 11 of the output register are used to designate functions for loading and reading memory. In this way, program development and debugging can still be carried out using the PDP-11.

As a final step in this process, programmable read-only memories (PROMs) can be programmed by connecting the vendor-supplied programming circuitry to the I/O module. A PDP-11 program writes the microprocessor code buffer into the PROM and then reads it back to assure correct programming.

SOFTWARE

Microprocessor code is assembled using a cross assembler consisting of macros written in MACRO 11, the PDP-11 macro assembler. The assembled and linked code can be accessed and used by PDP-11 programs performing the tasks mentioned above—memory emulation, RAM loading and monitoring, or PROM programming.

The PDP-11 programs were initially written in interpretive BASIC under DOS (Disk Operating System), and after successful operation were converted to macro assembler programs under DOS. Consequently all the features of the DOS system (editor, debugger, etc.) are available for microprocessor program development.

The macro-based cross assembler permits the definition of higher level macro sets in microprocessor code. In this way, CAMAC macros for the programmable crate controller can be written in IML (CAMAC Intermediate Language) syntax.

This approach to design and development, in close connection with a computer system, seems to be especially valuable when tasks like PROM writing and program testing change into routine work. Clearly, the same techniques can also be applied to any of the microprocessor chips on the market or in development. It is only necessary to provide the appropriate interface logic to an I/O module, and a set of macros to implement the microprocessor's instruction set.

REFERENCES

1. Abbott, D.L., Microprocessors and CAMAC-Modular Peripheral Interfaces with Distributed Intelligence, COMPCON 74, Digest of Papers.
2. Halling, H., CAMAC Serial System with Programmable Crate Controller. Nuclear Science Symposium, Nov. 1973 (to be published in *IEEE Transactions on Nuclear Science*).
3. MCS-8 8008 Users' Manual, Intel Corp., Nov. 1973 (Rev. 4).

ESONE ANNOUNCEMENTS

CAMAC SERIAL SYSTEM

The document 'CAMAC Serial System Organisation — A Description' has been prepared as a basis for a formal specification. It is available on request from the ESONE Secretariat as ESONE/SH/01 (or from the NIM Committee as TID 26488). As stated on the inside front cover of ESONE/SH/01, announcements concerning corrections and amendments will be made from time to time by the ESONE Committee. The first such announcement 'Addenda and Errata to the CAMAC Serial System Organization Description' has now been approved by the Dataway Working Groups of the ESONE and NIM Committees. It will be available

in Europe from the ESONE Secretariat as ESONE/SH/02. This announcement covers various errors, omissions and ambiguities that have been investigated by the Working Groups as a preliminary step towards producing the specification.

All who are making serious use of the information in ESONE/SH/01, or intend to do so, are strongly advised to request the Addenda and Errata, ESONE/SH/02, from the ESONE Secretariat, giving their names and full mailing addresses. Members of the ESONE Committee and Dataway Working Group will receive this document automatically.

A MULTI-USER DATA NETWORK FOR COMMUNICATION BETWEEN COMPUTERS

by

H. Verelst

ISR Division, CERN, Geneva, Switzerland

Received 26th November 1973

SUMMARY Independent computers are linked via a 500 kBaud transmission loop. Any computer can seize control and address a message to any other computer. The interface between each computer and its associated modem is a double-width CAMAC message processor module providing intermediate storage, code conversion and error checking.

INTRODUCTION

This system has been developed in support of the research carried out on the intersecting storage rings (ISR) at CERN. The first aim has been to provide the experimenters, engaged in nuclear data taking, with machine data available from the main control computer. Another goal is to return information about the beam behaviour to the control room. The facility could also be used to exchange data between two research teams.

These research teams, coming from all over the world, stay at CERN for limited periods and are equipped with a variety of computers; fortunately all have some CAMAC hardware.

In the ISR the research teams are distributed along the 1 km machine circumference.

These considerations led to the use of a common, closed transmission loop, accessed by each computer through a CAMAC interface.

Design work commenced towards the end of 1971, the first computer-computer communication being achieved during the summer of 1972. The network has been operational since early 1973.

SYSTEM

The basic configuration of the system is given in Fig. 1. Computer A can begin by transmitting a message and once finished, pass control to Computer B, which, if it has something to say, will seize the loop control for the necessary time period and subsequently pass control to C. If a port has nothing to say, nothing is done and control passes on to the first port on the loop which does have something to say. Such a system has the advantage that it needs no common control whatsoever and can accommodate further computers very easily. The transmission loop consists of a data pair and a control pair. The control pair differs from the data pair, in so far as the first port is provided with an inverting line receiver (all others are non-inverting). The closed control loop therefore acts as a cable oscillator. A positive transition followed by a negative transition travels along the control pair, reaching each port in succession. When a positive transition occurs, the message processor (CMP) is allowed to open the control loop before the transition is sent out again. The transition is 'blocked' at this particular port, which now has control over

the loop for the time period necessary to transmit its message. When the transmission is completed, the loop is closed again and the 'stored' transition passes on to the next port.

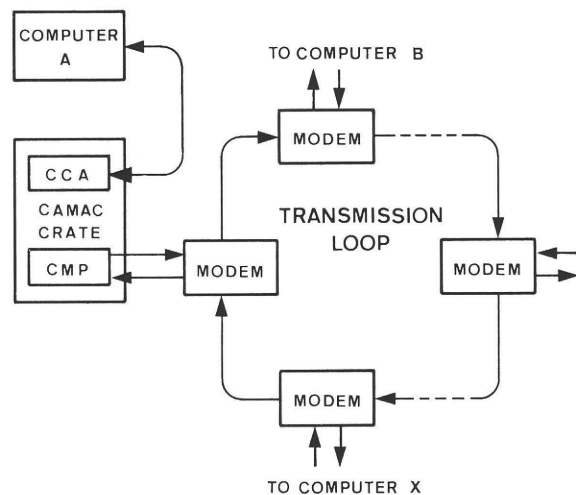


Fig. 1 Block Diagram of the Data Network

To transmit a message a computer passes it to an associated message processor (CMP). The message is segmented in 'packets' of 48 bytes. The identification of the destination is attached to each packet and the whole is passed on. As soon as the packet and the attached identifying information are stored, transmission may be 'enabled' and the message processor, then on its own, transmits at the first opportunity. In a first phase the transmitting port seizes control over the common loop and establishes a duplex link with the called processor, exclusive of all the other stations in the loop. It checks the identity of the correspondent, verifies if its own address has been correctly received and asks if the correspondent is ready to accept the message.

If all these tests are positive, the packet will be sent in a second phase of the transmission. The receiving CMP performs an error check, stores the packet and acknowledges the reception. At this moment the transmitting processor informs its computer of the correct transmission of the packet or, if not, why this transmission has not been successful (parity error, busy correspondent etc.).

Now the third phase starts: the communication is interrupted, all other stations are freed again, and control passes on to the next station. The original computer can load the next segment, or repeat the previous one, or send another message with another destination or just do nothing. In the receiving processor a Look-at-Me is set up. If the

identifying information attached to the packet specifies so, the receiver is disabled and the stored message protected until the host computer enables it again. If not, the stored packet can be overwritten and updated through the link without any intervention of the host computer.

CAMAC MESSAGE PROCESSOR

The ISR 8101 message processor (Fig. 2) is a double width CAMAC module. It contains two buffer memories (16 words by 24 bits), one for transmission and one for reception. Each of the buffer memories is either controlled by the host computer, or attached to the loop. In the former

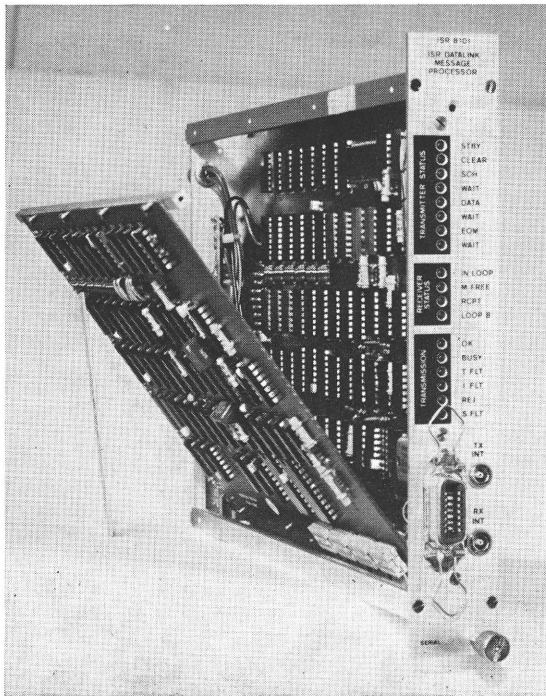


Fig. 2 The CAMAC Message Processor

case the host can write into, or read from it, but transmission is inhibited and no message will be accepted (memory BUSY). In the latter case the

host computer is only authorized to watch its associated buffer stores and to switch them back again into the first state at a suitable moment but transmission can go on and messages are accepted from the loop.

Seen from the computer, the two sections of the CMP are independent. For example one can receive a message from the loop while the other is loaded by its host computer or one can transmit on the loop while in the meantime the contents of the receiver section are read.

Input and output signals are TTL compatible, and transmission over a long cable requires an associated MODEM.

GENERAL CHARACTERISTICS

- Block size: 16 words by 24 bits
- Time-shared transmission loop (max. 256 ports per loop)
- Automatic loop control without priority
- Transmission mode: 500kBaud, serial asynchronous
- Guaranteed data rate at each port: 300kBaud/N (N: number of attached computers)
- Hardware correspondent identification and fault rejection

MODEM

A very simple MODEM has been developed using a 'bridge-type' 100 ohm output impedance line driver and a 100 ohm input receiver using a fast photocoupler (HP 5082-4360). The 'non-return to zero' signals provided by the CMP are directly transmitted on the loop. When the CMP is not connected to the MODEM, the latter acts as a simple repeater.

REFERENCES

1. den Herder I., Sbrissa E., Verelst H., Vree W., The ISR Data Network. CERN-ISR-CO/71-59.
2. ISR-8101 Message processor. CERN Handbook.
3. SYSTEM ISR 1521. CERN service manual.

BULLETIN ANNOUNCEMENTS

REPRINTS OF INTRODUCTORY PAPERS ON CAMAC

Reprints are available, on request, of the following papers, which can serve as introductory reading on CAMAC. The price per copy, in Belgian francs, is given in brackets and equivalent amounts in other currencies are acceptable.

1. *An Introduction to CAMAC*
L. Costrell, Washington, USA (B.Fr. 20)
2. *The Fundamental Principle of CAMAC*
H. Bisby, AERE, Harwell, England (B.Fr. 30)
3. *CAMAC Hardware*
F. Iselin, CERN, Geneva, Switzerland (B.Fr. 20)
4. *CAMAC System Configurations*
H. Klessmann, HMI, Berlin, Germany (B.Fr. 40)

5. *The Need for CAMAC Software*
I. N. Hooton, AERE, Harwell, England (B.Fr. 10)
6. *Introduction to CAMAC Software*
I. N. Hooton, AERE, Harwell, England (B.Fr. 20)

The papers are reprints from:

CAMAC Bulletin, no 2 for reprint 1.
Proceedings of the 1st International Symposium on CAMAC in Real-Time Computer Applications, Luxembourg, Dec. 1973 for reprint 2 to 6.

Orders should be addressed to:

Commission of the European Communities
D.G. XIII
29, rue Aldringen
Luxembourg

PROPOSAL FOR A CAMAC SYSTEM MEASURING TRIDIMENSIONAL COORDINATES

by
I. Török

Euratom Joint Research Center, Ispra, Italy
(on leave from Institute of Nuclear Research of the Hungarian Academy of Sciences, Debrecen, Hungary)

Received 20th February 1974

SUMMARY The use of CAMAC is recommended for measurements of volume coordinates and for positioning purposes. As an example, a possible measuring arrangement for the coordinates of a microscope is described briefly.

A semi-automatic digital coordinate measuring microscope has been developed in the ATOMKI (Institute of Nuclear Research of the Hungarian Academy of Sciences, Debrecen, Hungary). The system was specifically for measurement of recoiled proton tracks in nuclear emulsions, for neutron spectrometry, but can be used for any three (or less) dimensional coordinate measurements. The project started in 1967 and developed a special non-CAMAC electronic system. A description of the operation of this system follows, and it is then shown how it could be implemented in CAMAC.

NON-CAMAC SYSTEM

The system counts the forward and backward pulses from three linear incremental optical encoders (type LID II, manufactured by the firm J. Heidenhain, Traunreut, BRD) mounted on the microscope, and displays the coordinates of the microscope stage relative to an arbitrary reference point. The operator controls the movement of the stage and resets the system to the reference point. On receiving a signal from the operator, the system punches the X, Y and Z coordinates (5 decades each) in paper tape. The tape also contains control signals so that a telex machine can type out the coordinates from the tape. The system can punch, in the same format, a 15 digit label or arbitrary characters. (The former can be set by the operator on decimal preset switches, and the latter by a binary switch register, bit by bit). The system can punch three different special two-character labels for indicating special points (e.g. the beginning of a track) or errors. The system counts the labelled points and one type of error signal (non-valid track). Using two preset counters (which start to count at the labelled points, and give audio signals at appropriate count intervals) the operator can evaluate the measured pattern.

IMPLEMENTATION IN CAMAC

Today, such problems lend themselves to the application of CAMAC, and almost all the CAMAC units needed by such a system are available commercially. A possible arrangement for the above tasks is shown in Fig. 1. This arrangement gives the additional possibility of computing the track length and the proton and neutron energy, and of producing a histogram on the XY recorder. These tasks were not attempted in the non-CAMAC

system, where the data were transferred on paper tape to a computer for deriving the neutron spectrum. So the conclusion is that a CAMAC system (which can be assembled by the user from commercial modules, and which includes a com-

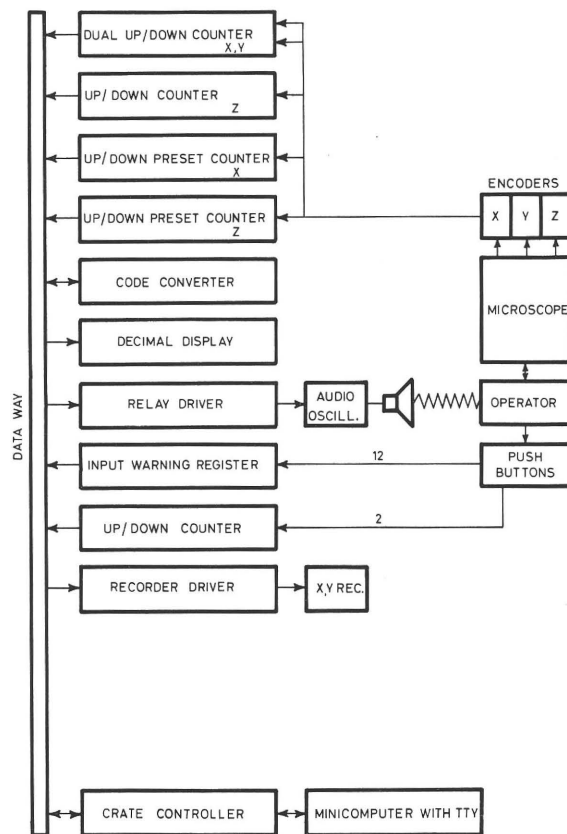


Fig. 1 A possible Measuring Arrangement

puting facility) is much more versatile than a special purpose wired program system. The time needed to insert the CAMAC control commands into the program (which is needed anyhow for processing the data) is much less than the time needed to develop a big complicated hardware system.

As a first approximation the only modules needed are the up-down counters for coordinates, and the input and output registers for the operator (marked by a vertical line in the Figure). All the other tasks can be done by software and by using the computers teletype. One computer can serve several measuring microscopes. Similar systems can be used for any coordinate measurement or positioning purposes.

MEMBERSHIP OF THE ESONE COMMITTEE

This list shows the member organisations and their nominated representatives on the ESONE Committee. Members of the Executive Group are indicated thus*.

International	European Organization for Nuclear Research (CERN)	<i>F. Iselin*</i>	Geneva, Switzerland
	Centro Comune di Ricerca (Euratom)	<i>L. Stanchi</i>	Ispra, Italia
	ESONE Secretariat	<i>W. Becker*</i>	
	Bureau Central de Mesures Nucléaires (Euratom)	<i>H. Meyer*</i>	Geel, Belgique
	Institut Max von Laue - Paul Langevin	<i>A. Axmann</i>	Grenoble, France
Austria	Studiengesellschaft für Atomenergie	<i>W. Attwenger</i>	Wien
	Inst. für Elektrotechnische Messtechnik an der T.H.	<i>R. Patzelt*</i>	Wien
Belgium	Centre d'Etude de l'Energie Nucléaire	<i>L. Binard</i>	Mol
Denmark	Forsøgsanlæg Risø	<i>P. Skaarup</i>	Roskilde
England	Atomic Energy Research Establishment	<i>H. Bisby*</i>	Harwell
	Culham Laboratory	<i>A. J. Vickers</i>	Abingdon
	Daresbury Nuclear Physics Laboratory	<i>B. Zacharov</i>	Warrington
	Rutherford High Energy Laboratory	<i>M. J. Cawthraw</i>	Chilton
	University of Oxford	<i>B. E. F. Macefield</i>	Oxford
	University of York	<i>I. C. Pyle</i>	Heslington
France	Centre d'Etudes Nucléaires de Saclay	<i>P. Gallice*</i>	Gif-sur-Yvette
	Centre d'Etudes Nucléaires de Grenoble	<i>J. Lecomte</i>	Grenoble
	Laboratoire de l'Accélérateur Linéaire	<i>Ph. Briandet</i>	Orsay
	Centre de Recherches Nucléaires	<i>G. Metzger</i>	Strasbourg
	Laboratoire d'Electronique et d'Instrumentation Nucléaire du Centre Universitaire du Haut Rhin	"	Mulhouse
	Laboratoire des Applications Electroniques de l'Ecole d'Ingénieurs Physiciens	"	Strasbourg
Germany	Deutsche Studiengruppe für Nukleare Elektronik c/o Physikalisches Institut der Universität	<i>B. A. Brandt</i>	Marburg
	Deutsches Elektronen-Synchrotron	<i>H.-J. Stuckenberg</i>	Hamburg
	Hahn-Meitner-Institut für Kernforschung	<i>H. Klessmann</i>	Berlin
	Kernforschungsanlage Jülich	<i>K. D. Müller</i>	Jülich
	Gesellschaft für Kernforschung	<i>J. G. Ottes</i>	Karlsruhe
	Institut für Kernphysik der Universität	<i>W. Kessel</i>	Frankfurt/Main
Greece	Demokritus' Nuclear Research Centre	<i>Ch. Mantakas</i>	Athens
Hungary	Central Research Institute for Physics	<i>J. Biri</i>	Budapest
Italy	Comitato Nazionale Energia Nucleare (CNEN)	<i>B. Rispoli*</i>	Roma
	CNEN Laboratori Nazionali	<i>M. Coli</i>	Frascati
	CNEN Centro Studi Nucleari	<i>F. Fioroni</i>	Casaccia
	Centro Studi Nucleari Enrico Fermi	<i>P. F. Manfredi</i>	Milano
	Centro Informazioni Studi Esperienze	<i>G. Perna</i>	Milano
	Istituto di Fisica dell'Università	<i>G. Giannelli</i>	Bari
Netherlands	Reactor Centrum Nederland	<i>A. T. Overtoom</i>	Petten
	Instituut voor Kernfysisch Onderzoek	<i>E. Kwakkel</i>	Amsterdam
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Romania	Institutul de Fizica Atomica	<i>M. Patrutescu</i>	Bucaresti
Sweden	Aktiebolaget Atomenergi Studsvik	<i>Per Gunnar Sjölin</i>	Nyköping
Switzerland	Schweizerische Koordinationstelle für die Zusammenarbeit auf dem Gebiet der Elektronik	<i>H. R. Hidber</i>	Basel
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LABORATORY REVIEWS

CAMAC IN THE NUCLEAR PHYSICS LABORATORY OXFORD

1

by

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Nuclear Physics Laboratory, Oxford, England

Received 18th February 1974

SUMMARY Nuclear physics research at the laboratory includes nuclear structure studies based on two Van de Graaff accelerators. For data acquisition from these experiments there is a CAMAC system with two branch highways, coupled through a system crate to two computers (PDP-10 and PDP-7). In addition there are serial data links to programmable stand-alone CAMAC systems.

INTRODUCTION

The Nuclear Physics Laboratory of the University of Oxford is involved in studies over the whole energy range of current nuclear research. It is partitioned into two major fields of interest. The first, high energy nuclear physics involving largely bubble and spark chamber measurements, is centred around the accelerators at CERN, the Rutherford Laboratory and NAL Batavia. The second is largely centred on nuclear structure investigations using the Van de Graaff accelerators in Oxford.

The analysis of the high energy physics data is based for the most part on a system¹ which automatically scans bubble chamber film and is controlled by a PDP-10 computer system. While it is anticipated that CAMAC will, in the future, form the vehicle for further instrumentation in the high energy physics activities, it is currently little used in this field in Oxford. In contrast, the data collection and storage facilities for the nuclear structure work are almost completely based on a CAMAC system. The CAMAC system is connected to a dual computer system comprising PDP-10 and PDP-7 computers.

OXFORD NUCLEAR STRUCTURE CAMAC SYSTEM

The presence of two computers and two accelerators has demanded a data collection system capable of being used on both accelerators and/or both computers simultaneously. It is basically a two branch system (EUR 4600e). To allow the possibility of each computer driving both branches and to provide fail safe back-up facilities it has been necessary to provide a switching mechanism between the two computers. This has taken the form of a 'System Crate' similar to that used at the Rutherford Laboratory². In the system crate, which is electrically identical to the normal CAMAC crate, transfers between system units have been introduced by using the read highway for further control lines and the write highway as a read-write bus structure. The presence in the system crate of a priority sorter together with branch drivers and interrupt vector modules (Fig. 1) enables both computers to talk to modules within the branch system.

The PDP-7 simulator through which the PDP-10 is connected to the CAMAC system in Fig. 1 will shortly be replaced by a direct PDP-10 connection to the System Crate via a PDP-10 source.

Within the two branches there exist crates dedicated to special purposes. In both branches crate 7 conforms to normal CAMAC (EUR 4100e) specifications, but is dedicated to collecting nuclear structure data from analogue to digital converters. These usually encode within a few microseconds a pulse relating to the energy of a particle detected in a nuclear counter. Since more than one particle is often detected in coincidence, this data collection mechanism operates in a multi-parameter mode, where more than one parameter is collected per event. To save computer overhead the incoming encoded ADC data is collected within the crate in dual 8×24 bit word buffers, and the data read in to the computer in a correlated sequential form. The presence of dual buffering for each ADC at the crate level very significantly improves the data rate that can be handled with a given efficiency. For example, if the total read time for a single CAMAC operation were 2 microseconds, a data input rate of 500,000 events per second would produce 50% losses. With the buffering facility used and the same input data rate this loss is reduced to 5% and, because the output from the buffer is de-randomised, very little overhead is required to service this data. In consequence the

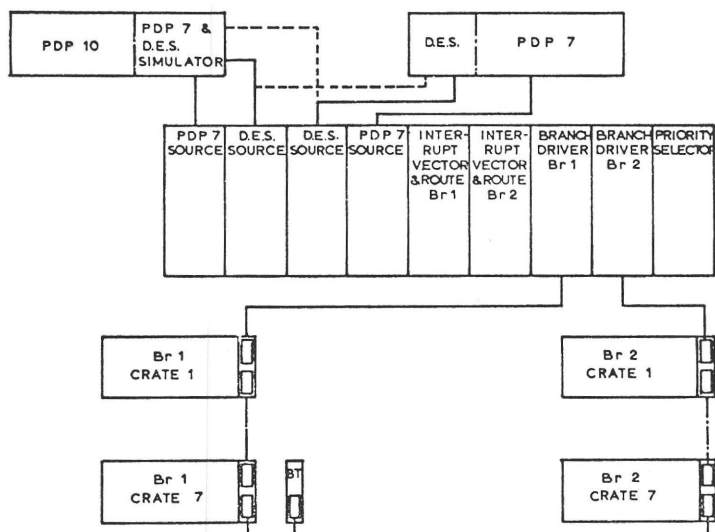


Fig. 1 The System Crate with Two Branch Highways.

The DES source handles the special purpose multiparameter Crate 7.

activity on the branch highway is under much better control. Because this is a special, well-defined activity, modules and software can be designed to exploit this type of data flow. When the interrupt vector modules find a branch demand and then the specific type of graded L representing a full CAMAC buffer, they route the computer interrupt to a special service routine. Figure 2 shows the arrangement of the channel buffer units and ADC's used in the multiparameter system.

GENERAL PURPOSE CAMAC

In addition to these multi-parameter crates there are crates for general-purpose CAMAC activities. These are intended for control applications and relatively slow data rates. Examples are stepping motor controls and scaler read-outs. These general-purpose crates (and the multi-parameter crates) are presented to the users as standard peripherals on the PDP-10. In consequence they can be assigned to a user and used in high level languages (FORTRAN, ALGOL). Accessing them through

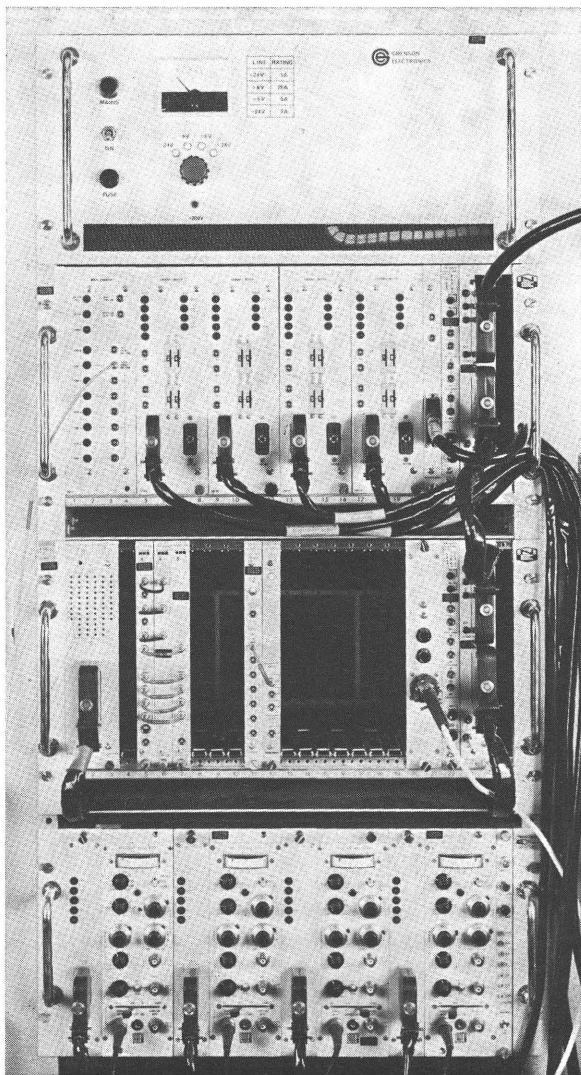


Fig. 2 The Special Purpose Crate.

This contains 4-channel buffer units, connected to the ADC's at the bottom of the Figure.

high level languages imposes a software overhead, greater in ALGOL than in FORTRAN. There is an additional monitor overhead because this PDP-10 is a multi-access system, and each user's devices and programs have to be protected from other users. As a result, a single read CAMAC operation takes approximately 1 millisecond. Additional facilities are provided for block transfers synchronised by L and/or Q. In these modes multiple read times are of the order of 100 microseconds.

OTHER CAMAC SYSTEMS

Stand alone CAMAC systems using 7025 programmed dataway controllers have also been used³, largely for repetitive dedicated control operations in the accelerators. For this purpose a special assembly language was written for the PDP-10. In addition we have two serial links operating at one megabaud³. These are unusual in a sense that they are asynchronous, the clock being stopped when an 8-bit character has been received. In this manner it has been possible to produce a full duplex connection between the computer and a serial controller which was a simple teletype module with the clock-rate changed.

DATA ANALYSIS

The data collected on the Nuclear Structure CAMAC system is analysed, simultaneously with data collection, on the PDP-10 while the PDP-7 computer is dedicated to data capture. The PDP-10 system is currently formatted to handle 30 active jobs. There are 24 terminals attached to the system.

SOFTWARE

Much work has been done in the Laboratory on the use of IML language for CAMAC. In particular several versions of the macro assembler syntax have been implemented⁴. More recently we have implemented a subroutine version of IML⁵. We anticipate that IML will be the major mechanism for communication to CAMAC.

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CAMAC MODULES FOR PHYSICS EXPERIMENTS

by

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R. Dulski, T. Koba, I. F. Kolpakov, A. P. Krjachko, N. M. Nikitjuk,
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Received 6th November 1973

SUMMARY A range of CAMAC modules has been developed for on-line data acquisition and processing. The modules are here divided into classes according to their applications, and the main technical characteristics are given. Various system configurations are shown.

A series of CAMAC modules and controllers has been developed to provide data acquisition from physics experiments, data processing and transfer into the computer¹. All these units have been designed to the CAMAC standard.

The units can be sub-divided into the following classes according to applications: converters, registers and scalars, interfaces and displays, controllers, generators and branch modules.

CONVERTERS

These include following units:

- Converter of logical levels Type 303 matches the logic levels of TTL integrated circuits and a BESM-4 computer.
- Analogue-to-digital converter Type 332 converts analogue signals into a digital code. The maximum conversion time is 70 μ sec for 8 bits.
- Digital-to-analogue converter Type 341 converts a 6-bit binary code into an analogue signal. The conversion time is 10 μ sec.
- Digital-to-time converter Type 351 uses a 1 MHz quartz oscillator, a 10-bit binary preset scaler and a 6-decade divider with preset division coefficient.
- Binary-BCD code converter Type 371 converts binary numbers into a BCD code. The conversion time of a 24-bit binary code is 10 μ sec.

REGISTERS AND SCALERS

These comprise the following units:

- Binary scalars Type 411 and 413. The capacity is 24 bits and the maximum counting rate is 70 MHz.
- Double binary scalars Type 412 and 413 each consist of two binary scalars with 16-bit capacity. The counting rate is 20 MHz.
- Preset scaler Type 431 is designed to provide preset time intervals or variable digital delay by means of an 8-decade scaler with a floating point digital display.
- Parallel input register Type 441 can store 16 independent signals. The duration of the input signals is 15 nsec.

INTERFACES AND DISPLAYS

These contain the following units:

- Relay control register Type 501 switches electrical signals by means of electromagnetic relays. The number of channels is 16.

- Parameter units Type 511 and 512 are used for manual data setting and subsequent transfer into the computer.
- Decimal display Type 521 is used for visual indication of 8 decimal digits.
- Digital voltmeter interface Type 531 is used for data transfer from a commercial digital voltmeter via the Dataway.
- Printer interfaces Type 541 and 543 are used for recording digital data on a 4 lines/sec parallel printer.
- Punch interface Type 542 is used for recording digital information on 8-hole punched tape using ASCII code with parity check.
- BESM-4 computer interface Type 581 is designed for on-line use with the BESM-4 computer in conjunction with a Type 603 crate controller. The unit accepts and sends control signals and 24-bit data words via the controller.
- Dataway display Type 591 is an auxiliary unit indicating the presence of logic signals on the Dataway lines. It is possible to generate signals L, Q, X and combinations of 24-bit digital information on the Dataway.

CONTROLLERS

These consist of the following units:

- Type 601 controller for TPA-1001 computers. This interfaces a CAMAC crate to a programmed channel of the TPA-1001 computer. Data transfer is initiated by the computer, which requests a crate for a flag.
- Type 603 controller for BESM-4 computers controls the units in a single crate and is used with a Type 581 interface.
- Type 604 controller for HP2116B computers is used for transferring digital data between the units in a single crate and the HP2116B computer. The controller is connected to the computer by means of two interface cards. For a multicrate system it is connected through a Type 821 branch driver.
- Type 611 controller for TPA-1001 computers interfaces a CAMAC crate to a programmed channel of the TPA-1001 computer. Control is achieved by means of input/output commands, as for computer peripherals, or by decoding function codes generated by the computer.
- Type 631 manual controller is used for manually controlling the units in the crate. By means of push-button switches it is possible to set a function, sub-address and other CAMAC commands.
- Type 641 program controller is used for controlling the units in a single crate. The controller provides the program for a specific mode of

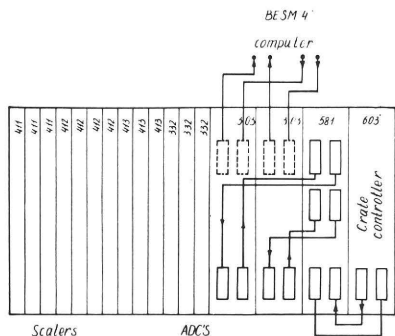


Fig. 5 Single Crate System with On-line Interface for the BESM-4 Computer

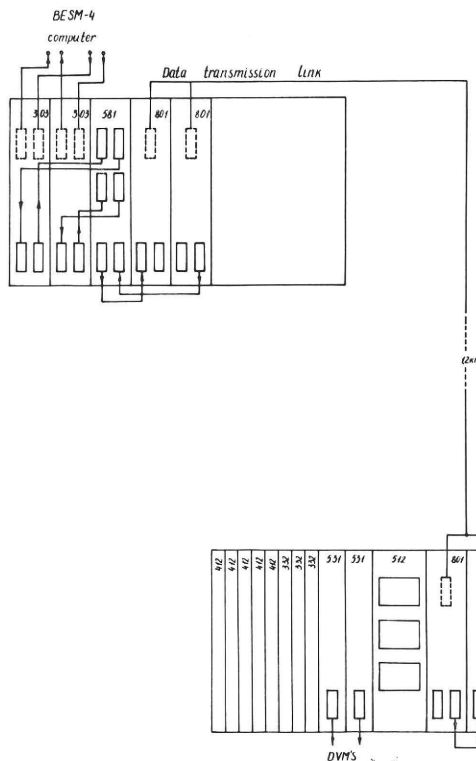


Fig. 6 CAMAC-BESM-4 System with a Long Distance Data Transmission Link

REFERENCE

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NEWS

CAMAC APPLICATIONS IN NUCLEAR MEDICINE AT VANDERBILT PRESENT STATUS AND FUTURE PLANS

CAMAC has been used for data acquisition and control of nuclear measurement systems in the Vanderbilt University Nuclear Medicine Laboratory for approximately two years. Data are acquired from three types of devices. These include a stationary multi-probe system, a computer-driven scanner and a dual-probe scanner not under computer control. Future extensions of the system include the collection of data from higher data-rate instruments (Anger-type scintillation camera) as well as computer networking.

The CAMAC system required a higher initial dollar investment when compared to a single dedicated scanner interface. However, it provided a much more versatile and more easily expanded

system. The use of CAMAC has been defended successfully on a cost basis alone, when a second device was added.

The CAMAC standard allows the replication of systems by laboratories without the large investments in time and money usually needed to interface specialised measurement systems to computers, and its modularity permits orderly growth of systems and protects against obsolescence.

The laboratory at Vanderbilt plans to use CAMAC for all applications where data-transmission-rate requirements permit and hopes that users in the non-nuclear field will come to utilise CAMAC in their measurement and data reduction systems where similar benefits should be obtained.

ESONE ANNOUNCEMENTS

2nd INTERNATIONAL SYMPOSIUM ON CAMAC IN REAL-TIME COMPUTER APPLICATIONS

A second CAMAC Symposium will take place in Brussels, middle of October 1975.

First information together with a call for papers has been distributed already as part of an invitation letter attached to issue 9 of CAMAC Bulletin.

For further information contact:

H. MEYER
c/o Commission of the European Communities
CRC-CBNM
B-2440 Geel-Belgium.

NEWS

HOW TO CONTACT CAMAC WORKING GROUPS

Everybody who is interested in further information on the activities of the CAMAC Working Groups or who would like to obtain advice for the application of CAMAC specifications is invited

to contact the appropriate chairman or secretary of the existing working groups. The corresponding addresses are given below.

ESONE-CAMAC WORKING GROUPS

ESONE-CAMAC Dataway Working Group (EDWG)

Chairman: R. Patzelt, Technische Hochschule Wien, 1040 - Wien, Gusschausstr. 21, Austria.

Secretaries: R. C. M. Barnes and I. N. Hooton, both of Electronics and Applied Physics Div., Building 347.2, AERE Harwell, Didcot, Berks. OX11 ORA, England.

ESONE-CAMAC Software Working Group (ESWG)

Chairman: I. N. Hooton, see above.

Secretary: H. Halling, Kernforschungsanlage Jülich GmbH, Zentrallabor für Elektronik/NE, 517 Jülich, Postfach 365, Germany.

ESONE-CAMAC Analogue Signals Working Group (EAWG)

Chairman: Th. Friese, Hahn-Meitner-Institut für Kernforschung Berlin GmbH, 1 Berlin 39, Glienickestr. 100, Germany.

ESONE-CAMAC Mechanics Working Group (EMWG)

Chairman: F. H. Hale, Electronics and Applied Physics Div., Building 347.2, AERE Harwell, Didcot, Berks. OX11 ORA, England.

ESONE-CAMAC Information Working Group (EIWG)

Chairman: H. Meyer, CBNM Euratom, Steenweg naar Retie, 2440 Geel, Belgium.

NIM-CAMAC WORKING GROUPS

NIM-CAMAC Dataway Working Group (NDWG)

Chairman: F. A. Kirsten, Lawrence Berkeley Laboratory, University of California, Berkeley, Ca. 94720, U.S.A.

Secretary: S. J. Rudnick, Argonne National Laboratory, P.O. Box X, Oak Ridge, Tennessee 37830, U.S.A.

Serial Systems Sub-group

Chairman: D. R. Machen, Los Alamos Scientific Laboratory, University of California, LAMPF/MP-1, Los Alamos, New Mexico 87544, U.S.A.

Systems Compatibility Sub-group

Chairman: D. Horelick, Stanford Linear Accelerator Center, Stanford University, P.O. Box 4349, Stanford, California 94305, U.S.A.

NIM-CAMAC Software Working Group (NSWG)

Chairman: R. F. Thomas, Jr., Los Alamos Scientific Laboratory, Los Alamos, New Mexico 87544, U.S.A.

Secretary: W. K. Dawson, University of Alberta, Dept. of Physics, Edmonton, Alberta, Canada.

NIM-CAMAC Mechanical and Power Supplies Working Group (NMWG)

Chairman: L. J. Wagner, Lawrence Berkeley Laboratory, University of California, Berkeley, California 94720, U.S.A.

NIM-CAMAC Analogue Signals Working Group (NAWG)

Chairman: D. I. Porat, Stanford Linear Accelerator Center, Stanford University, P.O. Box 4349, Stanford, California 94305, U.S.A.

DEVELOPMENT ACTIVITIES

A BRANCH HIGHWAY DRIVER FOR THE CII-C90-40 COMPUTER

by

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Received 11th February 1974

SUMMARY A Branch Highway driver for the CII-C90-40 computer is described. It is designed to control up to seven crates, and to transfer data by the programmed input/output channel of the computer.

This paper describes a branch highway driver for the CII-C90-40 computer used in a 1 GeV spectrometer experiment. The branch highway driver conforms to the EUR 4600 CAMAC Specification and is connected to the programmed input/output channel (24-bit data word) of the computer.

An input/output operation needs the following sequence: i) One instruction which selects the peripheral address. ii) One parallel input or parallel output instruction for the 24-bit data. One instruction to test the status of the selected peripheral unit. Only 32 of these instruction codes with 12 address bits are free for the branch driver. These are encoded to give five function bits (F). The 12 bits of the address are shared thus: C (3 bits), N (5 bits), A (4 bits).

The branch driver is principally composed of:

- CNAF registers to store the information from the address selection and status test instructions.

- WR data registers to synchronize the branch timing and the input/output timing of the computer. The branch driver has also alarm devices, which are connected to the interrupt system of the computer.
- The waiting time limiter circuit (WTL). This circuit is connected to the BTB signals from the addressed crates and generates an interrupt to the computer when it has not received the BTB response before a fixed time.
- The non-connected addressed crates circuit (NCAC) which acts before the CNAF is stored in the register.

The on-line crates connected to the branch are indicated by light-emitting diodes on the front panel of the branch driver. This information can also be read by the computer. The BD demand is directly connected to the interrupt system of the computer. The BG line is not used because each LAM can be connected directly to the interrupt system. The BQ line is connected to the response line of the status test instruction. BQ and BX are also stored and can be tested later by a special status test instruction. The branch driver allows a multi-addressing mode. Fig. 1 shows the block

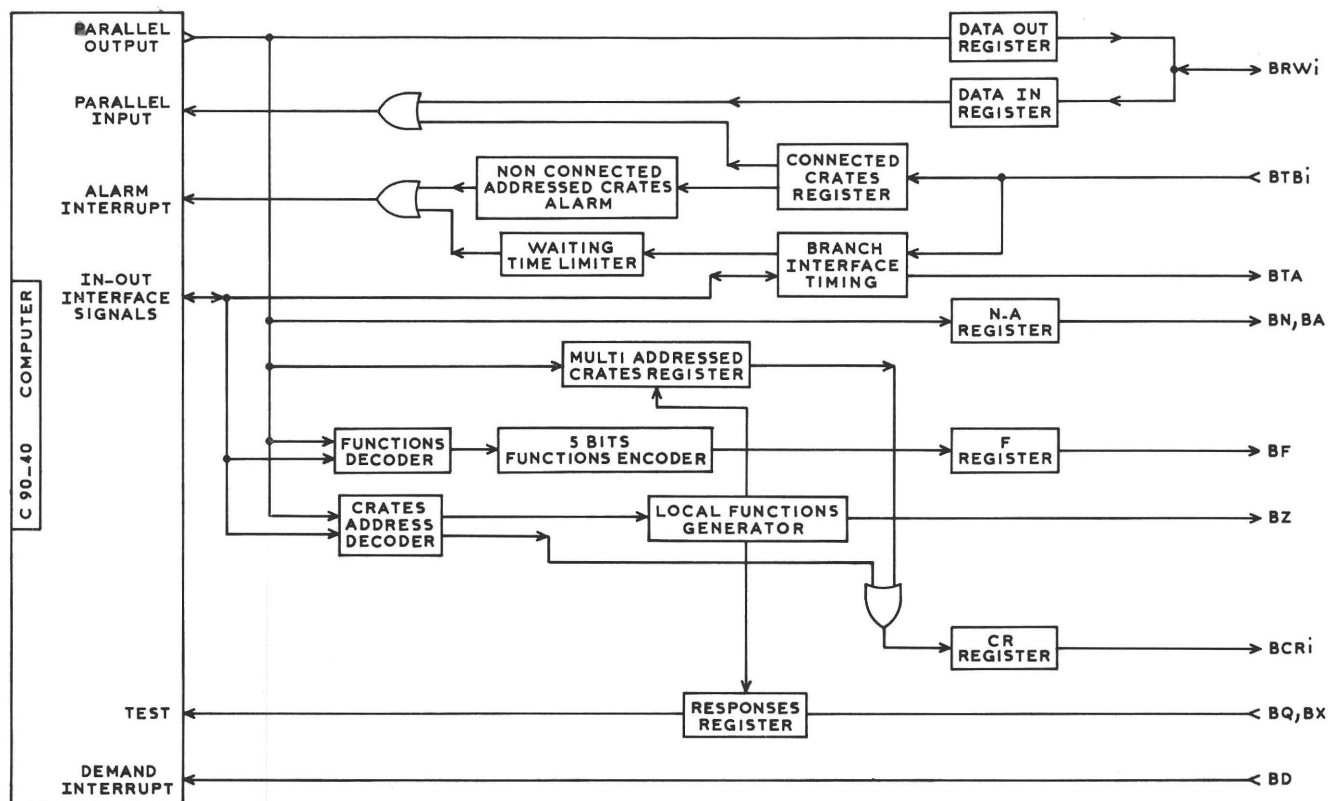


Fig. 1 Block Diagram of the Branch Driver

diagram of the branch driver. It is built in CAMAC mechanical format and is housed like a module in a CAMAC crate. It has no connection with the Dataway except for the +6 volts power supply. It is composed of 4 cards with wrapping sockets for integrated circuits.

The specialised functions of the branch driver have the crate address C(0) in their CNAF. They are as follows:

- Read the on-line connected crates: F(0).C(0)
- Reset the alarm systems:
NCAC: F(12).C(0)
WTL : F(14).C(0)
- Load the crate configuration for the multi-addressing mode:
F(20).C(0).Crate configuration
- Tests of:
Stored BX : F(27).C(0).A(1)
Stored BQ : F(27).C(0).A(2)
NCAC status: F(27).C(0).A(4)
WTL status : F(27).C(0).A(8)
- BZ command: F(30).C(0)

The distance between the experimental area and the computer room is about 85 meters. A pair of

differential branch highway trceivers (SCHLUMBERGER, JBHT 10) is used.

The branch driver in CAMAC format is situated in the first crate of the branch highway in the computer room. This crate is useful for program debugging and for testing our special home-made CAMAC modules. The system organization is shown in Fig. 2.

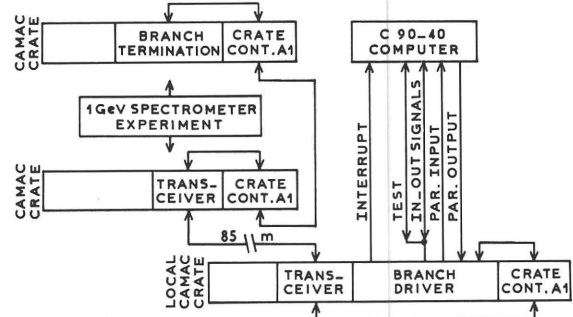


Fig. 2 System Organization

BULLETIN ANNOUNCEMENTS

PREPARATION OF CONTRIBUTIONS

Authors are requested to follow these instructions when submitting contributions for the Bulletin. Failure to do so may result in contributions being returned to the author for re-submission in a modified form, and may delay publication.

1. English is the preferred language. Contributions in other languages are equally welcome but only the summary will be translated.
2. Authors should state their name, business affiliation and postal address on a separate sheet if not included in the contribution.
3. The style, layout, use of bibliographic references and so on should follow as closely as possible the appropriate contents of this Bulletin.
4. For contributions to the New Products Section, each product description should be on a separate sheet and **any one description must not exceed 250 words or 1/3 Bulletin-page, including illustrations.**
5. For contributed articles, 1 200-1 600 words are preferred. **They must not exceed 2 000 words or 3 Bulletin-pages, including illustrations.** They

should be accompanied by a summary (abstract) suitable for translation into other languages and preferably not exceeding 50 words.

6. Manuscripts should be typed on alternate lines on only one side of the page.
7. Drawings and photographs should be included if they are relevant to the text. Original ink (not pencil) drawings and semi-mat prints of photographs, at least twice the final size, should be submitted. The author's name and the figure number should be written, lightly, in pencil on the back of each illustration. A list of all figure numbers and captions should be included on a separate sheet, even if these are given in the text or on the illustrations themselves.
8. Articles which are shortened, or adapted from, original papers should identify the original in the references.
9. **Authors must submit contributions before the closing dates** announced elsewhere in this Bulletin.
10. Reprints can be ordered at any time, but authors who are likely to require reprints in bulk should request these when submitting a contribution.

NEWS

ANNOUNCEMENTS BY CAMAC MANUFACTURERS

BORER ELECTRONICS AG is preparing 3 computers systems with CAMAC for monitoring and evaluation purposes at voltage transforming sites of big electrical power stations in Germany.

Each system will handle about thousand different

digital measurement values and some hundred analogue values for which the applied CAMAC systems are including 48-bit input registers, relaimultiplexers, ADC's, I/O registers ATC.

The computers applied are PDP-11-40.

'SHIFT'—A SERIAL HIGHWAY INTERFACE FOR TELETYPES

by

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Received 14th February 1974

SUMMARY A simple adaptor using standard MOS-LSI chips permits a conventional teletype port on a computer to act as a driver for the CAMAC Serial Highway. The adaptor performs the functions of delimiter byte insertion and deletion, clock generation, parity generation and checking, and level shifting.

INTRODUCTION

A convenient method of operating the recently defined CAMAC Serial System^{1,2} in its bit-serial mode is to use a standard teletype port as the Serial Driver. This requires some form of adaptor between the port and the two ends of the unidirectional serial loop, to perform the following four functions:

- *Delimiter Byte Insertion and Stripping:* The Serial Highway requires that WAIT delimiter bytes be transmitted by the driver between command messages in order that demand messages can propagate around the loop. To relieve the software of the burden of generating and receiving these delimiters, this should be done by the hardware.
- *Clock Generation:* Teletype ports are genuinely asynchronous (no bit-clock). Therefore, in order to provide the bit-clock for the Serial Highway, the adaptor must synchronize outgoing data to an internally generated bit-rate clock and transmit this to the Serial Highway. It must be able to correct for phase and small frequency differences between its internal clock and the clock generating the asynchronous data output.
- *Parity Generation:* Since at least some popular teletype ports do not generate transverse parity, this should be included in the adaptor. Also, at the receiving end, parity checking should be included.
- *Level Shifting:* The teletype port output—TTL, or RS-232 (CCITT), or current loop—must be translated to the signal standards of the Serial Highway (differential current drivers) and at the receiving end, translated back to the appropriate teletype signal.

IMPLEMENTATION AND DESCRIPTION

MOS LSI chips for serial transmission and reception greatly simplify the implementation of such an adaptor. While these chips are limited to about 40kHz data rate, this is not seen as a limitation since newer Teletype ports like the DEC DL11 also use MOS, and software considerations in these

interrupt-driven, programmed I/O systems will probably limit the data rate to the same order of magnitude anyway.

The teletype adaptor shown in Fig. 1 is designed around two MOS chips from Motorola, the MC 2257 L Terminal Transmitter and MC 2259 L Terminal Receiver. The present version is built on a wire-wrap board occupying a double width module (a printed circuit version will fit in a single width module). It consists of two nearly identical sections distinguished principally by their sequencing logic. Each section exists in one of two states, defined by its DELIM (delimiter) flip-flop, depending on whether the previous byte received and retransmitted was or was not a delimiter.

On the output side, the transmitter repeats on the Serial Highway every byte received from the teletype port. Odd parity is inserted in the eighth bit of each byte. Additionally, when the OUTPUT DELIM flip-flop is set, the last byte received (a delimiter) is continuously retransmitted as long as the asynchronous input line is idle. Thus the computer need only generate one delimiter between messages, and SHIFT expands this to a sequence of delimiters. When a start bit is detected on the input line, the transmitter completes its current byte and waits for the next byte from the receiver.

On the input side, the transmitter repeats to the teletype port every byte received from the Serial Loop while the INPUT DELIM flip-flop is reset, or when INPUT DELIM flip-flop is set and the current byte is not a delimiter. Thus, when SHIFT receives a sequence of delimiter bytes it passes only the first to the teletype port. Odd parity is checked by the receiver and the parity error flag is inserted in bit eight of the outgoing character. Note that the parity-error flag is ANDed with bit 7 to detect a delimiter since delimiters are defined as having correct parity.

Clock Synchronization: The requirements for clock frequency adjustment are determined mainly by the needs of the asynchronous data receiver. In order that a ten-bit character (START bit, 8 data bits, STOP bit) can be received correctly, the receiver's clock must not drift more than 1/2 bit time over ten bits with respect to the asynchronous data clock. This implies a frequency tolerance of $\pm 5\%$. At the byte level, frequency differences are compensated by the internal buffering of the receiver chip plus the addition or deletion of extra STOP bits and bit pauses, as necessary, in the retransmitted data stream.

The clock generator is crystal driven with a reference frequency of 4.9152MHz. Binary dividers and a rotary switch provide a selection of data rates from 9600b/s down to 150b/s. An external clock input at 16 times the data rate may also be selected.

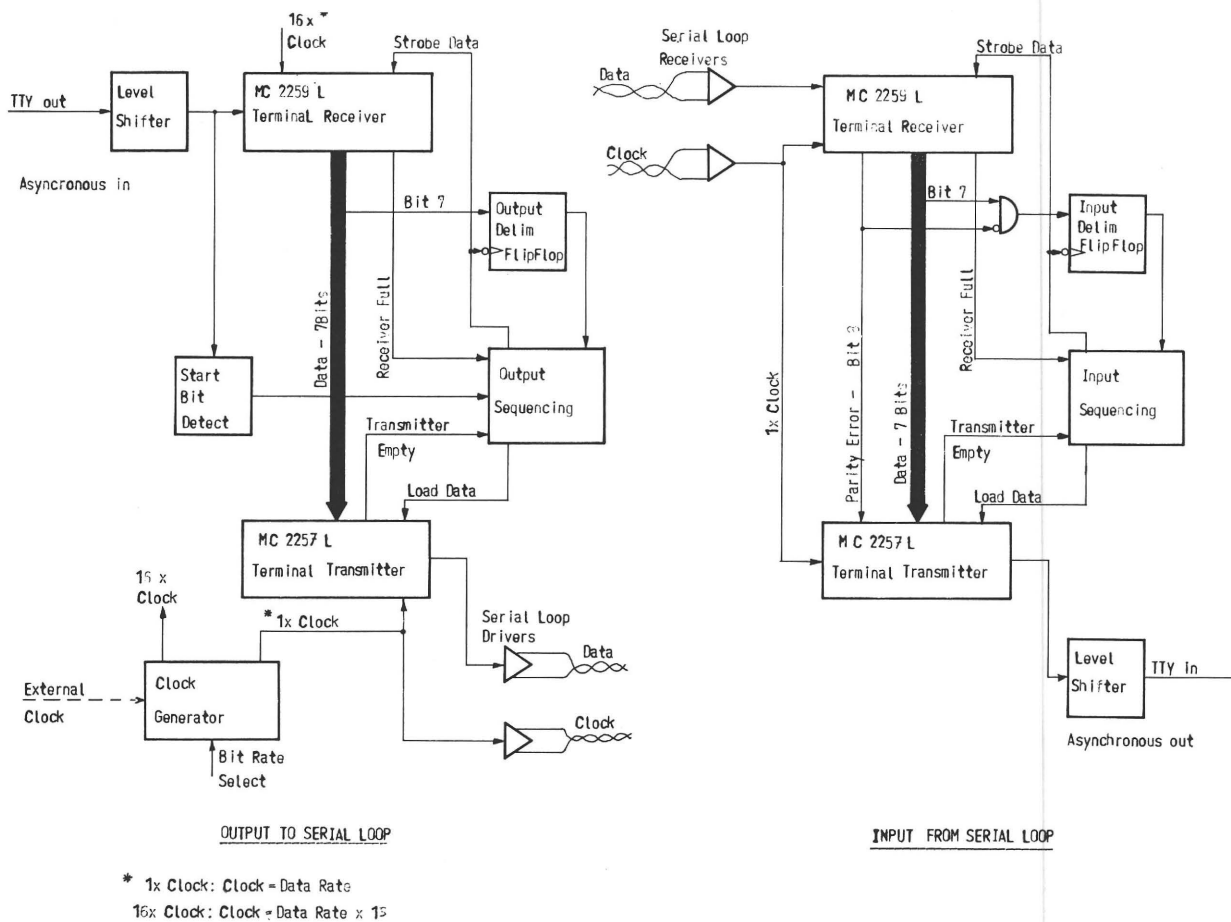


Fig. 1 Block Diagram of SHIFT Serial Highway Interface

Since the entire circuit requires only 23 integrated circuits plus some discrete components, there is space on the board to add other features, for example a modem.

There may also be applications where it is not feasible to include the SHIFT adaptor in a CAMAC crate. In such cases it would be quite easy to adapt the circuitry to virtually any circuit card format, and plug it into an empty slot in the computer.

REFERENCES

1. Barnes, R.C.M., The CAMAC Serial Highway - A Preview. *CAMAC Bulletin*, No. 8, November 1973, p. 5
2. 'CAMAC Serial System Organization - A Description', ESONE/SH/01, ESONE Committee (CRC Ispra), December 1973 and TID 26488, USAEC, Washington D.C., December 1973.

NEWS

CAMAC SOFTWARE FOR PDP-11

The following implementations of CAMAC related system software for the DEC PDP-11 computer and the DEC CA11-A have been made at the Hahn-Meitner-Institut, Berlin.

CAMAC-IML

An implementation of the CAMAC Intermediate Language (IML) is based on the Macro-Syntax (to be published by the Software Working Group). The full set of the macros is available with the exception of the block-transfer on special LAM and the X-error control statements. Those transfer modes not implemented by the hardware of the CA11-A are simulated by software. In the near future, it is intended to implement Macro-IML for the DEC CA11-C Controller.

BASIC with CAMAC

A CAMAC extension to the Single-User version of BASIC⁽¹⁾ has been implemented by introducing new keywords. The instruction set gives the programmer access to all hardware facilities of the CA11-A Controller, except the LAM-Handling.

At BCMN-Euratom, Geel, the 8-User version of BASIC⁽¹⁾ has been modified to adapt it to the CA11-A and to allow the insertion of assembler routines into the BASIC program.

¹ Halling *et al.*, KFA Jülich, *CAMAC Bulletin*, No. 6 (1973) pp. 15-17.

CAMAC PRODUCT GUIDE

AMENDMENTS TO ISSUE 9 (Hardware)

This guide consists of a list of CAMAC equipment which is believed to be offered for sale by manufacturers in Europe and the USA. The information has been compiled by CERN-NP-Electronics and is mainly based on information communicated by manufacturers and available up to the 6th June 1974.

Every effort has been made to ensure the completeness and accuracy of the list, and it is hoped that most products and manufacturers have been included. Inclusion in this list does not necessarily indicate that products are fully compatible with the CAMAC specifications nor that they are recommended or approved by the ESONE Committee. Similarly, omission from this list does not indicate disapproval by the ESONE Committee.

Readers are advised to send their addresses to manufacturers in order to be on their mailing list for current information on CAMAC Products and Applications. Readers are also advised to obtain detailed information from manufacturers or their agents in order to check compatibility and operational characteristics of their products.

Entries are grouped in new -N-, corrected -C-, and deleted -D- products, each such group arranged according to product class.

A full listing of products was published in No. 9 and will appear again in No. 11 of the Bulletin. Remarks on some columns in the Index of Products.

Column

- NCD - N is new, C is corrected, D is deleted entry.
- CODE - Classification code, a 2- or 3-digit decimal number (see below).
- WIDTH - 1 to 25, indicates module width or—for crates—the number of stations available.
 - 0 indicates unknown width or format.
 - Blank, the width has no meaning.
 - NA indicates other format, normally a 19 inch rack mounted chassis.
- NPR - Number in brackets is issue number of the Bulletin in which the item was or is described in the New Products section.
- DELIV - Date on which item became or will become available.

CLASSIFICATION GROUPS

code

- 1 DATA MODULES** (I/O Transfers and Processing)
- 11 Digital Serial Input Modules** (Scalars, Time Interval and Bi-directional Counters, Serial Coded etc.)
- 12 Digital Parallel Input Modules** (Storing and Non-Storing Registers, Coinc. Latch, Lam, Status etc.)
- 13 Digital Output Modules** (Serial: Clocks, Timers, Pulse Generators, Parallel: TTL Output, Drivers)
- 14 Digital I/O, Peripheral and Instrumentation Interfacing Modules** (Serial and Parallel I/O Regs, Printer-, Tape-, DVM-, Plotter- and Analyser Interfaces, Step-Motor Drivers, Supply CTR, Displays)
- 15 Digital Handling and Processing Modules** (and/or/not Gates, Fan-Outs, Digital Level and Code Converters, Buffers, Delays, Arithm. Processors etc.)
- 16 Analogue Modules** (ADC, DAC, Multiplexers, Amplifiers, Linear Gates, Discriminators etc.)
- 17 Other Digital and/or Analogue Modules** (Mixed Analogue and Digital, Not Dataway Connected etc.)
- 2 SYSTEM CONTROL** (Computer Couplers, Controllers and Related Equipment)
- 21 Interfaces/Drivers and Controllers** (Parallel Mode for 4600 Branch and Other Multi-

code

- Crate Bus, Single-Crate Systems, Autonomous Systems)
- 22 Interfaces/Controllers/Drivers for Serial Highway**
- 23 Units Related to 4600 Branch or Other Parallel Mode Control/Data Highway** (Crate Controllers, Terminations, Lam Graders, Branch/Bus extenders)
- 3 TEST EQUIPMENT**
- 31 System Related Test Gear**
- 32 Branch Related Testers/Controllers and Displays**
- 33 Dataway Related Testers and Displays**
- 34 Module Related Test Gear** (Module Extenders)
- 37 Other Test Gear for CAMAC Equipment**
- 4 CRATES, SUPPLIES, COMPONENTS, ACCESSORIES**
- 41 Crates and Related Components/Accessories** (Crates with/without Dataway and Supply, Blank Crates, Crate Ventilation Gear)
- 42 Supplies and Related Components/Accessories** (Single- and Multi-Crate Supplies, Blank Supply Chassis, Control Panels, Supply Ventilation)
- 43 Recommended or Standard Components/Accessories** (Branch Cables, Connectors etc., Dataway Connectors, Boards etc., Blank Modules, Other Stnd Components)

INDEX OF PRODUCTS
(AMENDMENTS TO ISSUE 9)

NCD CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
NEW ITEMS						
N .111	HEX COUNTING REGISTER (6X24BIT, 100MHZ NIM & TTL LEVELS, TTL CARRY OVF, BIN)	320	HYTEC	1	08/74	
N .111	TIME DIGITIZER (6CHANNELS, 16 BITS, 100 MHZ CLOCK RATE)	TD	JOERGER	1	08/74	
N .111	12-CHANNEL 100 MHZ SCALER(12X24BIT,-0.5V I/P THR, COMMON FAST CLEAR & INHIB, NIM)	2551	LRS-LECRDY	1	09/74	
N .111	12-CHANNEL 16-BIT SCALER (CERN SP92135)	9054	NUCL. ENTERPRISES	1		(10)
N .112	HEX COUNTING REGISTER (6X24BIT, 100MHZ NIM & TTL LEVELS, TTL CARRY OVF, BCD)	321	HYTEC	1	08/74	
N .113	DUAL PRESET COUNTER/TIMER (2X16/24BIT, 40MHZ MIN, SELF RELOADABLE)	1006	BORER	1	07/74	
N .121	PARALLEL INPUT GATE (CERN SP92133)	9049A	NUCL. ENTERPRISES	1		(10)
N .121	PARALLEL INPUT GATE (24 BIT)	9049B	NUCL. ENTERPRISES	1		(10)
N .122	INPUT REGISTER (24 INPUTS, + STROBE, OPTICALLY ISOLATED)	IR=2	JOERGER	1	06/74	
N .131	REAL TIME CLOCK	9064	NUCL. ENTERPRISES	1		(10)
N .133	OUTPUT REGISTER (2X16BIT, OPEN COLLECTOR)	1084	BORER	1	06/74	
N .142	15 BIT PARALLEL OUTPUT REGISTER (BIT ADDRESSABLE, NIM LEVELS OR PULSES)	C 343	INFORMATEK	1	/73	
N .142	INPUT/OUTPUT REGISTER (24 BITS IN, 12 BITS OUT, OPTICALLY COUPLED)	IOR=1	JOERGER	1	05/74	
N .142	16 BIT INPUT/OUTPUT REGISTER (O/P STAGES ON-PLUGABLE PC, FP CONNECTOR)	IOR 2053	SEN	1	04/74	
N .154	2048-WORD 16 BIT STORE	9061	NUCL. ENTERPRISES	2		(10)
N .161	16-CHANNEL A/D CONVERTER (DIFFERENTIAL INPUTS, 11 BITS + SIGN)	AM=1	JOERGER	2	06/74	
N .161	TIME DIGITIZER (6CHANNELS, 16 BITS, 100 MHZ CLOCK RATE)	TD	JOERGER	1	08/74	
N .164	16-CHANNEL A/D CONVERTER (DIFFERENTIAL INPUTS, 11 BITS + SIGN)	AM=1	JOERGER	2	06/74	
N .211	BIDIRECTIONAL DATA BREAK MODULE FOR PDP8 COMPUTERS (FOR USE WITH 7048-2)	1000	HYTEC	2	09/74	
N .22	DRIVER FOR SERIAL HIGHWAY	3992	KINETIC SYSTEMS	3	01/74	
N .232	PRIORITY GRADER	9037	NUCL. ENTERPRISES	1		(10)
N .233	BRANCH TERMINATOR (NON-INDICATING, 40 CM FLYING CABLE WITH BRANCH CONNECTOR)	BT 231	SEMRA-BENNEY	1	04/74	
N .233	(DITTD, XXX# CABLE LENGTH IN CM)	BT 231XXX		1	04/74	
N .233	BRANCH HIGHWAY TERMINATOR	BHT 2055	SEN	1	03/74	
N .411	CAMAC MINICRATE (+6V/15A, -6V/5A, +24V/2A, -24V/2A, 200W)	307/101	EDS SYSTEMTECHNIK	17	/73	(10)
N .411	POWERED CRATE (+6V/32A, -6V/32A, +24V/6A, -24V/6A, +200V/, 1A, 300W, POWER FAIL LAM)	PC 2057	SEN	NA	03/74	
N .431	BRANCH HIGHWAY CONNECTOR (FREE MEMBER, PIN MOULDING WITH METAL PIN PROTECTOR)	HSS0132P088N527=M	EMIHUS		/73	
N .432	DATAWAY MOTHERBOARD (WITH CONNECTORS)	1186	WEHRMANN		/74	(10)
N .433	CAMAC CARRYING CASE (TAKES 12 MODULES)	C/NCC12-6	HENESA		/73	
N .433	GENERAL-PURPOSE IC PATCH BOARD	18605	VERO ELECTRONICS		/74	

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
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CORRECTED ITEMS

C	.113	PRESET QUAD COUNTER (4X24BIT, 75 MHZ, NIM + TTL LEVELS, TTL CARRY OVF, BINARY)	310	HYTEC	1	/73	
C	.114	PRESET QUAD COUNTER (4X24BIT, 75 MHZ, NIM + TTL LEVELS, TTL CARRY OVF, BCD)	311	HYTEC	1	/73	
C	.122	DUAL INPUT REGISTER (2X24BIT, I/P INTEGR TTL, FULL LAM, OUTPUT STROBES)	220	HYTEC	1	/73	
C	.122	INPUT REGISTER (2X24BIT, 3 MODES OF DATA ENTRY, LED DISPLAY)	IR	JOERGER	1	/72	(7
C	.123	16 FOLD DCR (16 DISCR, COMMON STROBE, -70MV THRESHOLD, FAST SUMMING OUTPUTS)	23408	LRS-LECROY	2	/71	(6
C	.123	16 BIT PATTERN UNIT (CERN 071, 16 INDIV NIM INPUTS, COMMON NIM GATE, LED DISPLAY)	16P 2047	SEN	1	/72	(5
C	.127	64 LINE SURVEYOR (SINGLE OR CONTINUOUS SURVEY CYCLES, 3 SURVEY MODES)	64LS 2052	SEN	1		(9
C	.132	BUFFER STORE/REGISTER (32X24BIT, WITH EXTERNAL ADDRESSING FACILITY)	104	HYTEC	1		
C	.132	BUFFER STOR /REGISTER (32X16BIT, WITH EXTERNAL ADDRESSING FACILITY)	105		1		
C	.132	(SAME, 16X16BIT, WITHOUT EXT ADDR)	103		1	/73	
C	.132	DUAL 16 BIT OUTPUT REGISTER (SELECTABLE O/P STAGES ON PLUGABLE PC, FP CONNECTOR)	20R 2051	SEN	1		(9
C	.133	OUTPUT REGISTER (2X16BIT VIA ISOLATING CONTACTS)	1082	BORER	1	/72	(4
C	.133	DUAL OUTPUT REGISTER (2X24BIT, OPEN COLL O/P, FULL LAM, OUTPUT STROBES)	200-2	HYTEC	1	/73	
C	.142	(SAME, 32X24BIT, WITHOUT EXT ADDR)	100	HYTEC	1		
C	.142	(SAME, 32X16BIT, WITHOUT EXT ADDR)	101		1	/72	
C	.142	(SAME, 16X24BIT, WITHOUT EXT ADDR)	102	HYTEC	1	/72	
C	.142	INPUT/OUTPUT REGISTER(2X24BIT IN, 2X12BIT OUT, 3 ENTRY MODES, LED DISPLAY)	IR=1		1	/72	(7
C	.143	TERMINAL DRIVER	J TY 20	SCHLUMBERGER	1	/73	(8
C	.145	INTERFACE FOR MEASURING DEVICES (DUAL INPUT FOR 2 INSTRUMENTS)	DD 200-1412	DORNIER	1	02/74	(10
C	.147	COMMUNICATION INTERFACE (V24/V23/V21 MODEM INTERFACE WITH AUTO-DIAL OPTION)	DD 200-2911	DORNIER	1	/73	(10
C	.154	PROGRAM STORE/REGISTER (256X24BIT RAM + 64X24BIT ROM, EXT ADDR, USE WITH 7025-2)	110A	HYTEC	1		
C	.154	(SAME BUT WITHOUT EDIT ROM)	110		1		
C	.154	(SAME BUT NO BUFFER AND NO EXT ADDR)	112		1	/73	
C	.154	3-DECADE ADC & 16-WAY MUX (PRESET X1-X10 AMPL, 16X24 STORE, 100USEC/CH UPDATE)	500-1	HYTEC	1	/73	
C	.154	(SAME BUT BINARY ADC)	501		1	/74	
C	.161	3-DECADE ADC & 16-WAY MUX (PRESET X1-X10 AMPL, 16X24 STORE, 100USEC/CH UPDATE)	500-1	HYTEC	1	/73	
C	.161	(SAME BUT BINARY ADC)	501		1	/74	
C	.161	(SAME, BUT AMPL GAIN CAN BE SET AND STORED INDIVIDUALLY/CHANNEL, BCD/BIN)	510		2	06/74	
C	.161	OCTAL TIME-TO-DIGITAL CONVERTER(10BIT/CH 102/204NSEC RANGES, FAST CLEAR)	2228	LRS-LECROY	1	01/74	(9
C	.161	12-CHANNEL ADC (12 FAST I/P, 10BIT/CH, .25PC SENSITIVITY, FAST CLEAR)	2249A	LRS-LECROY	1	01/74	(9
C	.161	ANALOGUE TO DIGITAL CONVERTER (80MHZ, 12 BITS)	9060	NUCL. ENTERPRISES	1	06/74	(10
C	.164	(SAME, BUT AMPL GAIN CAN BE SET AND STORED INDIVIDUALLY/CHANNEL, BCD/BIN)	510	HYTEC	2	06/74	
C	.213	CRATE INTERFACE FOR MULTI 20 OR MULTI 8	J CM 8/20	SCHLUMBERGER	3	/74	

NCD	CODE	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
C	.233	TERMINATION UNIT (WITH BUILT-IN CABLE)	1592	BORER		1	/73
C	.234	EXTENDED BRANCH SERIAL DRIVER	3990	KINETIC SYSTEMS		5	03/74
C	.431	(***# 107, 207 - OR CUSTOMER SPECIFIED - FOR CORRESPONDING LENGTH IN CM)	CD 18067/***	EMIHUS			/71
C	.432	DATANAY CONNECTOR, EDGE TYPE II (WIRE WRAP)	1-163633-0	AMP AG			/70
C	.432	(TERMI-POINT/WIRE WRAP)	1-163634-0				/70
C	.432	(MOTHERBOARD SOLDER)	1-163635-0				/70
C	.432	(WIRE SOLDER)	1-163636-0				/70
C	.433	CAMAC CARRYING CASE (TAKES 8 MODULES)	C/NCC8-4	HENESA			/73
C	.437	LAM GRADER CONNECTOR (52-PIN FIXED MEMBER, TAKES PIN TYPE 031-9540-000)	2 0B 52 P	ITT CANNON			/70

DELETED ITEMS

D	.111	QUAD COUNTING REGISTER (4X24BIT, 100MHZ)	300	HYTEC		1	/73
D	.112	QUAD COUNTING REGISTER (4X24BIT, 100MHZ)	301	HYTEC		1	/73
D	.122	DUAL INPUT REGISTER (2X24BIT, INPUT)	221	HYTEC		1	/73
D	.122	32 BIT INPUT REGISTER	C 345	INFORMATEK		1	/73
D	.132	OUTPUT REGISTER (32X16BIT, EX. ADDRESS)	101	HYTEC		1	
D	.132	OUTPUT REGISTER (256X24BIT, EX ADDRESS)	111	HYTEC		1	/73
D	.144	MEMORY OSCILLOSCOPE DISPLAY	C 311	INFORMATEK		2	/73
D	.147	BIT-SYNCHRONIZER - CAMAC PROGRAMABLE	DD 200-2250	DORNIER		3	/73
D	.147	FORMAT-SYNCHRONIZER	DD 200-2260			4	/73
D	.147	MODEM INTERFACE WITH AWD OPTION	DD 200-2912			1	02/74
D	.147	SENSOR (INTER. UP TO 65,000 GROUPS OF	C 347	INFORMATEK		1	/73
D	.161	ADC - MEMORY INTERFACE	J CAN 20 I	SCHLUMBERGER		2	/71
D	.164	FET MULTIPLEXER	DD 200-1031	DORNIER		1	/72
D	.164	(WITH FRONT PANEL CONNECTOR)	DD 200-1231			1	/72
D	.164	FET MULTIPLEXER	DD 200-1033	DORNIER		1	/72
D	.164	(WITH FRONT PANEL CONNECTOR)	DD 200-1233			1	/72
D	.165	VOLTAGE CALIBRATOR	J ET 10	SCHLUMBERGER		1	/73
D	.211	INTERFACE CAMAC - T2000	C COB 10	SCHLUMBERGER		NA	/73
D	.211	CAMAC - T2000 BRANCH INTERFACE	T IC 20			NA	/73
D	.213	CONTROLEUR DE CHASSIS MULTI 8-CAMAC	JCM 8	INTERTECHNIQUE		3	/71
D	.213	CONTROLEUR DE CHASSIS MULTI 20 - CAMAC	JCM 20	INTERTECHNIQUE		3	/73
D	.213	CRATE INTERFACE FOR PDP 8/I	J CPDP 8/I	SCHLUMBERGER		3	/73
D	.214	MEMORY , 32 REGISTERS	DD 200-2952	DORNIER		3	/73
D	.214	(SAME WITH 48 REGISTERS)	DD 200-2953			3	/73
D	.214	(SAME WITH 64 REGISTERS)	DD 200-2954			3	/73
D	.214	PROGRAM MEMORY	DD 200-2961	DORNIER		1	/73
D	.214	(SAME BUT 512 WORDS OF 16 BITS)	DD 200-2962			1	/73
D	.214	(SAME BUT 768 WORDS OF 16 BITS)	DD 200-2963			1	/73
D	.214	PROGRAM MEMORY FOR PROCESSOR (2K PROM)	DD 200-2965			2	03/74
D	.214	(SAME BUT 3K PROM)	DD 200-2966			2	03/74
D	.214	(SAME BUT 4K PROM)	DD 200-2967			2	03/74
D	.214	(SAME BUT 1024 WORDS OF 16 BITS)	DD 200-2964			1	/73
D	.214	ADDITIONAL MEMORY	DU 200-2971	DORNIER		1	/73
D	.214	(SAME BUT 2048 WORDS OF 16 BITS)	DU 200-2972			1	/73
D	.214	(SAME BUT 3072 WORDS OF 16 BITS)	DU 200-2973			1	/73
D	.217	SYSTEM 3000 CONTROLLER	1552	BORER		2	/72
D	.233	BRANCH HIGHWAY TERMINATION MODULE	CD 18107	EMIHUS		NA	/72
D	.417	CRATE (6U EMPTY, WITH VENTILATION RAFFLE)	IB/9905-5HV1	OSL/IMHOF-BEDCO		25	/73
D	.417	FAN MOUNTING PLATE (FOR IB/9905-5HV1)	CAM/FM				/73

INDEX OF MANUFACTURERS

- AEG-Telefunken
Elisabethenstrasse 3, Postfach 830
D-7900 Ulm, Germany
- C AMP AG**
Haldenstrasse 11
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Benney—See Semra-Benney
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ITT Cannon—See Cannon
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OSL/Willsher and Quick -- See OSL
respectively Willsher and Quick
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00-086 Warsaw, Bielanska 1, Poland
Polon—See also Zjednoczone
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- C Saip—See Schlumberger**
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Standard Engineering Corp.
44800 Industrial Drive,
Fremont, California 94538, USA
Tech and Tel—See Technograph
Techcal - See Stnd Engineering
Technograph and Telegraph Ltd.
Easthampstead Road
Bracknell, Berkshire, England
- C Tekdata Ltd.**
Westport Lake, Canal Lane,
Tunstall, Stoke-on-Trent,
Staffs ST6 4PA, England
Tektronix, Inc.
P.O. Box 500, Beaverton,
Oregon 97005, USA
Telefunken—See AEG-Telefunken
TMA Electronics—See BI RA Systems
Transrack
B.P. 12
22, Avenue Raspail
F-94100 Saint-Maur, France
- C Ultra Electronics (Components) Ltd.**
Fassetts Road
Loudwater, Bucks., HP 10 9UT Engl.
- N Vero Electronics Ltd.**
Industrial Estate, Chandler's Ford,
Eastleigh, Hants SO5 3ZR, England
- N Karl Wehrmann, Industrievertr.**
Spaldingstrasse 74
D-2000 Hamburg 1, Germany
Wenzel Elektronik
Lamontstrasse 32
D-8000 München 80, Germany
Wenzel Elektronik (UK) Ltd.
Arndale House, The Precinct
Egham, Surrey, England
Willsher and Quick Ltd.
Walrow
Highbridge, Somerset, England
Willsher and Quick GmbH
Steylerstrasse 27, Postfach 2192
D-4054 Nettetal 2, Germany
Zjednoczone Zaklady Urzadzen
Jadrowych Polon, Biuro Zbytu
PI-00-086 Warszawa,
Bielanska 1, Poland

SOFTWARE PRODUCTS

INTRODUCTION

The Software Guide, a newcomer in the CAMAC Bulletin, lists a number of software packages, programs and routines which have been developed by software firms, manufacturers of CAMAC equipment, and at research laboratories.

Work is going on to implement IML—the intermediate level CAMAC language. One contribution to IML implementation is listed in the Index of Software Products below, but at least five other laboratories are at present implementing IML on various computers.

The Software Guide lists products which are in

current use or will be in nearest future. Some of the software listed is commercially available. Information about other are presumably available from respective authors. The correctness of the list has been carefully checked against data provided. Inclusion in the list does not necessarily indicate endorsement, recommendation or approval by the ESONE Committee, nor does omission indicate disapproval.

The classification used tentatively and reproduced below, is the one proposed in issue 9 of the CAMAC Bulletin, March 1974.

SOFTWARE CLASSIFICATION GROUPS

	Page		Page
.5 Software.	VIII	.54 Support Software I (translators).	X
.50 Fundamental Concepts, General Subjects.		.541 Assemblers (with/without macros).	
.500 General Descriptions, Documentation, etc.		.542 Cross-Assemblers.	
.501 Languages.		.543 Compilers.	
.502 Algorithms.		.544 Interpreters.	X
.51 User-Oriented Programs I (full system support with user run-time and CAMAC system service programs).	VIII	.55 Support Software II.	XI
.52 User-Oriented Programs II (specific run-time programs).		.551 Loaders.	
.53 User-Oriented Programs III (subprograms, routines, Hardware programs).	IX	.552 Linking Programs.	
		.553 Utility Routines.	
		.57 Other Service Programs.	
		.571 Editors.	
		.572 Debugging Routines.	
		.573 Test Routines.	XI

INDEX OF SOFTWARE PRODUCTS

.50 Fundamental Concepts, General Subjects

TITLE== IMPLEMENTING CAMAC BY COMPILERS CLASS== .50
 PUBL. REF.== PROC CAMAC SYMPOSIUM, LUXEMBOURG, DEC 1973
 W. KNEIS, GFK, ZYKLOTRON-LB., KARLSRUHE
 DESCRIPTION== DEMANDS ON REAL-TIME SYSTEMS SUCH AS MINIMUM EXECUTION TIME, MINIMUM CORE REQUIREMENTS, ETC., RECOMMEND THE USE OF COMPILERS IN CAMAC PROGRAMMING. THE POSSIBILITY TO IMPLEMENT A CAMAC LANGUAGE BY A COMPILER IS FIRST OF ALL A FUNCTION OF THE LEVEL AND CONCEPT OF THE LANGUAGE. META-LANGUAGES, DESCRIBING THE SYNTAX OF A PROGRAMMING LANGUAGE, ARE USED TO FORMULATE A COMPILER FOR A SPECIFIC LANGUAGE. THE METHOD DESCRIBED HAS BEEN USED TO WRITE A COMPILER FOR IML, THE INTERMEDIATE LEVEL CAMAC LANGUAGE, IMPLEMENTED IN AN ASSEMBLER ENVIRONMENT.

TITLE== PROCEDURE CALLS- A PRAGMATIC APPROACH CLASS== .50
 PUBL. REF.== PROC CAMAC SYMPOSIUM, LUXEMBOURG, DEC 1973 NAME==
 AUTHORS== J. MICHELSON, M. HALLING, KFA, JUELICH ESONE REGISTR DATE== 31 MAY 1974
 DESCRIPTION== DISCUSSION OF PROCEDURE CALLS AS THE BASIS FOR CAMAC SOFTWARE WITHIN HIGH-LEVEL LANGUAGES. COMPARISON WITH SYNTAX MODIFICATIONS TO LANGUAGES. DISCUSSION OF IMPLEMENTATION RESTRICTIONS DUE TO LANGUAGE REQUIREMENTS FOR EXISTING HIGH-LEVEL LANGUAGES, E.G. CLOSED SYSTEM-SUBROUTINES WHICH EXECUTE ONE DEFINED OPERATION (INVOLVING ONE OR MORE CAMAC CYCLES AS A GROUP). COMPARISON OF US-NIM CAMAC FORTRAN SUBROUTINES AND PROCEDURE-CALL SYNTAX OF ESONE SWG IML LANGUAGE. APPLICATION OF PROCEDURE-CALLS TO APPLICATION-ORIENTED SOFTWARE.

TITLE== CAMAC FACILITIES IN THE PROGRAMMING LANGUAGE OF PL-11 CLASS== .50(PL-11)
 AUTHOR== ROBERT D RUSSELL, CERN, GENEVA NAME== EXTENDED PL-11
 PUBL. REF.== PROC CAMAC SYMPOSIUM, LUXEMBOURG, DEC 1973 OPERATIVE DATE== 1971/72
 SOFTWARE TYPE== LANGUAGE, PL-11(EXTENDED) COMPUTER== PDP-11
 TECHNIQUE OF INCORPORATING CAMAC FEATURE== CAMAC INTERFACE USED== CA 11
 IN-LINE CODING OF CAMAC STATEMENTS WORDS ARE 16 BITS LONG
 FACILITIES== SYMBOLIC DEVICE NAME USED, DEMAND HANDLING INCLUDED
 DESCRIPTION== PL-11 IS AN INTERMEDIATE-LEVEL, MACHINE-ORIENTED PROGRAMMING LANGUAGE EXTENDED TO INCLUDE CAMAC FEATURES. SYNTACTIC FORM OF CAMAC STATEMENTS ARE ANALOGOUS TO STANDARD PL-11 STATEMENTS. SYMBOLIC NAMES FOR VARIABLES AND FUNCTIONS ARE DECLARED ONCE, AND OPERATIONS ARE EXECUTED BY STATEMENTS REFERRING TO THESE NAMES. USE OF SYMBOLIC NAMES MAKE PROGRAMS READABLE, AND SIMPLIFIES MODIFICATIONS OF CAMAC CONFIGURATIONS.
 EXAMPLE OF STANDARD STATEMENT== WHILE PRINTSTATUS = BUSY DD,
 EXAMPLE OF CAMAC STATEMENT== WHILE CRTSTATUS = BUSY DD,

.51 User-Oriented Programs I (full system support)

TITLE== BACKGROUND-FOREGROUND SYSTEM FOR PULSE-HEIGHT ANALYSIS OF 1ND-DIMENSIONAL MULTIWIRE PROPORTIONAL CHAMBER DATA CLASS== .51
 AUTHOR== DR. A. HEUSLER, IKP, KFA, JUELICH ACRONYM== BFG
 SOFTWARE TYPE== SYSTEM PROGRAM OPERATIVE DATE== 19747
 LANGUAGES USED== FORTRAN & MACRO ASSEMBLER COMPUTER USED== PDP-15
 PROG AVAILABLE ON PAPER TAPE, ASCII CODE CAMAC INTERFACE== BORER TYPE 2200
 CORE REQUIREMENTS== 24K
 NIM SYSTEM== DISK, MAGTAPE, DECTAPE,
 MEMORY SCANNING DISPLAY (IN-HOUSE)
 DESCRIPTION== THE SYSTEM SOFTWARE PERMITS START AND STOP OF BLOCK TRANSFER FROM THE A/D CONVERTERS TO THE PDP-15 MEMORY (LIST MODE OUTPUT ONTO MAGTAPE, ON-LINE SORTING IF DESIRED).
 THE BORER INTERFACE HAS BEEN MODIFIED TO ALLOW BLCK LENGTHS UP TO 4K 18 BIT WORDS.

TITLE== CAMAC OPERATING SYSTEM FOR CONTROL APPLICATIONS CLASS== .51
 AUTHOR== DR. B. MERTENS, IKP, KFA, JUELICH ACRONYM== COS
 PUBL. REF. CAMAC BULLETIN NO 9, MARCH 1974 OPERATIVE DATE== 1972
 TYPE OF SOFTWARE== SYSTEM PROGRAMS COMPUTER USED== PDP-15
 PROG LANGUAGES USED== FORTRAN, MACRO ASSEMBLER CAMAC INTERFACE== BORER TYPE 2200
 FACILITIES== SYMBOLIC DEVICE NAME USED, SINGLE & MULTIPLE ACTION PER CORE REQUIREMENT== 16K
 INSTRUCTION, REAL-TIME DEMAND HANDLING INCLUDED.
 AVAILABLE ON PAPER TAPE, ASCII CODE
 DESCRIPTION== THE SYSTEM SOFTWARE PACKAGE PERMITS READ AND WRITE OF UP TO 100 MODULES. REAL-TIME TASKS MAY BE DEFINED ON-LINE, ABOUT 60 ELEMENTARY COMMANDS ARE PREDEFINED, SUCH AS--
 NAME MODULE, C#1, N#2, A#3/DEFINE SYMBOLIC NAME
 =READ MODULE/F#0
 =WRITE MODULE 321/F#16
 =DISAB MODULE/F#24
 =DEFINE TASK/OPEN A TASK-DEFINITION
 =END/CLOSE TASK-FILE
 =AFTER 15 SECS TASK/EXECUTE USER-DEFINED TASK 15 SECS FROM NOW
 =ROLL MODULE 3456/VALUE TO BE WRITTEN NEXT TO MODULE

TITLE== TRIUMF CONTROL SYSTEM SOFTWARE
AUTHORS== D P GUARD, W K DAWSON,
TRIUMF, UNIVERSITY OF ALBERTA, CANADA
PUBL REF== CAMAC BULLETIN NO 6, NOV 1972
TYPE OF SOFTWARE== COMPLETE SYSTEM SUPPORT
FOR CONTROL OF TRIUMF CYCLOTRON

CLASS== .51
ACRONYM==
OPERATIVE DATE== 1973
COMPUTERS== 4 SUPERNOVAS
INTERFACE== IN-HOUSE TYPE

DESCRIPTION== THE SYSTEM SOFTWARE PACKAGE MONITORS OVER 1000 ANALOGUE PARAMETERS AND 1000 DIGITAL STATUS POINTS, SEARCHES OUT-OF-LIMIT READINGS, DISPLAYS MEASUREMENTS ON REQUEST, SETS OVER 300 ANALOGUE POINTS FROM A CENTRAL CONSOLE AND PERFORMS A NUMBER OF OTHER ROUTINES. A REAL-TIME EXECUTIVE PROGRAM = NATS (FOR NOVA ASYNCHRONOUS TASKING SUPERVISOR) = SCHEDULES AND SUPERVISES CAMAC TASKS = SUPPORTED BY A LIBRARY OF SUBPROGRAMS = AS THEY ARE REQUESTED. JOBS TO BE PERFORMED ARE STRUCTURED INTO SEQUENCES OF CAMAC OPERATIONS SPECIFIC TO A PIECE OF HARDWARE (= CAMAC MODULE). THERE IS THUS A DIRECT MODULAR HARDWARE= SOFTWARE CORRESPONDENCE. CONTROL IS BASICALLY CLOCK-INITIATED SOFTWARE SCAN OF CYCLOTRON MONITORING, BUT INTERRUPTS ARE INCLUDED, MAINLY INITIATED BY CONSOLE.

.53 User-Oriented Programs III (subprograms, etc.)

TITLE== CAMAC AND INTERACTING PROGRAMMING
AUTHOR== DR E M RIMMER
PUBL REF== PROC CAMAC SYMPOSIUM, LUXEMBOURG, DEC 1973, & BASIC CALLABLE ROUTINES, NP GROUP NOTE NP-DHG, RIMMER
SOFTWARE TYPE== SET OF SUBROUTINES
PROGR LANGUAGE USED== HP ASSEMBLY
HOST LANGUAGE== BASIC (HP EXTENSION OF)
HOST LANGUAGE== BASIC (HP EXTENSION OF)
CAMAC FEATURE INCORPORATED== IN-LINE CODED CALLS IN BASIC, SUBROUTINES IN ASSEMBLY, ABSOLUTE ADDRESS
FACILITIES== SINGLE & MULTIPLE ACTION/INSTRUCTION, NO DEMAND HANDLING
AVAILABLE IN FORM== PAPER TAPE, ASCII CODE

CLASS== .53(BASIC)
ACRONYM== HPCMA, HPCMB, HPCMC
OPERATIVE DATE== 1971/72
PROGRAM OBTAINABLE FROM== NP-DIV, CERN, CH-1211 GENEVA
COMPUTER USED== H-P 2100-SERIES
CAMAC INTERFACE USED== BOREN TYPE 2201,
CERN TYPES 7218 & HPCC-060
CORE REQUIREMENTS== 8K OF 16 BIT WORDS
MIN SYSTEM REQUIREMENTS== TELETYPE OR OR TEKTRONIX 4010 TERMINAL & CC A1

DESCRIPTION== THESE BASIC-CALLABLE CAMAC SUBROUTINES IN THREE VERSIONS FOR THREE INTERFACES PROVIDE MOST COMMAND FACILITIES FOR CONTROL AND DATA TRANSFER. DATA WORDS MAY BE 16 OR 24 BITS LONG (ONLY 16 BITS FOR HPCC-060), BINARY, BCD OR LOGIC (0 OR 1). ROUTINES COVER BLOCK TRANSFERS, PROGRAMMED, AND SEQUENTIAL ADDRESSING & UTILITY ROUTINES, IN TOTAL 18 & 3 OPTIONALLY. GENERAL FORM OF CALL STATEMENT== CALL (SUBROUTINE NUMBER,C,N,A,F,D,Q)
CALL (SUBROUTINE NUMBER,C,N,A,F,D(I),Q,W)
WHERE W IS WORD COUNT, D IS DATA, C,N,A,F, & Q HAVE USUAL MEANING.
EX== CALL(10,1,2,0,16,D(I),Q,20)
TIME IS APPR 5 MSECS/STATEMENT, BLOCK TRANSFER CALL GENERATED DIRECTLY BY INTERFACE ARE MUCH FASTER.

TITLE== SPECIFICATIONS FOR STANDARD CAMAC SUBROUTINES
AUTHOR== RICHARD F THOMAS, JR
PUBL REF== CAMAC BULLETIN NO 6, MARCH 1973
TYPE OF SOFTWARE== SET OF SUBROUTINES
PROGRAMMING LANGUAGE USED== FORTRAN
CAMAC FACILITIES== BASIC CAMAC OPERATIONS, STANDARD BLOCK TRANSFERS IN SINGLE AND MULTIPLE ACTION STATEMENTS
AVAILABLE AS== ALGORITHM

CLASS== .53(FORTRAN)
ACRONYM== SEE DESCRIPTION
OPERATIVE DATE== 1973
PROGRAM OBTAINABLE FROM== USAEC NIM COMMITTEE, CAMAC SOFTWARE WG
COMPUTER== INDEPENDENT
CAMAC INTERFACE== ANY
CORE REQUIREMENTS== NOT SPECIFIED

DESCRIPTION== A SET OF 6 SUBROUTINES, OF WHICH ONE IS CALLED BY ALL THE OTHER, PERMITS A GREAT VARIETY OF SINGLE AND MULTIPLE CAMAC OPERATIONS TO BE PERFORMED. DEMAND HANDLING, OTHER THAN BY TEST LAM, IS NOT COVERED. THE SUBROUTINES EXECUTE CAMAC OPERATIONS AS FOLLOWS==
CMCBSC = SINGLE CAMAC FUNCTION AT SINGLE ADDRESS ONE OR MORE TIMES
CMCBSEQ = SINGLE CAMAC FUNCTION AT SUCCESSION OF ADDRESSES
CMCASC = SPECIFIED CAMAC FUNCTION IN ADDRESS SCAN MODE
CMCRPT = SPECIFIED CAMAC FUNCTION IN REPEAT MODE
CMCSTP = SPECIFIED CAMAC FUNCTION IN STOP MODE
CMCLUP = SPECIFIED CAMAC FUNCTION AT A HIERARCHICAL SEQUENCE OF ADDRESSES WITH OPTIONAL SKIP OF SEQUENCE BASED ON Q
GENERAL FORM OF STATEMENT==
CALL CMC... (PARAMETER LIST)
EXAMPLE== CALL CMCSTP(F,B,C,N,AD,LN,DATA,ERRDRA,NEX)

TITLE== CAMAC FUNCTION FOR RT11
PUBL REF== URTEC
AUTHORS== L. BYARS, R. KEYSER
TYPE OF SOFTWARE== CAMAC SUBROUTINE FOR FORTRAN/RT11

CLASS== .53
NAME== CAMAC
VERSION== RT11
OPERATIVE DATE== JUNE 1974
PROG MAINTENANCE BY== URTEC
OBTAINABLE FROM== URTEC
COMPUTER USED== PDP-11
CAMAC INTERFACE USED== DCU11
(EG&G/ORTEC)
CORE REQUIREMENTS==
MINIMUM SYSTEM REQUIREMENTS==

PROG. LANGUAGE USED== PDP-11 ASSEMBLY
HOST LANGUAGES FOR DESCRIBED SOFTWARE== RT11/FORTRAN
TECHNIQUE OF INCORPORATION== CAMAC FEATURE IS EMBEDDED

FACILITIES== SINGLE OR MULTIPLE INSTRUCTIONS, DEMAND HANDLING
AVAILABLE ON == PAPER TAPE
DESCRIPTION== USED AS CALL CAMAC (IF, IN, IA, IO, IDATA) TO TRANSFER DATA TO/FROM CAMAC AND TEST. IO IS QBIT AND XBIT.

TITLE== FORTRAN SUBROUTINES
AUTHOR== H. POHL

CLASS== .53(FORTRAN)
NAME== FORTRAN CALLS
VERSION== V002
OPERATIVE DATE== MARCH 1973
PROG OBTAINABLE FROM== H. POHL
ZEL, KFA, JUELICH
COMPUTER USED== PDP-11
CAMAC INTERFACE== BOREX TYPE 1533A
CORE REQUIREMENTS== 16K X 16 BITS
MIN SYSTEM== 8K = 16K (16K RECOMMENDED)

TYPE OF SOFTWARE== PROCEDURE CALLS
PROG LANGUAGE USED== FORTRAN
CAMAC SOFTWARE ENVIRONMENT== FORTRAN ON PDP-11 (THREADED CODE)
TECHNIQUE OF INCORPORATION OF CAMAC FEATURES== SUBROUTINES
FACILITIES== SINGLE ACTION STATEMENTS
AVAILABLE ON DEC-TAPE
DESCRIPTION== FORTRAN SUBROUTINES FOR SINGLE ACTIONS, MUCH SIMPLER THAN THE NIM
APPROACH (REF. R. F. THOMAS) FOR THE BOREX 1533A CONTROLLER WRITTEN IN
REENTRANT CODE.

.54 Support Software I (translators)

TITLE== S/UNIP AN UNIVERSAL MACRO PROCESSOR
AUTHOR== SOFTWARE-PARTNER
TYPE OF SOFTWARE== MACRO PROCESSOR
FOR PROG LANGUAGE== ALL LANGUAGES
CAMAC FEATURE INCORPORATED IN-LINE
FACILITIES== FOR FULL-SET IML WITH MACRO PROCESSOR DIRECTIVES

CLASS== .54
OPERATIVE DATE== APRIL 1974
PROG MAINTENANCE BY== SOFTWARE-PARTNER
OBTAINABLE FROM== SOFTWARE PARTNER
61 DARMSTADT, GROSSGERAUERWEG 2, BRD
NIM SYSTEM== WRITTEN IN HIGH LEVEL
LANGUAGE, CAN RUN ON IBM, UNIVAC, CGC,
ICL, SIEMENS, ETC..

DESCRIPTION== S/UNIP IS A LANGUAGE INDEPENDENT MACRO PROCESSOR AND THEREFORE A TOOL
FOR MACRO EXPANSION OF EVERY EXISTING OR FUTURE PROGRAMMING LANGUAGE,
THUS S/UNIP MAINTAINS AND PROCESSES MACROS IN HIGH LEVEL LANGUAGES
(FORTRAN, BASIC, ALGOL, PEARL, ETC.) AS WELL AS ASSEMBLY LANGUAGES.
S/UNIP OPERATES AS A PRE-PROCESSOR GENERATING SOURCE CODE STATEMENTS
FOR SUBSEQUENT COMPILATION, POSSIBLY ON ANOTHER COMPUTER.

TITLE== MACROS FOR 1533A
AUTHOR== MR. HEER

CLASS== .541
NAME== MACRO 1533A
OPERATIVE DATE== FEBRUARY 1973
PROG MAINTENANCE BY== MR. HEER
PROG OBTAINABLE FROM== MR. HEER
ZEL, KFA, JUELICH
COMPUTER== PDP-11
CAMAC INTERFACE== BOREX TYPE 1533A
CORE REQUIREMENTS== 8K X 16 BITS
MIN SYSTEM== DOS V004, 008, 009

TYPE OF SOFTWARE== MACRO-SET
PROG LANGUAGE USED== MACRO 11
CAMAC SOFTWARE ENVIRONMENT== ASSEMBLER
TECHNIQUE OF INCORPORATION OF CAMAC FEATURE== IN-LINE
FACILITIES== SINGLE ACTION STATEMENTS, SYMBOLIC DEVICE NAMES
AVAILABLE ON DEC-TAPE

DESCRIPTION== THIS IS A SIMPLE MACRO SET (NO DECLARATIONS) FOR SINGLE ACTION
STATEMENTS, EXECUTION SPEED IS HIGHER (APPROX 30 USECS/INSTRUCTION,
DEPENDING ON TYPE OF INSTRUCTION ON TYPE OF PDP-11), NOT INTER-
RUPTABLE MACROS (PRIORITY=7).

TITLE== A BASIC-MACRO 11 COMPILER
PUBL. REF.== CAMAC BULLETIN NO. 10, JULY 1974
AUTHOR== B. BECKS
TYPE OF SOFTWARE== COMPILER
FOR PROGRAMMING LANGUAGE== BASIC
CAMAC SOFTWARE ENVIRONMENT== MACRO ASSEMBLER
TECHNIQUE OF INCORPORATION OF CAMAC FEATURE== IN-LINE
FACILITIES== SINGLE-ACTIONS
PROG. AVAILABLE ON DEC-TAPE

CLASS== .543
NAME== MABA
OPERATIVE DATE== JANUARY 1974
PROG. MAINTENANCE BY== B. BECKS
PROG. OBTAINABLE FROM== B. BECKS,
ZEL, KFA-JUELICH
COMPUTER USED== PDP-11
CAMAC INTERFACE== BOREX TYPE 1533A
CORE REQUIREMENTS== 16K X 16 BITS
MIN SYSTEM== DOS V08 OR V09 16K

DESCRIPTION== THIS COMPILER TRANSLATES TESTED (INTERPRETIVE) BASIC PROGRAMS INTO
MACRO-11 SOURCE CODE, RUN-TIME IS IMPROVED BY A FACTOR OF 15 TO 20,
EASILY ADAPTABLE TO OTHER CONTROLLERS (MACROS), OUTPUT CODE LINKED
WITH FLOATING POINT PACKAGE CAN RUN ON STAND-ALONE MINI-COMPUTER.

TITLE== A CAMAC EXTENDED BASIC LANGUAGE
AUTHOR== J M SERVENT (SCHLUMBERGER), FRANCE
PUBL. REF.== PROC CAMAC SYMPOSIUM, LUXEMBOURG, DECEMBER 1973
TYPE OF SOFTWARE== INTERPRETIVE LANGUAGE EXTENDED WITH MACRO-
INSTRUCTION GENERATOR
LANGUAGE== EXTENDED BASIC

CLASS== .544(BASIC)
ACRONYM== CASIC
OPERATIVE DATE== 1973
PROGRAM OBTAINABLE FROM==
SCHLUMBERGER/SAIP, BAGNEUX, FRANCE
COMPUTER== PDP-11
CAMAC INTERFACE USED== ICP 11 & JCC 11

DESCRIPTION== STANDARD BASIC IS EXTENDED WITH 4 NEW TYPES OF STATEMENTS AND 2
SPECIAL REGISTERS, EXECUTION OF CAMAC STATEMENTS ARE SPEEDED UP ABOUT
10 TIMES COMPARED WITH STANDARD BASIC.
TYPICAL STATEMENTS==
DECLARATIVE== 100 LET \$S8 = STA (2,4,N+3,A+2)
OPERATIONAL== 130 R1 = CAM (\$S8, READ)
CONDITIONAL== 156 IF %CAM = 0 THEN LET A = A+1
INTERRUPT/LAM== 23 ON LAM %REG THEN GOTO 130
THE INTERRUPT WILL BE SERVICED ONLY WHEN PROGRAM HAS ADVANCED TO THE
LAM-HANDLING STATEMENT.

TITLE== FOCAL OVERLAY FOR CAMAC DATA AND COMMAND HANDLING
 AUTHORS== F MAY, H HALLING, K PETKECZEK
 PUBL REF== CAMAC BULLETIN NO 1, JUNE 1971
 TYPE OF SOFTWARE== INTERPRETER (EXTENDED)
 CAMAC SOFTWARE ENVIRONMENT== FOCAL
 TECHNIQUE OF INCORPORATION OF CAMAC FEATURE==CAMAC EXTENSION ON
 OVERLAY, IN-LINE CODING OF CAMAC COMMANDS
 DESCRIPTION== THE INTERPRETER IS PRIMARILY INTENDED FOR EASILY PROGRAMMED ON-LINE
 CAMAC SYSTEMS IN NON-TIME-CRITICAL CONTROL AND DATA HANDLING
 APPLICATIONS AND FOR TEST ROUTINES.
 THERE ARE 9 CAMAC STATEMENT TYPES COVERING GENERAL CONTROLS (Z, C, I)
 AND CAMAC COMMANDS WITH/WITHOUT DATA TRANSFER.
 THE GENERAL FORM OF A CAMAC STATEMENT IS --
 +A CF,C,N,A,F,FB,HW L,LH,QI
 WHERE SEVERAL PARAMETERS MAY BE OMITTED.

CLASS== .544(FOCAL)
 NAME== FOCADAT
 OPERATIVE DATE== 1970
 COMPUTER USED== PDP-8
 CAMAC INTERFACE USED==
 IN-HOUSE CC & INTERFACE
 CORE REQUIREMENTS== 4K & 8K 12 BITS/WORD

TITLE== 8-USER BASIC UNDER DUS
 WITH INTERPRETER EXTENDED FOR CAMAC
 AUTHOR== PFEIFFER, SPRICKMANN, CARLEBACH
 TYPE OF SOFTWARE== DOS SYSTEM INTERFACE TO BASIC AND CAMAC
 PRG LANGUAGE USED== BASIC
 CAMAC FEATURE INCORPORATED BY== EXTENDING INTERPRETER

CLASS== .544(BASIC)
 NAME== 8-USER BASIC UNDER DUS
 VERSION== 001
 OPERATIVE DATE== JANUARY 1974
 PRG MAINTENANCE BY== D, P, PFEIFFER,
 PRG OBTAINABLE FROM== D, P, PFEIFFER,
 ZAM, KFA, JUELICH
 COMPUTER USED== PDP-11
 CAMAC INTERFACE== BORER TYPE 1533A
 CORE REQUIREMENTS== 16K X 16 BITS
 MINSYSTEM== DOS V08 OR V09, 16K

SOFTWARE AVAILABLE ON DEC-TAPE
 DESCRIPTION== THE 8-USER BASIC CAN BE RUN UNDER DOS. A HELP FILE CONTAINS ALL
 MODIFICATIONS OF THE 1 TO 8 USER BASIC. NO INTERRUPT HANDLING. A
 COMMUNICATION BETWEEN THE 8 USERS IS POSSIBLE BY ONE COMMUNICATION
 WORD PER USER. EXPANDED ERROR MESSAGE HANDLING, FILE HANDLING
 EXTENDED. TIME-COMMAND ADDED.

TITLE== DRACL (TM), AN INTERPRETIVE REAL-TIME MONITOR
 WITH CAMAC SUPPORT
 PUBL REF== ORTEC, INCORPORATED
 AUTHORS== L. BYARS, R. KEYSER
 TYPE OF SOFTWARE== SYSTEM
 PRG LANGUAGE USED== PDP-11 ASSEMBLY
 CAMAC FEATURE IS EMBEDDED

CLASS CODE== .544
 ACRONYM== DRACL (TM)
 OPERATIVE DATE== APRIL 1974
 PRG MAINTENANCE BY== ORTEC
 COMPUTER USED== PDP-11
 CAMAC INTERFACE USED== EG&G/ORTEC TYPE
 DC011
 CORE REQUIREMENTS== 5K X 16 BIT WORDS
 MIN SYSTEM REQUIREMENTS== TTY & DC011

FACILITIES== SINGLE OR MULTIPLE INSTRUCTIONS, DEMAND HANDLING
 AVAILABLE ON PAPER TAPE AND DISK
 DESCRIPTION== DRACL INTERPRETS ARITHMETIC STATEMENTS, PROGRAM CONTROL STATEMENTS,
 COMMENTS, I/O STATEMENTS, AND HARDWARE CONTROL STATEMENTS AND EXECUTES
 THE DESIRED FUNCTION.
 DRACL (TM) IS A TRADE MARK REGISTERED BY ORTEC, INC.

.55 Support Software II

TITLE== A FOCAL INTERRUPT HANDLER FOR CAMAC
 AUTHORS== F MAY, W MARSCHIK, H HALLING
 PUBL REF== CAMAC BULLETIN NO 6, MARCH 1973
 TYPE OF SOFTWARE== INTERRUPT HANDLER (SYSTEM PROGRAM)
 DESCRIPTION== FOCALINT IS A GENERAL PURPOSE SYSTEM PROGRAM, ADAPTABLE FOR SPECIAL
 USE. UP TO 3 CRATES WITH 24 INTERRUPTS EACH CAN BE SERVICED. ONE
 PROGRAM LINE IN FOCAL IS RESERVED FOR EACH INTERRUPT. SHORT ROUTINES
 CAN BE TYPED INTO THESE LINES SERVICING THE ASSOCIATED INTERRUPTS,
 ALTERNATIVELY A FOCAL SUBROUTINE CAN BE USED. CURRENT LINE IN THE
 BACKGROUND PROGRAM WILL BE FINISHED BEFORE JUMPING TO INTERRUPT
 ROUTINE AND RETURNS TO NEXT LINE IN THE BACKGROUND PROGRAM AFTER
 SERVICING.

CLASS== .553(FOCAL/PAL)
 NAME== FOCALINT
 OPERATIVE DATE== 1971
 COMPUTER USED== PDP-8

.57 Test Routines

TITLE== CAMAC TEST PROGRAM
 AUTHOR== DR. B. MERTENS, IKP, KFA, JUELICH
 SOFTWARE TYPE== TEST ROUTINES, STAND ALONE PROGRAMS
 AVAILABLE ON PAPER TAPE, ASCII CODE

CLASS== .573
 OPERATIVE DATE== 1971
 COMPUTER== PDP-15
 CAMAC INTERFACE== BORER TYPE 2200
 CORE REQUIREMENTS== 16K

DESCRIPTION== STAND ALONE PROGRAMS TEST SOME FUNCTIONS OF THE BORER TYPE 2200
 INTERFACE, THE CRATE CONTROLLER AND TWO IN-HOUSE MODULES (C01 & C02)
 ERROR MESSAGES ARE OUTPUT IF THERE ARE HARDWARE FAILURES.

NEWS

ANNOUNCEMENTS BY CAMAC MANUFACTURERS

APPLIED COMPUTER SYSTEMS LIMITED is offering a software package, CATY, designed at the Daresbury Laboratory (U.K.) to help with the testing of CAMAC modules and peripherals interfaced via CAMAC.

CATY is a machine independent high-level language based upon a subset of BASIC with extensions for addressing CAMAC. However, unlike many BASIC systems, the programs written in CATY are compiled and not interpreted. Thus, the speed at which CAMAC is driven, using this testing aid, is of the same order as that at which it would be driven when in use for applications.

CATY has been implemented upon a 4K DEC-PDP-11 and has now been in use for one year. During this time, new facilities have been added to the language in the light of the requirements of test engineers.

CATY was on show during the 1st CAMAC Symposium and Exhibition in Luxembourg where it was used to checkout the remote job entry communication channel to Daresbury's IBM 370/165.

NUCLEAR ENTERPRISES announce further success with their CAMAC-based Multi-Channel Analyser incorporating the DEC-PDP-11.05 computer. Systems have already been supplied to Denmark, Pakistan, South Africa, in addition to those supplied in the United Kingdom. Systems being commissioned at the moment include Analysers for West Germany, Kuwait and Pakistan in addition to two systems for the National Radiological Protection Boards, The Royal Free Hospital, Central Electricity Generating Board, Portishead and others in the United Kingdom.

A wide range of peripherals is offered and the flexibility of the CAMAC system is used to supply tailor-made input and output format.

NUCLEAR ENTERPRISES have also recently supplied Data-Logging systems to various disciplines. Three such systems, based on the 7025 Programmable Dataway Controller, have been supplied to C.E.R.L. Leatherhead, to whom Nuclear Enterprises acknowledge their assistance and advice on tailoring the original system to compete in the Data-Logger market.

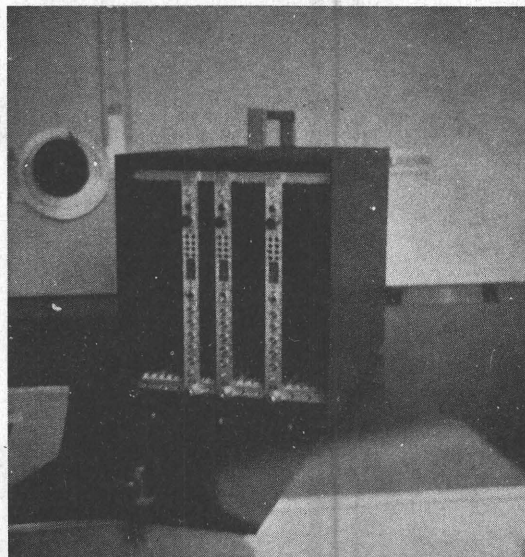
Other systems have been supplied to the Royal Navy, for submarine trials, to British American Tobacco and to the National Coal Board, in addition to those supplied in the more traditional market of nuclear research.

NUCLEAR ENTERPRISES have recently won an order for supply of CAMAC modules to CERN Lab. 2. The total value of the order is in excess of £50,000 and concerned the following five new modules, delivery of which commenced Summer 1974.

1. 9049 Parallel Input Gate.
2. 9054 12-Channel 16-Bit Scaler.
3. 9063 Serial Bi-Directional Transmitter.

4. SPS2048 Single Crate Test Controller with Program Plug Board.
5. SPS2090 Universal Input/Output Register.

HIGH ENERGY AND NUCLEAR EQUIPMENT S.A. is offering carrying cases for CAMAC units. These cases are lockable and can be supplied for either 8 or 12 single-width units. They are low weight, very strong, comparatively inexpensive and available from stock.



SEMRA BENNEY (ELECTRONICS) LIMITED have now available a low-cost Branch Termination Unit, Type BT231 in a single-width unit equipped with a flying lead (40 cm) for connection to the last controller in a multicrate system.

TEKTRONIX is offering a wave measuring and analysing system to all CAMAC users and on any computer.

The basic system consists of the Tektronix 'Digital Processing Oscilloscope' (DPO) and/or the fast 'Transient Digitizer' (R7912) originally interfaced to a PDP-11 computer via a dedicated interface unit. The new 'CAMAC APD/R7912 Controller' is intended as a general interface between any computer equipped with CAMAC and the DPO/R7912 Tektronix assemblies. This development has been done in collaboration with CERN* where a Tektronix wave analysing system with a Hewlett-Packard computer was required for the detection of extremely weak signals in high noise using the flexibility of the DPO in combination with a computer.

The double-width CAMAC unit is fully compatible with the CAMAC Specification, EUR 4100 (1972)—TID 25877 and is now commercially available.

* Vanuxem, J.P., APD/R7912 Controller, Type 161, CERN CAMAC Note 51-00.

A CAMAC MULTICRATE SYSTEM ON-LINE TO AN HP2116B COMPUTER

by

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Joint Institute for Nuclear Research, Dubna, U.S.S.R.

Received 6th December 1973

SUMMARY A CAMAC four-crate system is described. The crate controllers and the branch driver that couples them to the computer are specific to the HP2116B computer. The interconnecting cables are limited to a total length of 4 m. The maximum rate of information exchange is 312,500 16-bit words per second.

INTRODUCTION

A system of four CAMAC crates on-line to an HP2116B computer is considered in this paper. This system is used for data acquisition in high energy physics experiments (Fig. 1). Two interface cards in the input/output system of the computer^{1,2} are coupled to a Type 821 driver (DHP) which has star connections to the four crates (up to seven crates can be coupled to the driver). Each CAMAC crate in the system is controlled by a Type 604 specialized controller. This controller also allows a single crate to be connected to the computer by means of two interface cards. The

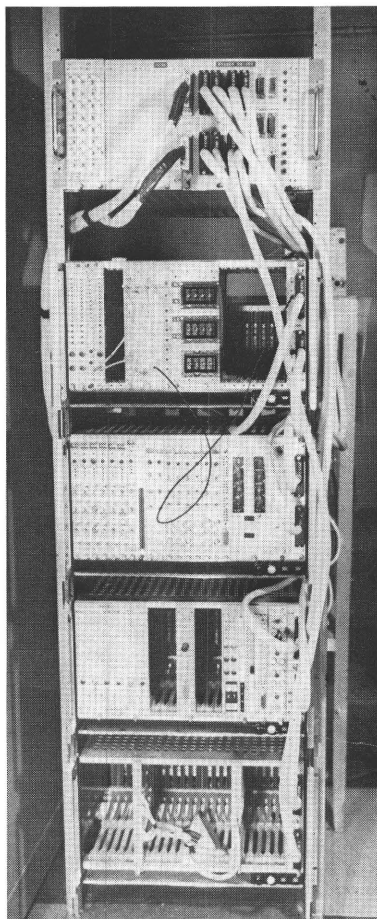


Fig. 1 View of the Four Crates in the CAMAC System

word length in all types of data transfer in the system is limited to 16 bits. The maximum rate of data transfer is 312,500 words a second.

DESCRIPTION OF THE SYSTEM

Two channels (control and data) are provided to connect the driver to the computer (Fig. 2). The channel consists of an interface card in the input/output system of the computer, and an interconnecting cable with the corresponding connector on the driver. Inside the driver the signals of each channel are fed in parallel to seven connectors. Thus, the driver has a separate pair of connecting channels for each of seven crate controllers.

Data transfer in the system is performed as follows. The computer sends a CNAF command via the command channel. A crate number decoder in the driver generates a signal on one of seven individual crate number lines. The addressed controller stores the command in registers and generates a CAMAC cycle with the corresponding Dataway command. When reading, the data are transferred to the Dataway by an addressed module. Then, via the controller and the data channel, the data are transferred to the driver, ANDed with the crate number signal, and written into the register in the interface card. When writing, the data from the interface card via the data channel and the controller are transferred to the Dataway and are taken by the addressed module. During other command operations (for example, Z) a data transfer is not organized, and commands are performed in the driver, controllers or modules.

Request signals from the modules are ORed in the controller, and the output is transferred via the command channel to the driver, where it sets one of the interrupt register triggers. This generates an interrupt request to the computer. The computer reads the state of 16 request lines previously selected in the controller and processes the request.

The driver has no registers, except the trigger interrupt register, since there are registers for storing information in the interface card of the computer and the specialized controller. By pushing a command button or by an external signal it is possible to set one of the register triggers and so generate an interrupt request. The computer reads the contents of the register, finds the source of interruption, begins to process the request, and sends to the driver a response signal which switches on the corresponding lamp on the front panel. The modules of the system³, the specialized controller and the branch driver been developed and made at the Laboratory of High Energies, JINR. The driver is made as a CAMAC module not connected to the Dataway.

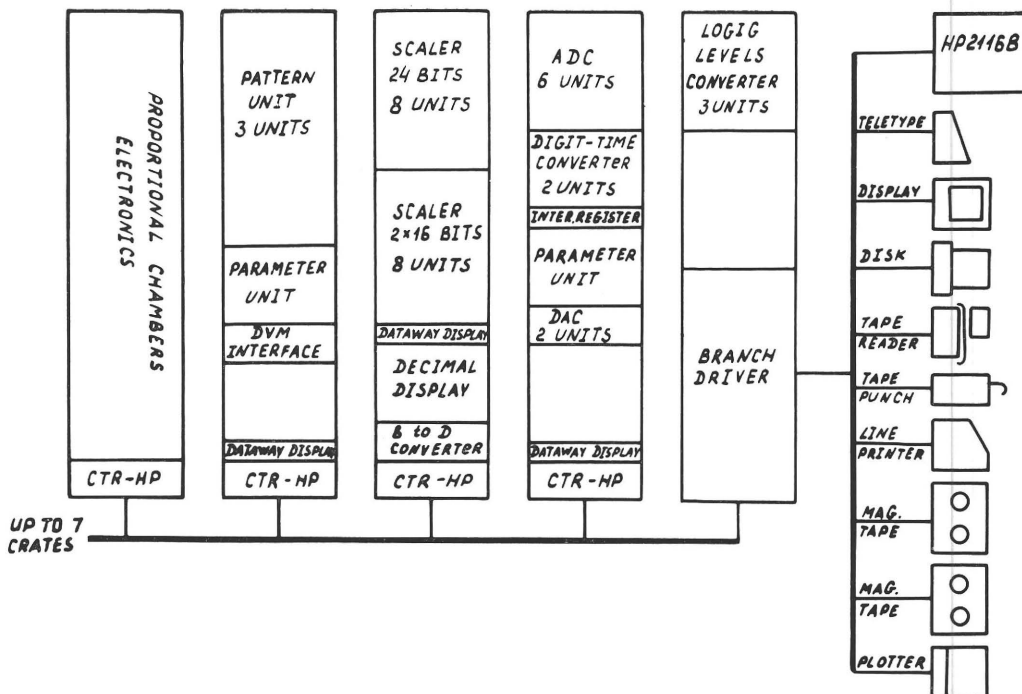


Fig. 2 Block Diagram of the CAMAC Four Crate System On-line to the HP2116B Computer

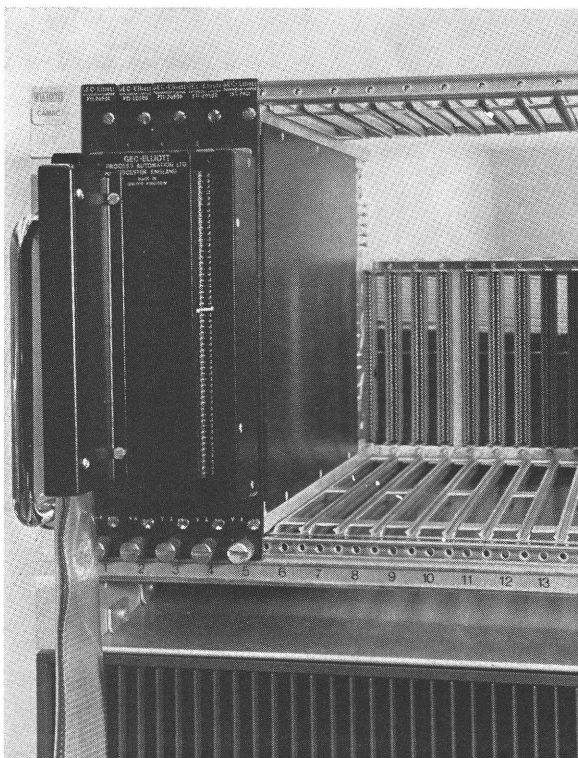
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1. A pocket guide to HP computers, Hewlett Packard, 1970.
2. A pocket guide to interfacing HP computers, Hewlett Packard, 1969.
3. Arefiev, V.A., *et al.*, Digital Modules for Physics Experiments and Measurements in the CAMAC System. *CAMAC Bulletin*, No. 5, Nov. 1972, pp. 19-20.

NEWS

ANNOUNCEMENTS BY CAMAC MANUFACTURERS

GEC-ELLIOTT PROCESS AUTOMATION LIMITED has developed an interface for the GEC 2050 and 4080 computers, and the first was



delivered (for a GEC 4080) in January 1974 (see photograph). The interface operates as a system crate unit (see *CAMAC Bulletin*, No. 7, page 21) in conjunction with the GEC-Elliott Executive Controller MX-CTR-2; it consists of single-width units PTI-2050 C and PTI-2050 D (Program Transfers Interface, Control and Data respectively) joined by a screw-on front-panel bus, the IUB (Inter-Unit Bus). Connection to the computer is via an edge-connector on the front face of the IUB.

It is a feature of the GEC 2050 and 4080 that they can carry-on a number of autonomous transfers at a time, and the interface can support up to seven autonomous channels, each of which uses a further PTI-2050D unit in collaboration with the standard Interrupt Vector Generator IVG-2401 thus a full complement of seven autonomous channels and the program transfer channel would use one PTI-2050C, eight PTI-2050D and one IVG-2401, connected by a 10-width IUB.

Other units from the GEC-Elliott Executive Suite of System Crate units will work with this interface: Branch Coupler (BR-CPR-2) of which up to seven may be used, each driving a full EUR 4600 Branch Highway, and the SC-TST-1, a System Crate two-command manual unit. In addition, of course, the interface will time-share with any of the other computer interfaces (PDP-9, 11 or 15; Nova; Interdata 70; Honeywell, etc) supplied by GEC-Elliott.

DEDICATED CAMAC CRATE CONTROLLER WITH AUTONOMOUS DATA COLLECTION

by

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Received 18th February 1974

SUMMARY This dedicated CAMAC crate controller suits the special requirements of many high energy nuclear physics experiments. It allows data collection from sources with arbitrary block lengths, and from a fixed array of sources. Several features minimise the load on the computer.

INTRODUCTION

The trend in particle physics experiments is undoubtedly towards high data-taking rates. During a typical 'run' with irregularly timed incoming 'events', datasets with several hundreds of words have to be transferred roughly 10 times per second to the process computer, which in turn gives most of the data to the central computer after some formatting and preprocessing. It is obvious that the throughput is strongly dependent on the time needed to read the data out of the CAMAC crates. This is best done by using Direct Memory Access and transfer in one block whenever possible. A special difficulty in these applications is the irregular time sequence of the incoming data, e.g. from preprocessors for spark and proportional chambers.

Mainly to overcome this problem a controller with a built-in buffer for 256 CAMAC words has been developed, originally for use with PDP-8 computers. This feature facilitates 'data gathering regions' each consisting of up to three crates (using a Dataway extension method to be described elsewhere), which operate in parallel to derandomize and deliver data blockwise in the 'first ready—first come' mode.

AUTONOMOUS OPERATION

In order to get maximum benefit from the data memory, the controller is able to gather data without action by the computer. In this mode, called Data Collection, the Dataway timing generator recycles unless it is stopped by the Hold feature. The data gathering period commonly contains an Address Scan Mode (described in EUR 4100 5.4.3.1), which can be started by a trigger signal via a front panel connector. Usually data sources like scalars, ADC's and time-digitizers are read in a sequence determined by a prewired list consisting of up to 16 stations (using the extension technique: up to 48 stations). Within stations, up to 16 subaddresses can be read utilizing the Q Response. The end of the list normally terminates the Data Collection. An additional CAMAC cycle is commonly used for generating the clear signal C.

The Address Scan period may be preceded or followed, as desired, by a Stop Mode section. This is useful for chamber readout devices which normally deliver an uncertain number of data words to be read. If the Stop Mode is used, the Data Collection is

initiated by the L signal of the readout module, which indicates that the first wire address is ready to be read. The controller grants as soon as possible $N(i) \cdot F(0) \cdot A(0)$. At time S1, the data word is written into the buffer memory, then S2 causes the (chamber) readout device to search for further valid wire numbers. If the search procedure takes more time than is available before the next CAMAC cycle, the HOLD signal (P2) is used in order to avoid empty places in the buffer. The end of the chamber readout period is indicated by $Q \rightarrow 0$. The last word may be used to store a distinct pattern to simplify orientation within the data block.

Upon finishing the data collection or upon filling the buffer completely, the controller starts the data transfer to the computer. The processor program need only enable the data channel. The controller may, if desired, generate an Interrupt signal to announce the block transfer. For events yielding more than 256 CAMAC words, data collection is suspended until the whole buffer content is accepted by the processor. In this way, several consecutive block transfers may be made, the last of which is terminated by an End-of-Event signal causing the computer to start data analysis. In special cases the apparent buffer length may be shortened by jumper connections (which waste some time, because the information must still pass all 256 places of the shift register). On the other hand provisions are made to initiate transfers only when a certain minimum number of words has been collected.

Since the computers to be used have word lengths of less than 24 bits, the user can choose by switch 'Only Low Byte' (12 or 16 bits), 'Only High Byte' or 'Both Bytes' (High and Low alternate).

SPECIAL FEATURES

Sometimes it is necessary to scan a number of data sources only a few of which have useful data, for example ADCs most of which did not pass a certain threshold. The signal 'No Store' to a private contact causes the buffer not to store the word on the Read lines although a normal CAMAC cycle takes place in order to keep the scanning mechanism running. In these cases it is mandatory to store also the address of the source. For this purpose the controller offers the current station number (binary coded) via 4 private pins to the user, who can route them to unused read lines in the module generating the 'No Store' signal. (The present subaddress is accessible to this module on the Dataway.) As a second solution to this problem the addresses of several from a large number of sources can be found using pattern units or similar devices. It saves a lot of collecting time to tell the controller directly which address is to be read. This is done via the

same 4 private pins just mentioned in the 'External Scan Mode' (activated by another P contact).

A further useful feature is a 4 digit display which shows in octal code the data on Read or Write busses, Hi or Lo order, selected by a 4 position switch. This, as well as some status indication LEDs speed up fault location, but it can also be used to read the contents of selected registers, by means of an auxiliary module using the binary coded station number.

PROGRAMMED OPERATION

Because it may be in Autonomous Mode, the controller is not always ready for the performance of 'normal' command operations. Programmed operation is interlocked with Autonomous Mode and specially requested. Two possibilities are provided to do this: A Look-at-me signal from at least 1 of 15 stations, or a computer demand transmitted by a command pulse. Simultaneous LAMs are arranged in a priority sequence by hardware encoders. All LAMs may be disabled by a switch at the rear or by program. When the controller is ready, an Interrupt pulse is generated and the 4 bit LAM Address is offered to the accumulator input. In most

cases the appropriate service routine will respond with a command word NAF.

There are two types of command words, each 12 bits long. One contains 5 bits each for N and F plus a bit indicating whether A = 0 or A is to be left unchanged. The A command word transmits the 4 bit subaddress only. The two word types are distinguished by the MSB. This solution establishes a good compromise between hardware, time and computer memory space requirements in most applications. The command word is stored in the controller. Thus, only an Execute pulse need be repeated for subsequent executions of the same command. After each execution the Response signals Q and X are available in the computer. During Read operations data are stored in the buffer. After termination of the 'Dialogue' by a special pulse from the computer the memory content is transferred just as in the Autonomous Mode, but always both orders (Hi and Lo). For small buffer loads, a time penalty is incurred because of the reason mentioned above. However, this principle was maintained here in favour of economy.

The Block Diagram shows the essential parts of the controller and their interconnection. A detailed description (in German) may be obtained directly from the authors*.

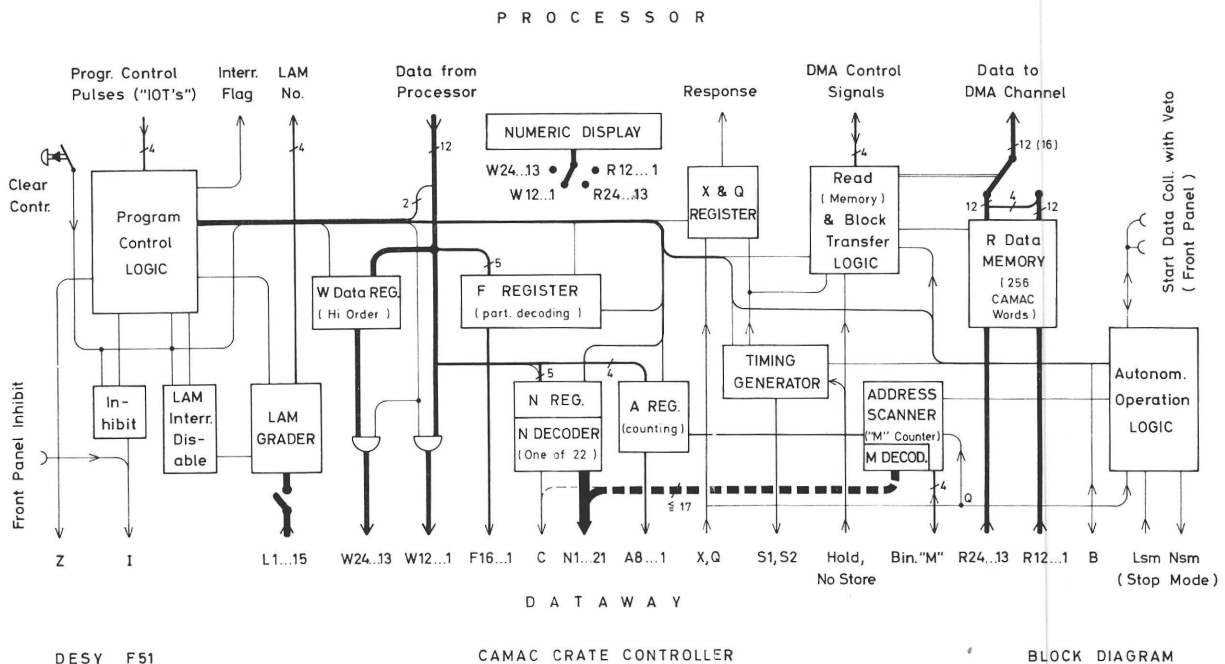


Fig. 1 Block Diagram of the Crate Controller

* D-2000 Hamburg 52, Notkestieg 1.

NEWS

CAMAC PRESENTATIONS IN USA

The IEEE Education Activities Board in cooperation with the Nuclear and Plasma Society staged a one-day tutorial course on CAMAC on 26th March 1974 in New York. Fifty people attended from diverse fields and the interest was high.

Several papers on CAMAC are also to be given at the IEEE Industry Applications Society and the Instrument Society of America meetings in October 1974.

CAMAC MULTI-BRANCH SYSTEM FOR CONTROL DATA 3100 COMPUTERS

by

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Received 18th February 1974

SUMMARY A CAMAC interface for the CDC 3100, handling up to eight CAMAC branches, is used in conjunction with a system controller that provides extensive LAM-handling and modes of operation. The system will be used to control the Karlsruhe Isochronous Cyclotron, and is programmed partly in CAMAC IML and partly in CDC Assembler.

INTRODUCTION

The Karlsruhe Isochronous Cyclotron is presently equipped with a CAMAC-supported control system. The available computer is a CDC 3100 which has been used also for the various on-line experiments conducted at the cyclotron. In addition to conventional units (magnetic tapes, discs, card reader, etc.) the peripheral equipment includes several non-standard interfaces. A system controller¹ (24-bit unit) developed in Karlsruhe, and capable of performing complex CAMAC functions by hardware, was appropriate for the connection to CAMAC. The system controller was modified only where this was required by the revision of the CAMAC specifications or by IML software³. Adaptation to CDC I/O standards was made in the CAMAC interface. Special importance was attached to easy checking by the user (essential in the test phase), simplified LAM handling and the possibility of extension.

For technical reasons the presently employed system for cyclotron control called for a separate branch. A second branch incorporating a system controller of the same type is available for connection of other on-line experiments.

SYSTEM CONFIGURATION

Fig. 1 is a schematic diagram of the system configuration. The CAMAC interface meets the hardware/software specifications of a CDC standard 24-bit data channel⁵. Input/output devices are normally connected to a data channel via specific interfaces. In a similar manner the CAMAC branches are connected to the computer via the CAMAC interface. Besides this connection, compatible with every CDC computer of the 3100 series, the CAMAC interface is provided with a DMA channel connection (24 bits) with automatic incrementing of addresses. The DMA channel serves mainly to connect autonomous transfers which are caused by specific alarm conditions in the CAMAC system. (The DMA channel developed here is not a CDC standard option.) As protection against noise the entire branch highway was installed in a flexible corrugated metal tube with insulation against other external potentials. This shielding brings the individual CAMAC crates to the computer potential.

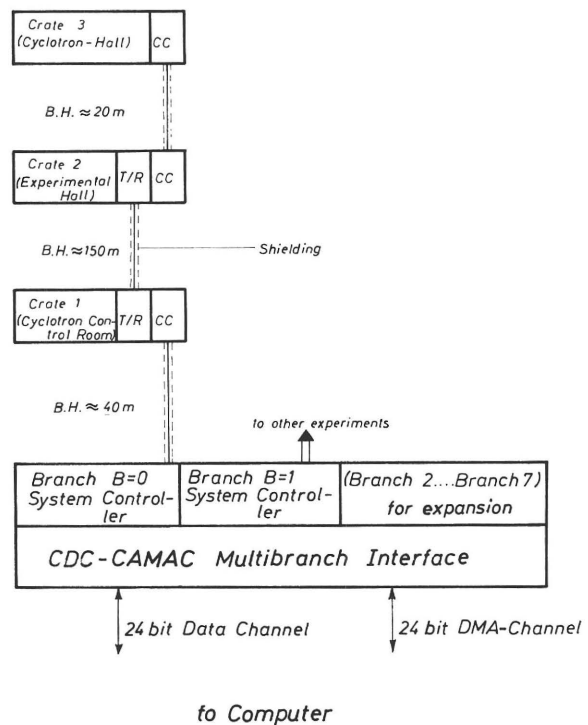


Fig. 1 Block Diagram of CDC-Multibranch-System
CC: Crate Controller, T/R: Transmitter/Receiver,
BH.: Branch Highway

Connections between the CAMAC modules and the various measurement and control units are physically isolated by opto-couplers. Special transmitter-receiver modules were inserted between crates 1 and 2 to convert the unipolar TTL levels to bipolar signals, because of the considerable length of the highway. If it had been developed earlier the serial branch would also have been worth considering for this application. Each crate has a LAM grader⁴ suited to the system controller used here.

CAMAC INTERFACE

First of all, the CAMAC interface (lower part of Fig. 2) contains the necessary level adaption. The following options make system handling more convenient to the user, relieve programming, and increase the transfer rate. These options are the registers for CAMAC command and operands, for computer instructions, interrupts and interrupt masks, and quite a number of address registers with automatic increment for autonomous transfers. All the registers are decoded and displayed on the front panel. These registers are loaded via the program-controlled data channel, for instance by the computer instruction 'LOAD CAMAC COMMAND'

and a subsequent 24-bit output representing BCNAF. Appropriate computer instructions are available for the other registers, e.g., 'LOAD ADDRESS REGISTER', followed by data giving the initial and final core memory addresses for the modules involved in autonomous transfers (max. 16 per branch).

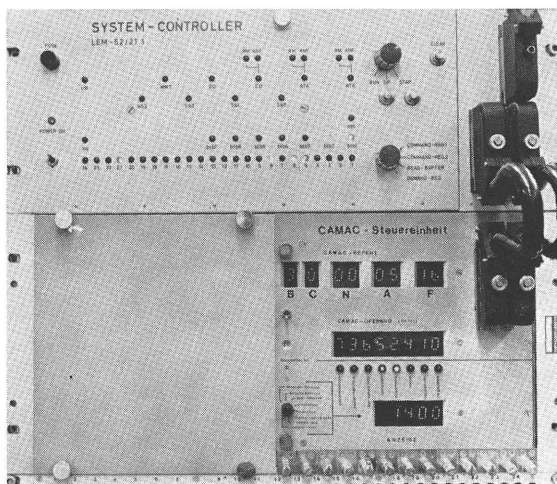


Fig. 2 CAMAC Multibranch Interface for CDC 3100 and System Controller

When handling a LAM demand we distinguish between LAM's resulting in normal interrupts (IT's) i.e. programmed data transfers, and LAM's causing faster autonomous transfers (AT's) via DMA into a core memory buffer area. Twelve IT's are provided in the multibranch interface: one per branch and four specific IT's, namely 'READY BUSY', 'END OF BLOCK TRANSFER', 'ADDRESS OVERFLOW', and 'ABNORMAL END OF OPERATION'. All IT's can be selectively set, cleared and masked. Each AT (max. 128) increments the initial address held for it and leads to ADDRESS OVERFLOW IT on attaining its final address. IT's and status have their own lines to the computer (for further details, see LAM-HANDLING).

SYSTEM CONTROLLER

The system controller (Fig. 2, upper part) designed for connection to a 24-bit computer, is able to serve a fully developed branch. Besides the single word transfer there are the various familiar block transfers and module to module transfer (Fig. 3). The number of A and N increments and their size can be stated. The block transfers mentioned can also be effected in a cyclic repeat mode. There are 16 instruction registers available for autonomous transfers. Following an alarm condition, up to 16 modules spread over the branch can execute the CAMAC instruction assigned to them and store data in the similarly programmed core memory buffer. The autonomous transfer has the highest, the module-to-module transfer the lowest priority. The operational modes interrupted by higher priorities are subsequently continued without loss of data. Eight interrupt

levels are provided in addition: one IT per crate and one for the system controller (Time Out or prohibited mode of operation). Instruction and status registers can be reread; in addition, the contents of these registers—and all other significant states—are displayed on the front panel.

LAM-HANDLING

The most essential aspects of LAM-handling using the LAM grader⁴ will now be summarized. The 23 LAM's possible in a crate are stored in the LAM grader and can be masked or rearranged. As a result of a LAM, a branch demand (BD) is generated from the crate, whereupon the system controller requests the 24 bit alarm pattern GL1...GL24. The LAM grader used assigns to each crate only one GL-line corresponding to its crate number, and resulting in one crate interrupt 1...7. The GL8 line is assigned to the system controller. The remaining GL9...GL24 are assigned by the LAM grader as required and lead to autonomous transfers. Each crate interrupt causes a branch interrupt, and hence a computer interrupt. The computer must trace back the LAM, by reading the status register in the CAMAC interface, system controller, LAM grader and module, before it can take appropriate action. This takes 50-100 μ sec, and could become time-critical with the possibility of 162 LAM's per branch. On the other hand, the 16 autonomous transfers per branch have typical reaction times of 4-10 μ sec. After this time the data are already stored in the core memory. Unless a time-critical feature of the system calls for immediate action, the data may be processed after the appropriate memory area has overflowed and caused an address overflow IT.

CONCLUDING REMARKS

Work on this system started two years ago with 2 \times 0.5 men engaged in it. On account of the required configuration almost no hardware, besides that indicated in the references, and no software at all could be taken over. The CAMAC-IML language proposed in November 1972, and its subsequent developments, had a productive effect upon the hardware. Certainly, simple methods of implementation² of these IML-statements will open CAMAC to a major group of users.

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1. Ottes, J.G., CAMAC System Controller für CALAS-Endstelle, KFK 1412, Jun. 71.
2. Kneis, W., Implementation of CAMAC IML in an Assembler Language Environment (See the *Bulletin*, page 28).
3. ESONE Software Working Group Papers, SWG-41/73, SWG-37/73 (unpublished working papers).
4. Heep, W., Ottes, J., Tradowsky, K., Alarmverarbeitung und autonomer Datentransfer, GfK, Ext 22/71-7, Nov. 1971.
5. CDC-I/O-Specifications, CDC-Nr. 600 48 800.

SOFTWARE

TRANSLATING CAMAC TEST PROGRAMS FROM INTERPRETIVE TO ASSEMBLED BASIC

by

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Received 14th February 1974

1

SUMMARY Test programs for CAMAC modules and systems can be written and changed easily by using interpretive BASIC. A major disadvantage is the slow execution speed. A compiler has therefore been written for the PDP-11 to translate tested BASIC programs into macro-assembler programs.

INTRODUCTION

Since late 1971 test programs for CAMAC modules and systems have been written at the KFA Jülich in interpretive BASIC on the PDP-11. These programs can be written and debugged easily by 'hardware people'. Particularly because our interpretive BASIC is running under DOS (Disk Operating System) with all its file-handling capabilities, testing and debugging are performed quickly. But the major disadvantage of interpretive BASIC is its slow execution speed. To overcome this disadvantage a compiler was written to translate tested BASIC programs into Assembly language programs. Then the user only runs the macro-assembler and linker to get a load module for execution under DOS.

IMPLEMENTATION

Since the compiler translates only tested programs, it relies upon the syntax analysis performed by the interpretive BASIC and does no further syntax checking itself. Therefore the input code can be translated into macroassembler code line by line.

For some BASIC statements the powerful MACRO 11 allows direct replacement of a BASIC statement by a macro statement.

All the line numbers in the BASIC program are changed into labels, all variable names into address names. For arithmetic calculations the same floating point package is used as in the interpretive system. This is especially important for speed comparison.

Whereas the interpretive 'Evaluate' routine (EVAL) performs calculations at runtime, the compiler uses a slightly modified EVAL version for parsing the arithmetic expressions, thus improving execution speed at runtime.

Speed improvement also takes place because the variables, arrays and subroutine returns are directly accessed by their addresses instead of searching for their names in the interpretive version.

The CAMAC-BASIC calls are simply replaced by CAMAC macros. There are two groups of CAMAC macros depending on the need for address modification at runtime.

RESULTS

The short example shows compiler input and output. One can see the line-number to label

conversion and the high packing density of BASIC source code. For example, line number 30 is converted to label DA0000, and the BASIC statement calling for a CAMAC write operation is compiled into 14 lines of assembly language code. The compiler program can be run on a 16K DOS configuration where the compiled code is transferred to the disk line by line. The speed improvement (depending on the programs) is a factor of 15 to 20.

A further advantage of the compiled code is the possibility of loading and running these program segments in other systems (like Real time systems or small machine configurations without operating systems, where calculations are performed by the program).

SOURCE

```
#KB: <CAMA
10 FOR I = 1 TO 10
20 LET X = 15 * 15
30 CW 16, 1, 16, 0, X
40 NEXT I
50 END
R
```

OUTPUT

```
KB: <CAMA.PAL
.CSECT
.GLOBAL ETOA, COS, SIN, ATN, LOG, EXP
.GLOBAL SGN, SQRT, CRLF, ERTEST
.GLOBAL ADDF, SUBF, MULF, DIVF, CHFF
.GLOBAL INT, PWRF, OUTTTY, ABS, ERROR
.GLOBAL FIXSD0, NORMD0, CAMVA, SK
.GLOBAL CAADR, ADDR, FUNC, CRTNR, STNR
.GLOBAL CCSR, CLEAR, ZS, CSR, SBADR, HOW
.GLOBAL HOR, SAVE, CAMA, SURE, UP, DOWN
.GLOBAL ARAYD, RND, RNDM
.MCALL .PARAM
.PARAM
$00000: CCC I, AA, AB
BA0000: FOR I, AA, AB
CA0000: MOV #AD, Z1
MOV #AC, Z2
MOV #SA, Z2
MOV (Z0)+, (Z2)+
MOV (Z0)+, (Z2)+
MOV (Z0), (Z2)
MOV #SA, Z0
JSR PC, MULF
JSR PC, ERTEST
MOV #K, Z0
MOV #SA, Z2
MOV (Z2)+, (Z0)+
MOV (Z2)+, (Z0)+
MOV (Z2), (Z0)
DA0000: MOV #X, R0
MOV (R0)+, R2
MOV (R0)+, R3
MOV (R0)+, R4
JSR PC, CAMVA
MOV R2, S0+2
MOV R3, S0
WRITE 16, 1, 165000, 1, S0 0
CLR 0+2
CLR 0+4
BIT #200, 165400
BEQ .+16
MOV #040000, 0+2
MOV #100001, 0+4
EA0000: NEXT I
FA0000: END
```

Source: Example of BASIC Source Code used as Input to the Compiler

Output: Corresponding Macro-Assembler Code Generated by the Compiler

This way of programming, which is important for untrained users, will hopefully encourage people to use a computer-CAMAC system as development tool.

IMPLEMENTATION OF CAMAC INTERMEDIATE LANGUAGE (IML) IN AN ASSEMBLER LANGUAGE ENVIRONMENT

by

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Received 18th February 1974

SUMMARY This paper describes the implementation of a subset of an early version of CAMAC Intermediate Language (IML) in the host language environment of the COMPASS assembler for the CDC 3100.

INTRODUCTION

Faced with the problem of using CAMAC with a CDC 3100 computer via our own multi-branch controller², we had also to find a quick solution for CAMAC programming. CAMAC IML appeared to be a good approach for handling CAMAC devices, as we wanted to make these facilities available for user programming.

Firstly, CAMAC IML is an international standard. Secondly, due to its straightforward definition, it is a language which, on the whole, is context-free. This is a good condition for backup-free translation of IML in one pass³. However, CAMAC IML is by definition only an I/O language for handling CAMAC devices. It must, therefore, be embedded in a host language. In our implementation we have chosen the COMPASS assembler¹ of the CDC 3100 as the host language.

CAMAC IML SUBSET

The version of the CAMAC IML actually implemented is similar to the definition of the macro syntax of IML proposed by the ESONE Software Working Group (SWG)⁵ in June 1973.

TRANSLATION

A CAMAC IML-assembler program is translated in two steps. This method is illustrated in Fig. 1.

Firstly, a main processor analyzes the whole host/parasite program (Fig. 2a) to recognize IML and assembler statements. Whenever IML statements are present, the main processor passes control to the IML compiler which translates them into the appropriate object instruction set of the mnemonic assembler language, COMPASS¹. The assembler part of the program is not affected by this step. The object code of the translated IML statements is inserted in the host assembler environment at the locations where the IML statements had formerly been. For examples of the generation of this in-line code refer to Fig. 2.

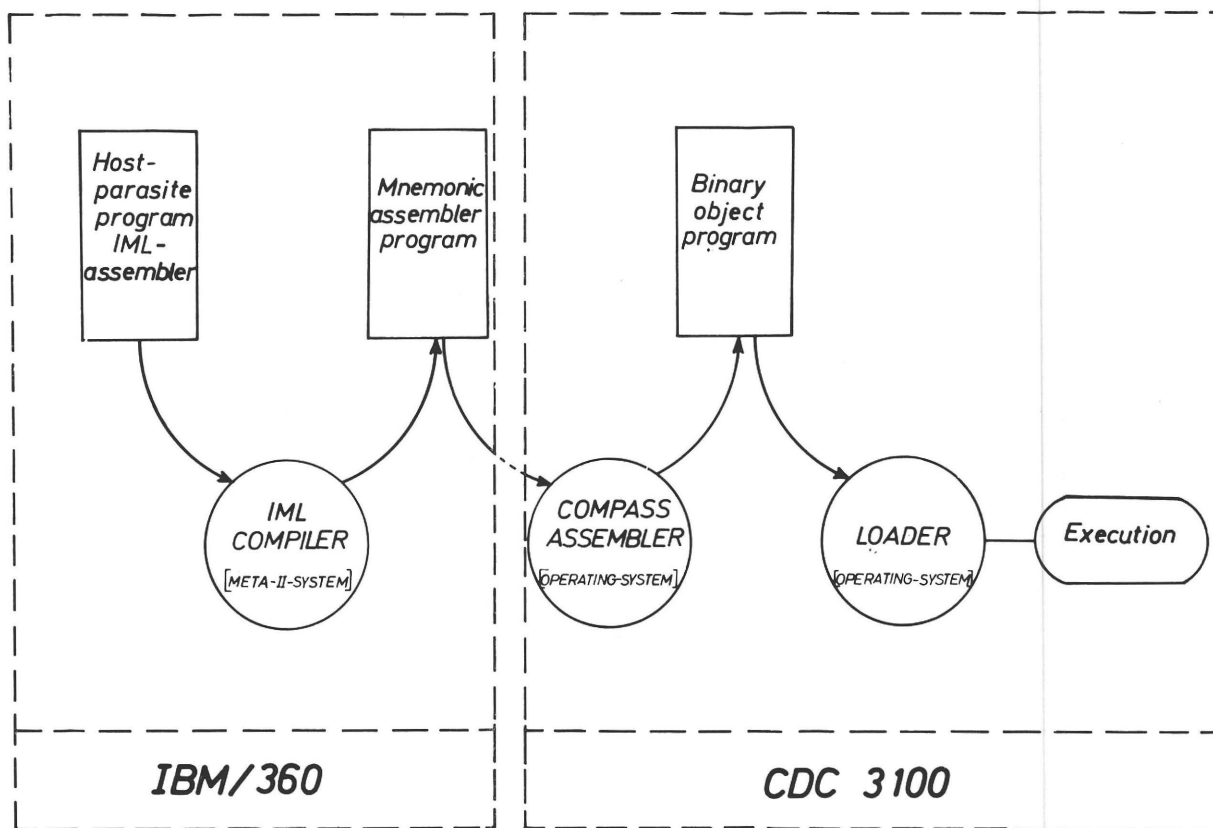


Fig. 1 Method of Translating IML Programs

After this IML translation, the whole resulting object program is in the mnemonic COMPASS assembler form (Fig. 2b). In the second step this program can be assembled like any other assembler program by the COMPASS assembler of the operating system (Fig. 2b, Fig. 2c).

In this implementation, switching between the two languages is controlled by Job-Control-Language (JCL) statements. As can be seen from Fig. 2a, the statement—\$*,I—indicates IML statements and the statement—\$*,A—indicates the assembler text. The statement—\$—serves to start the translation of IML statements.

TRANSLATOR

To obtain a straightforward and relatively quick object code the CAMAC IML is translated by a compiler. The compiler is produced by means of a metacompiler system^{3,4} running on a nearby IBM/360-165. This way has been chosen because the CDC 3100 is extensively used for on-line experiments, whereas the IBM/360 can very easily be accessed via the IBM terminal system TSO. Besides the advantages of saving core, computing time, storage media etc. on the CDC 3100, this procedure allows the use of the enormous external storage media and excellent source program editing facilities of the IBM/360. In practice the translation of IML is done on the IBM/360 and assembling of the COMPASS object program is done on the CDC 3100 (Fig. 1).

Based on the principles of the META II system proposed by D.V. Schorre⁶, the whole META II/X system⁴ written in FORTRAN IV, takes about 120k bytes of core, including a large program buffer and various table areas. A practicable minimum version could have about 60k bytes of core (25k for the program and 35k for the data area). For example, typical translation times for an IML-compiler description are 5-6 sec and the average compile time for one IML statement is about 100msec.

With this system a compiler for IML can be defined by writing the IML compiler description in terms of the metalanguage which closely resembles the Backus-Naur-Form (BNF). This description contains the syntax and semantic definition for IML. The semantic definition is expressed in terms of the mnemonic COMPASS assembler instructions. This description is translated into an internal representation which can be interpreted by a subsystem of META II/X, the META simulator.

To process the translation of IML statements the internal representation of the previously produced IML compiler is loaded, and so the META simulator can execute the translation. These two parts take about 12k bytes of core without program buffer area. Since the META II/X system works as a one-pass compiler, there is no need to hold large program buffer areas. In addition, the subsystem, META simulator and internal representation of the IML compiler can, in principle, run on another

computer with FORTRAN capabilities, but this has not yet been verified.

CONCLUSIONS

This implementation has the following general features:

- Relatively quick and convenient programming of the CAMAC handling part of programs.
- Short execution times for the CAMAC IML instructions (15-30microsec.).
- Additional data processing possible in the assembler. For problems which can be solved by FORTRAN, the linkage from assembler to FORTRAN programs can be realized via the FORTRAN subroutine calling mechanism provided by the operating system.
- Ease of compiler writing (in this case for CAMAC IML) and of extending it by means of the metacompiler system.
- Lack of means of debugging source programs during execution or immediately after error detection. This is due to the fact that IML is compiled on the IBM/360. (However software and hardware developments are planned to reduce this dead-time.)

This concept can be extended easily. Not only special user subroutines can be programmed in this way, but it is also possible to write general purpose subroutines for servicing the various module interrupts (LAMs) by use of IML and the assembler. Therefore, an extension of this concept is planned to allow LAM-synchronized IML statements for user programming.

The method of producing IML compilers with the META II/X system is characterized by easy application, very good bootstrapping, and expansion properties. Therefore, it can be adapted to the final version of CAMAC IML now being defined by the ESONE-SWG. Similarly, successive extensions can be made starting from a first relatively small subset of IML. In so doing, only the additional part of the IML facilities need be incorporated in the IML compiler description.

REFERENCES

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2. Karbstein, W., Kögel, B., A CAMAC Multi-Branch System for the CDC 3100 Computers (to be published in the *CAMAC Bulletin*, this issue).
3. ESONE Software Group Paper, SWG-13/73 (unpublished working paper).
4. Kneis, W., META II/X—Beispiel eines Metacompiler-Systems (to be published).
5. ESONE Software Group Papers, SWG-41/73 and SWG-37/73 (unpublished working papers).
6. Schorre, D.V., META II, a Syntax-Oriented Compiler Writing Language. *Proc. of the 19th Natl. ACM Conf.*, (1964), D1.

NEW PRODUCTS

DATA MODULES (I/O Transfers and Processing)

Digital Serial Input Modules

12-Channel, 16-Bit Scaler

This single width module Type 9054, which conforms to the CERN SPS2135 Specification, contains twelve 16-bit binary scalers, accessed by sub-addresses A(0) to A(11). Overflows are stored in a 12-bit register at sub-address A(15). The scalers have a guaranteed maximum count rate of 6MHz. Inputs are accepted on twisted-pair cables, giving rejection of spikes and common-mode signals. All scalers are gated by a common gate input on a twisted pair, or by a single-ended gate input which can be indefinitely cascaded. The scalers and overflow register are individually controlled and read by dataway commands.

Ref. Nuclear Enterprises Ltd.

Digital Parallel Input Modules

Parallel Input Gate

Two versions of this single-width module are available, the 9049A, which conforms to the CERN SPS2133 Specification, and the 9049B. The 9049A accepts 16 bits of data and a data strobe and provides an acceptance signal in reply. In this way 'Handshake' Operation can be achieved and dataway L generated without using the coaxial input. A +6V supply, fused at 250mA, is available at the front panel.

The 9049B accepts 24 bits of data and relies on the coaxial input to ensure that data is settled before reading. By internal link option the module can accept 22 bits of data and provide the 'Handshake' Operation of the 9049A. No fused output supply is provided.

Ref. Nuclear Enterprises Ltd.

Digital Output Modules

Output Register

This single-width module is available in two versions, Model C-OC-24 with a 24-bit data register and TTL output or Model C-OR-16 with a 16-bit data register and reed relay contact outputs. Both models serve to supply data to an external instrument via the CAMAC Dataway. The module contains a data register which can be set via the dataway and connected by choice of logic to the corresponding output plug. For monitoring purposes, the data held in the registers can be read via the dataway.

The timing of the data flow between the dataway, the module and the external instrument is controlled

by the timing signals T_i and T_o available on the front panel as well as normal CAMAC Status and Command signals. Timing with respect to the demand and output of new data can be carried out in either the "Handshake" or "Strobe" modes. In each case the instrument differentiates between Master and Slave modes.

Ref. Wenzel Elektronik

Real Time Clock



This single-width module Type 9064 contains a register which counts in days, hours, minutes, seconds and tenths of seconds. It may be synchronised to the mains frequency by direct connection to the Dataway 117 volt ac line or alternatively, it may be clocked by an external pulse generator. The unit is suitable for 50 Hz or 60 Hz line frequencies. Also contained in the unit is a counter which may be preset to a value from 1 to 99 and then decremented at a rate derived from the main counter as determined by setting a front-panel switch. This provides a counting interval of between 1 second and 99 hours. When this period terminates, the module LAM signal is asserted and may be used to trigger an event such as a channel scan in a data-logging system. A front-panel enable signal is provided for the period of the count so that scalers may be gated. Indication that counting is in progress is provided by a front-panel LED indicator. This unit is in production.

Power requirements: +6V, 1.2Amps

Ref. Nuclear Enterprises Ltd.

Digital I/O, Peripheral and Instrumentation Interfacing Modules

NIM ADC to CAMAC Interface

This single-width module Model C-AI-2 is designed to allow NIM ADC's similar to the Wenzel Elektronik MAD-8A to be connected to the CAMAC Dataway. It features a selective masking capability and can operate with a single ADC with a live-time signal pulse or with two ADC's in the multiplex mode. In the multiplex mode the ADC outputs may be bussed or connected via a Wenzel Elektronik Multiplex Unit. The module has LAM 1, LAM 2, LAM 3, Clock or Live-Time and ADC Busy signals available on Lemo sockets on the front panel, with a 34-pin Cannon connector for the ADC or Wenzel Elek-

tronik Multiplex Unit and normal CAMAC connector on the rear panel.

The ADC Busy signal on the front panel may be used to gate on an external clock generator for use with a scaler to obtain a digital readout of a live-or clock-time measurement.

Ref. Wenzel Elektronik

Measuring Instrument Connector Module

A single-width CAMAC module connects chemical and physical analysis equipment and meteorological meters used for the acquisition of sensor data in automatic surveillance systems. The CAMAC interface corresponds to the recommendations for standardisation of automatic measuring networks for air surveillance by the Bundesministerium des Innern (Federal Ministry of the Interior) of the FRG.

The measuring instrument connector can be tested by a built-in reference. One module can be connected with two instruments. Each connection has the following facilities:

1 analog measuring input, 16 digital inputs for instrument scanning, 8 digital inputs for instrument identification, 8 digital outputs for instrument status information, 8 digital outputs for instrument control, 1 power supply output (auxiliary voltage) 24V, 50mA.

Ref. Dornier AG.

Long-Distance Transmitter Module

To transmit data via the public telephone network, this single-width CAMAC module permits a dialogue with a modem (D 200 or D 1200 S) via the V 24 interface (CCITT) or with an automatic selector unit (AWD)

Data transmission is in the START-STOP operation (asynchronous data transmission) with 8-bit-words; the transmission rate is selectable within 600 and 1200 baud. According to the ECMA 16 and ECMA 24 standards, errors in data transmission can either be prevented by using parity even (7-bit-transmission) or cyclic block protection (code-transparent 8-bit-transmission).

All functions in the module are software-controlled and can thus be adapted to a wide variety of operating conditions and transmission procedures.

Ref. Dornier AG.

Digital Handling and Processing Modules

2048-Word, 16-Bit Store

This double-width CAMAC module Type 9061 contains a 16-bit \times 2048 Random Access Memory which may be accessed either via the dataway or from the front panel. A priority selector permits maximum access by both interfaces simultaneously while at the same time allows the necessary refresh cycles to be performed automatically. A memory increment

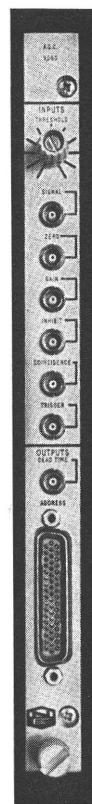
facility is available at the front-panel interface, and data may be written in or read out along a two way input-output bus using "handshake" timing. Data can either be a 16-bit word or two 8-bit bytes. Cycle time is 750ns. A 4096 word version is also under development.

The design of this unit was originated by Daresbury Nuclear Physics Laboratory.

Ref. Nuclear Enterprises Ltd.

Analogue Modules

Analogue to Digital Converter



This single-width module Type 9060, now in production, converts input analogue voltage signals to digital binary words, with a precision of 12 bits using the Wilkinson technique. The output can be transferred to the dataway or directly to the storage module Type 9061. The module stores 8 conversions before accessing the computer (by generating LAM) and transfers the data as a block, resulting in a derandomised input rate to the computer, and a faster maximum rate of data accumulation.

This module offers excellent compactness without sacrificing versatility. A single Write command, subsequently stored in the control register of the module, presets the range, channel width, digital back bias, coincidence mode and conversion mode. The front panel carries input/output connectors and the threshold potentiometer. Also included on the front panel are a trigger input for use in dc sampling, a fast inhibit, and a coincidence input where the signal duration defines coincidence or anticoincidence timing. Provision has been made for spectrum stabilisation using the Gain Adj and Zero Adj inputs.

Ref. Nuclear Enterprises Ltd.

Quad Charge Digitizer

The QD410 Charge Digitizer is a single-width module that contains four separate 10-bit charge-sensitive ADC's with individual gating inputs and buffer registers. The unit is designed to operate on negative input signals (as from fast photomultipliers) in the range of 0-250 pC. Each channel has a monitor output which provides a convenient method of monitoring the actual switching time and the dc current applied to the integrator. Other significant features of this unit are the fast gate-switching time of < 1 nsec, a conversion time of 20 μ sec maximum, full LAM logic, excellent linearity and temperature stability.

Ref. EG & G/ORTEC

SYSTEM CONTROL (Computer Couplers, Controllers and Related Equipment)

Interfaces/Drivers and Controllers

Universal System Controller

This high capacity, universal system controller is largely independent of the computer on account of its modular design. The controller consists of the following three units: the branch driver, the interface program and a computer-specific unit, the adaptor control element. The data between computer and controller can be transferred via two channels, the programed channel or the DMA-channel.

The system controller is equipped with a micro-programable control element and a RAM-store as well as with a total of 16 channels which store the commands and data for the transfer. The system controller can thus be operated in the following two modes:

1. *Program-controlled operation*

The output or input of data is determined by the program.

2. *Automatic operation*

Upon a request which originates e.g. from a CAMAC module, the interface signals automatically to the computer to transmit data between core memory and adaptor control unit.

As the computer receives no interrupt signal, the transfer of a data word does not lead to a program interruption. If, however, a block transfer has been made or in case of an error, the system controller generates interrupts.

This concept allows a low computer load at the same time as high data transfer rates.

Ref. Dornier AG.

Units Related to 4600 Branch or Other Parallel Mode Control/Data Highway

Priority Grader

This single-width module Type 9037, now in production, accepts a LAM pattern via a rear-panel, 52-way, Cannon connector, grades the LAM's according to a prepatched priority and provides a 4-bit graded LAM pattern. This pattern is directly available from the 52-way connector or is read via the Dataway using a function 0 command. Up to 15 LAM signals may be graded and the result is presented as a binary code from 1-15. A 4-bit latch is used to prevent transitions occurring when the

module is addressed or during a graded LAM operation.

This unit can be used in conjunction with a 9030 Controller, 9016 Crate Controller A1, or EC 372 Controller.

Visual indication in binary code is provided together with an interrupt level which is generated when any patched LAM is set. Provision is also made for accepting a front panel interrupt.

Power requirements: +6V, 200mA

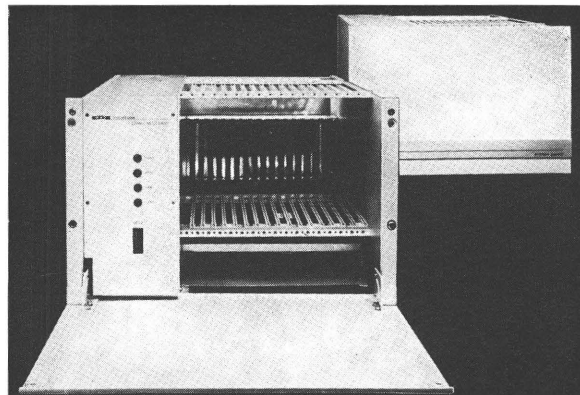
Ref. Nuclear Enterprises Ltd.

CRATES, SUPPLIES, COMPONENTS, ACCESSORIES

Crates and Related Components/Accessories

CAMAC Minicrate

A CAMAC Minicrate is now available that includes the Dataway, power supply, and blower unit. Eight stations are occupied by the power supply as an integral part of the 19" crate. The front datum of the 17 stations available for CAMAC units and of the power supply is inset by 6 cm with respect to an overall front plate covering all units and their front-panel connections.



System cables for outside connections are directed to the bottom or rear of the crate. The overall front plate can be equipped with elements for system control and display functions. The minicrate should stimulate new ideas to promote an increased use of CAMAC especially for mini-systems as needed, for instance, in medicine and laboratory uses.

Power supply: +6V/15A, -6V/5A, ±24V/2A.

Ref. EDS Systemtechnik

Recommended or Standard Components/Accessories

CAMAC Dataway

A new CAMAC Dataway Type 1186 is now available that complies with the requirements of the CAMAC specification EUR 4100e (1972) and is therefore compatible with all CAMAC crates.

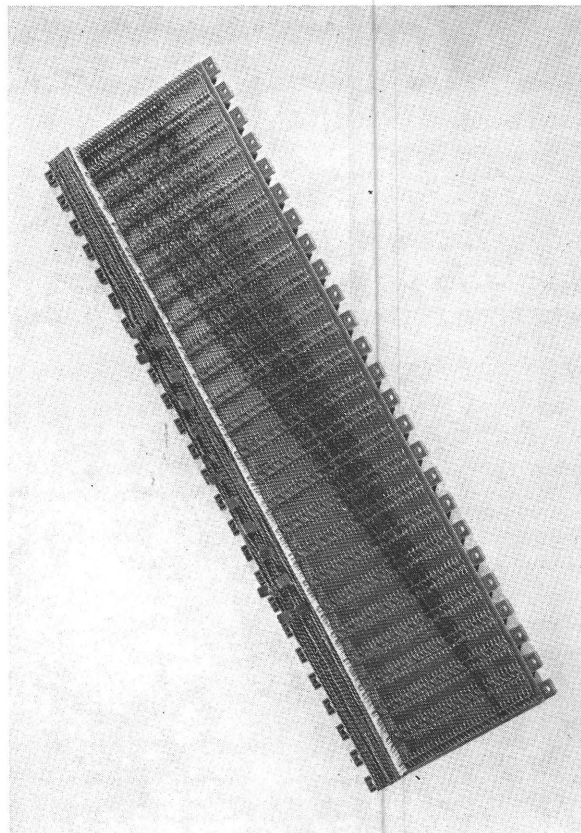
Specification:

1. printed circuit board with approved CAMAC edge-connectors;
2. 'L' and 'N' connections made by Wire-Wrap or Termini-Point;
3. the 13 busbars, in accordance with EUR 4100e para. 8 table X, are isolated copper strips with input via 'fast-on' tabs.

Additional wiring and other special features may be incorporated to suit individual requirements.

The Dataway Type 1186 is inexpensive and delivery time is short.

Ref. KARL WEHRMANN



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NEWS

PRESENTATION OF CAMAC IN MILAN

CAMAC was presented to a meeting of the Associazione Nazionale Italiana per l'Automazione in Milan on 7th May, 1974.

Various aspects of CAMAC and of the ESONE Committee were dealt with by different speakers

from Laboratories in Italy which are members of ESONE.

The meeting was attended by about 50 people who were largely drawn from Italian industrial companies.

ACTIVITIES OF THE CAMAC WORKING GROUPS

The ESONE Committee in Europe and the USAEC NIM Committee in America have both authorised different working groups to investigate specific aspects of CAMAC. The European and American working parties are performing their activities in close collaboration.

ESONE-CAMAC WORKING GROUPS

Dataway Working Group

Chairman: R. Patzelt, IEMTH, Wien

The Serial System Description has been completed in close collaboration between the NIM and ESONE Working Groups and published as document ESONE/SH/01. It is intended to be guidance for interested CAMAC-users working on early implementations of serially driven systems. The final, definitive specification will incorporate experience gained by using this Description.

Correction and modifications will become necessary during this period, and will be published. The first set has already been prepared and agreed upon by NDWG and EDWG. Besides clarifications and minor improvements, it includes changes that allow for multicrate-operations and improved data-byte synchronisation properties. Further improvements are under consideration concerning the signal standards, the mechanism of bypass and loop collapse control, and the implementation of the 3-byte memories associated with demand message generation. A second set of amendments is intended to become available around the end of the year.

The performance of the Serial System and proposed additions and modifications are being tested by computer-simulation that checks failure-rates and transmission-efficiency.

The compatibility of the Serial System with other relevant standards, especially the proposal of the IEC/TC 66 for a Digital Bus for programmable measuring instruments, is under investigation. The minimum requirements for connecting single instruments or CAMAC crates with low rates of data transfer to the Serial Highway are under consideration.

Modes of Block Transfer additional to those defined in EUR 4100 have been specified, taking into account technical developments and the demands of efficient programming and real-time data acquisition.

Concerning the maintenance of the established Specifications, an announcement changing the state of the Branch Highway Lines BV1 to BV5 from RESERVED to FREE has been agreed by NDWG and EDWG. It is also proposed to assign BV7 to a synchronising signal for block-transfers.

Software Working Group

Chairman: I.N. Hooton, AERE Harwell

The ESONE and NIM-CAMAC Software Working Groups, having a technical definition of IML, are now preparing a document that can be endorsed

by the ESONE and NIM-CAMAC Committees. It is expected that preliminary copies of this document, containing the semantic definitions and an appendix giving a suggested macro-expansion syntax, will be available shortly.

An ESONE Software Working Group Sub-Group has been set up, under the Chairmanship of Professor I.C. Pyle, to prepare proposals on the use of BASIC for testing CAMAC hardware units. These proposals will be submitted to the full Working Group for approval before being recommended for publication.

The need for close collaboration with the NIM-CAMAC-Software Working Group has been most significant in the recent discussions on IML. Interaction both with the NIM Committee and with the ESONE Dataway Working Group, has shown its value in the recent resolution of the problems associated with block-transfers.

Information Working Group

Chairman: H. Meyer, BCMN JRC, Euratom, Geel, Belgium

The Working Group considered further possibilities for the improvement of the content and layout of future Bulletins.

The publication of information on CAMAC, its applications and applicability in the form of interviews will be continued. Because of the increasing content of the Product Guide, its publication in full will be made in every second issue of the Bulletin in future. Only amendments to the previous contents will be published in the alternate issues. The sample Software Guide published initially with Issue No. 9 appears in an amended form in this Issue. The suitability of information content and classification rules will be considered further, hopefully with the support of readers.

A series of introductory papers is planned which takes into account that, to an increasing extent, potential CAMAC users are not necessarily familiar with the more fundamental features of systems for measurements and control. More descriptions of CAMAC features for dedicated applications are to be also considered.

An index of CAMAC papers, non-commercial news and announcements that have been published with *CAMAC Bulletin* Issues 1-10, is attached to this Issue.

NIM-CAMAC WORKING GROUPS

Dataway Working Group

Chairman: F.A. Kirsten, Lawrence Berkeley Laboratory

The principal activity of the NIM Dataway Working Group so far in 1974 has been with regard to the CAMAC Serial System. The Serial System Description has been published as USAEC report TID-26488 and as ESONE document ESONE/SH/

01. Implementations of the Serial System are currently underway and discussions have continued on clarifications and other matters, including block transfers, both at meetings of the Serial System and Block Transfer Subgroups and at the Working Group meeting in March. The March meetings were held at the Kitt Peak National Observatory in Tucson, Arizona and included a joint meeting with the Software Working Group on the subject of block transfers. The Working Group members also visited the Kitt Peak National Observatory installation on Kitt Peak, south of Tucson, to see the telescope installations and the associated CAMAC systems. The Working Group is scheduled to meet in July at the Los Alamos Scientific Laboratory in New Mexico and also in conjunction with the Nuclear Science Symposium in Washington, D.C. in December.

Software Working Group

Chairman: R.F. Thomas, Jr., Los Alamos Scientific Laboratory

The NIM Software Working Group has worked closely with the Dataway Working Group in the formulation of the CAMAC Serial System Description (USAEC report TID-26488, ESONE document ESONE/SH/01) and in subsequent discussions regarding the Serial System. A joint NDWG/NSWG meeting on March 20 was concerned primarily with block transfers and particularly with the significance of Q in block transfers. The meetings of the NSWG on March 21 and 22 included discussions of IML, BASIC extensions, FORTRAN subroutines and mnemonics for F codes. The next NSWG meetings will be contiguous with those of the NDWG at Los Alamos in New Mexico in July and in Washington D.C. in December.

NEWS

FUSION RESEARCH CENTRES ADOPT CAMAC

The Data Acquisition Co-ordination Committee (DACC)*, representing eight European Centres engaged in Nuclear Fusion Research, reports that it has adopted CAMAC for interfacing data acquisition/display peripherals and machine control devices to the minicomputers used to aid plasma physics diagnostics and machine monitoring. As an adjunct to this decision, IML is also to be introduced as a first step towards software standardisation.

The DACC was set up during the latter part of 1973 to advise the Committee of Directors of the Laboratories having Contracts of Association with Euratom on the choice of hardware and software for data acquisition and processing purposes related to the Euratom Fusion programme. In carrying out this task, the DACC is required to provide liaison between the member laboratories and the various Standardisation bodies in the fields of electronics and data processing.

The importance of the decision to standardise the means of connecting peripheral devices to small computers arises from the arrangement whereby Euratom gives preferential financial support to the building of certain approved experiments in return for which the 'host' laboratory provides facilities for physicists from other Associated laboratories to carry out physics experiments upon the experimental assembly. With the increasing use of small computers in the experimental environment it is clearly of advantage for visiting physicists to be able to connect their diagnostic equipment to the 'in house' computer. In adopting CAMAC as the hardware standard the DACC indicated that Branch Highway Systems adhering to the requirements of EUR 4600 were preferred but that single crate systems were permissible. The use of Serial Highway Systems was not ruled out but no decision on the use of such systems would be made until an ESONE report was issued.

Although the arguments in favour of the choice of CAMAC as a standard may also be used to justify the selection of a standard computer and language, such an arrangement is complicated by existing commitments of the associated laboratories. These complications may be minimised by the use of portable software or high level languages and some work along these lines has been reported by two of the larger laboratories within the Association.

1. the use of CLSD⁽¹⁾ at the Culham Laboratory, United Kingdom.
2. and the use of PL within CEA Laboratories in France.

The use of the former language implies the backing of a large central computer and is not acceptable to all the laboratories within the Association. The DACC has decided, therefore, that IML⁽²⁾ should be adopted within the Association. To assess the practical effects of such a decision, IML is being implemented within PL at Fontenay-aux-Roses, France and as part of CLSD at Culham. It is expected that IML macros will be produced to suit most of the small computers currently in use.

It has been agreed that DACC should co-ordinate its work closely with the current activities of the various ESONE Working Groups and a sub-committee has been set up under the Chairmanship of Mr. D. Zimmerman, IPP, Garching, F. R. Germany, to study the recommendations of the ESONE Analogue Signals Working Group.

* DACC Chairman (1974/75) is Dr. C. Gourdon, Fontenay-aux-Roses, France.

¹ A Portable Language for System Development. M. Calderbank, V.J. Calderbank. Software-Practice and Experience, Vol. 3 p. 309 (1973). LSD Manual CLM-PDN 9/71 V.J. Calderbank, M. Calderbank.

² Introduction to CAMAC IML. I. N. Hooton, P. J. Hagan, Harwell report, AERE R7578.

PAPER ABSTRACTS TRANSLATIONS

CAMAC Applied to the Evaluation and Development of Microprocessor Systems

D. L. Abbott and H. J. Ringel

Summary

CAMAC is used as a flexible interface to develop systems based on microprocessor integrated circuits. A computer and CAMAC provide a tool for evaluating the microprocessor while it is connected to real I/O hardware, debugging microprocessor software and, finally, loading programmable ROMs. The work is aimed at developing a programmable crate controller for the CAMAC Serial System.

Zusammenfassung

CAMAC wird als flexibles Interface für die Entwicklung von Systemen mit Mikroprozessor-Bausteinen eingesetzt. Die Verwendung von CAMAC mit einem Rechner erlaubt die Untersuchung einer Mikroprozessoreinheit, welche an normale Ein/Ausgangsgeräte angekoppelt ist, erlaubt das Austesten von Mikroprozessorprogrammen sowie auch das Laden von programmierbaren ROMs. Das Ziel der Arbeiten ist die Entwicklung einer programmierbaren Überrahmensteuereinheit für das serielle CAMAC-System.

Résumé

Le système CAMAC est utilisé, en raison de la souplesse de son interface, pour le développement de systèmes basés sur des circuits intégrés microprocesseurs. Un ordinateur associé à CAMAC constitue un instrument qui permet d'évaluer les caractéristiques du microprocesseur lorsque celui-ci est relié à du matériel Entrée/Sortie en temps réel, de mettre au point le logiciel du microprocesseur et, enfin, de charger des mémoires mortes programmables. Les travaux ont pour objectif de mettre au point un contrôleur de châssis programmable pour le système CAMAC série.

Riassunto

Il CAMAC è impiegato come interfaccia per lo sviluppo di sistemi basati su «microprocessor». Un calcolatore e il CAMAC forniscono un mezzo per valutare il «microprocessor» connesso a reali unità di ingresso-uscita, per correggere il software del microprocessore e infine caricare le memorie ROM programmabili. Lo scopo del lavoro è lo sviluppo di un modulo di controllo programmabile per il sistema CAMAC serie.

Samenvatting

CAMAC wordt gebruikt als een flexibele interface voor de ontwikkeling van systemen die gebaseerd zijn op geïntegreerde microprocessorschakelingen. Computer en CAMAC dienen als hulpmiddel bij de beoordeling van microprocessors, het opsporen van fouten in de microprocessor software en het programmeren van de ROMs. Het doel van deze werkzaamheden is de ontwikkeling van een programmeerbare crate controller voor het CAMAC Serial System.

Резюме

САМАС был применен в качестве удобного интерфейса для разработки системы, использующей интегрированный микропроцессор. ЭВМ и САМАС являются орудием для определения работы микропроцессора подключенного к аппаратуре для запуска программ и, для зарядки программированных ЯОМ-ов. Исследования имеют в виду разработку программированного контроллера крейта для последовательной системы САМАС.

A Multi-User Data Network for Communication Between Computers

H. Verelst

Summary

Independent computers are linked via a 500 kBaud transmission loop. Any computer can seize control and address a message to any other computer. The interface between each computer and its associated modem is a double-width CAMAC message processor module providing intermediate storage, code conversion and error checking.

Zusammenfassung

Voneinander unabhängige Rechner sind über eine 500 k Baud-Übertragungsschleife miteinander verbunden. Jeder Rechner kann die Steuerung übernehmen und eine Information an einen der anderen Rechner übertragen. Die Koppelheit zwischen Rechner und zugehörigem Modem besteht aus einer CAMAC-Einheit (Doppelmodul) zur Informationsverarbeitung welche eine Zwischenspeicherung von Daten Code-Umsetzung und Fehlerprüfungen erlaubt.

Résumé

Des ordinateurs autonomes sont interconnectés par une ligne de transmission à 500 kBauds, en boucle fermée. Chaque ordinateur peut assumer le contrôle et adresser un message à n'importe quel autre ordinateur. L'interface entre chaque ordinateur et le modem qui lui est associé est un module CAMAC double unité de traitement des messages, qui assure une mémorisation intermédiaire, une conversion de code et le contrôle des erreurs.

Riassunto

Calcolatori indipendenti vengono collegati mediante un circuito di trasmissione da 500 kBaud. Ogni calcolatore può prendere il controllo e indirizzare un messaggio a qualsiasi altro calcolatore. L'interfaccia fra ogni calcolatore e il relativo modem è un modulo CAMAC a doppia larghezza per il trattamento di messaggi dotato di memoria intermedia, conversione di codice e controllo di errori.

Samenvatting

Afzonderlijke computers worden via een 500 k-Baud transmission loop met elkaar verbonden. Iedere computer kan de besturing overnemen en een boodschap naar een andere computer zenden. De interface tussen computer en modem is een CAMAC-message processor modul dat o.a. zorg draagt voor tussentijdse buffering, fouten detectie en code conversie.

Резюме

Независимые ЭВМ соединены через петлю 500 К. бод-овой линии связи. Любая ЭВМ может принудить управление и передать данные к любой ЭВМ. Интерфейс между ЭВМ и связанным с ним модемом разработан в виде двухмодульного блока САМАС, который является процессором обеспечивающим промежуточное хранение данных, преобразование кодов и проверку.

Proposal for a CAMAC System Measuring Tridimensional Coordinates

I. Török

Summary

The use of CAMAC is recommended for measurements of volume coordinates and for positioning purposes. As an example, a possible measuring arrangement for the coordinates of a microscope is described briefly.

Zusammenfassung

Es wird der Einsatz von CAMAC für die Messung von Raumkoordinaten und für entsprechende Einstellvorrichtungen empfohlen. Als Beispiel wird eine Meßvorrichtung für ein Mikroskop kurz beschrieben.

Résumé

Le système CAMAC convient particulièrement bien à la mesure des coordonnées spatiales et au positionnement. Une brève description d'un ensemble de mesure des coordonnées d'un microscope est donnée à titre d'exemple.

Riassunto

Si raccomanda l'impiego del CAMAC per la misura delle coordinate di volume e per determinazioni di posizione. A titolo d'esempio si descrive brevemente il metodo per misurare le coordinate di un microscopio.

Samenvatting

Het gebruik van CAMAC wordt aanbevolen voor het meten van 3-dimensionale coördinaten. Als voorbeeld wordt een korte beschrijving gegeven van een mogelijke opstelling voor het meten van de x, y en z coördinaten van een microscoop.

Резюме

Рекомендуется применение CAMAC-а для измерений пространственных координат. В качестве примера рассмотрена возможная установка для измерения координат на микроскопе.

CAMAC in the Nuclear Physics Laboratory Oxford

B. E. F. Macefield

Summary

Nuclear physics research at the laboratory includes nuclear structure studies based on two Van de Graaff accelerators. For data acquisition from these experiments there is a CAMAC system with two branch highways, coupled through a system crate to two computers (PDP-10 and PDP-7). In addition there are serial data links to programmable stand-alone CAMAC systems.

Zusammenfassung

Zu den kernphysikalischen Forschungen des Laboratoriums gehören Untersuchungen der Atomstruktur, für die zwei Van-de-Graaff-Beschleuniger zur Verfügung stehen. Für die Datenerfassung werden zwei CAMAC Branch Systeme verwendet, welche über einen System-Überrahmen als Steuereinheit an zwei Rechner (PDP-10 und PDP-7) angeschlossen sind. Zusätzlich sind serielle Datenübertragungseinrichtungen für programmierbare "stand-alone" CAMAC-Systeme vorhanden.

Résumé

Les travaux de recherche de physique nucléaire exécutés au laboratoire comprennent des études de structure nucléaire utilisant deux accélérateurs Van de Graaff. L'acquisition des données fournies par ces expériences est réalisée à l'aide d'un système CAMAC équipé de deux Interconnexions de branche relié par l'intermédiaire d'un châssis système, à deux ordinateurs (PDP-10 et PDP-7). Le laboratoire dispose en outre de liaisons série qui transmettent les données des systèmes CAMAC autonomes et programmables.

Riassunto

Le ricerche di fisica nucleare svolte presso il laboratorio comprendono studi delle strutture nucleari mediante due acceleratori Van de Graaff. Per ottenere i dati nel corso degli esperimenti ci si serve di un sistema CAMAC con due rami principali, collegati a due calcolatori (PDP-10 e PDP-7) attraverso un contenitore di comando del sistema. Esistono inoltre collegamenti di dati seriali con sistemi programmabili CAMAC isolati.

Samenvatting

Tot het kernfysisch onderzoek van bovengenoemd laboratorium behoort ook de bestudering van kernstructuren met behulp van twee Van de Graaff versnellers. De data acquisitie van de beide experimenten is gerealiseerd met een CAMAC-systeem bestaande uit twee Branches. De twee branches zijn via een system crate aan twee computers (PDP-7 en PDP-10) gekoppeld. Daarnaast wordt nog gebruik gemaakt van serial data links en zelfstandige programmeerbare CAMAC-systemen (7025 controller).

Резюме

В лаборатории ведутся исследования ядерных структур с помощью двух ускорителей Van Graaff. Сбор данных из этих экспериментов выполняется в системе CAMAC с двумя ветвями сцепленными через «системный кейт» с двумя ЭВМ [PDP-10 и PDP-7]. Кроме того имеются линии последовательной связи с программированными самостоятельными системами CAMAC.

CAMAC Modules for Physics Experiments V. A. Arefiev et al.

Summary

A system of CAMAC modules has been developed to provide on-line data acquisition and processing. Modules are sub-divided into classes according to applications, and their technical characteristics are given. A number of various system configurations is shown.

Zusammenfassung

Es wurden CAMAC-Einheiten für ein System zur Echtzeit-Datenerfassung und -verarbeitung entwickelt. Die Anwendungsbereiche und technischen Merkmale der Einheiten sowie eine Reihe verschiedener Systemkonfigurationen werden beschrieben.

Résumé

Un système de modules CAMAC a été mis au point pour l'acquisition et le traitement des données en ligne. Les modules sont subdivisés en deux classes, suivant leur application. Leurs caractéristiques techniques sont indiquées. Différentes configurations du système sont décrites.

Riassunto

È stato sviluppato un sistema di moduli CAMAC per l'acquisizione ed il trattamento di dati in linea. I moduli sono suddivisi in classi a seconda delle applicazioni e ne sono indicate le caratteristiche tecniche. Vengono illustrate varie configurazioni del sistema.

Samenvatting

Een systeem van CAMAC-modules werd ontwikkeld voor de on-line gegevensverwerking en -verwerking. De betrokken modulen worden in klassen onderverdeeld volgens de toepassing en hun technische karakteristieken worden aangegeven. Verder wordt aandacht geschonken aan een aantal verschillende systeem configuraties.

Резюме

Разработан набор блоков CAMAC для сбора и обработки данных. Представлена классификация и главные технические характеристики блоков. Показаны системы с разными конфигурациями.

A Branch Highway Driver for the CII-C90-40 Computer

J. C. Faivre, C. Legrele and J. C. Lugol

Summary

A Branch Highway driver for the CII-C90-40 computer is described. It is designed to control up to seven crates, and to transfer data by the programmed input/output channel of the computer.

Zusammenfassung

Es wird eine Branch-System-Kopplung für den CII-C90-40-Rechner beschrieben, an welche bis zu sieben Überrahmeneinheiten angeschlossen werden können. Daten werden unter Programm Kontrolle über den Eingabe-/Ausgabekanal des Rechners übertragen.

Résumé

Description d'une commande d'Interconnexion de branche pour l'ordinateur CII-C90-40. Elle est conçue pour commander jusqu'à 7 châssis et transférer des données par le canal entrée/sortie programmé du calculateur.

Riassunto

Si descrive un elemento di comando del ramo principale CAMAC per il calcolatore CII-C90-40 progettato per controllare fino a sette contenitori e per trasferire dati mediante il canale programmato I/O del calcolatore.

Samenvatting

Er wordt een beschrijving gegeven van een branch-highway-driver voor de computer CII-C90-40. Deze is ontworpen voor het besturen van ten hoogste zeven rekken en voor het overbrengen van gegevens via het geprogrammeerde input-output-kanaal van de computer.

Резюме

Описан драйвер ветви для ЭВМ CII-C90-40, предназначенный для управления до 7 крейтов и передачи данных через программный канал ввода-вывода ЭВМ.

'Shift'—A Serial Highway Interface for Teletypes

D. L. Abbott

Summary

A simple adaptor using standard MOS-LSI chips permits a conventional teletype port on a computer to act as a driver for the CAMAC Serial Highway. The adaptor performs the functions of delimiter byte insertion and deletion, clock generation, parity generation and checking, and level shifting.

Zusammenfassung

Ein einfacher mit Standard-MOS-LSI Bausteinen ausgerüsteter Adapter erlaubt die Verwendung von konventionellen Fernschreiber Koppereinheiten für Rechner um den Anschluss von seriellen CAMAC Übertragungssystemen zu ermöglichen. Der Adapter sorgt für die Einfügung und Löschung von Delimiter Bytes, für die Taktgenerierung, für die Paritätserzeugung und -kontrolle sowie für die Anpassung von Signal Niveaus.

Résumé

Un simple adaptateur utilisant des circuits MOS-LSI normalisés permet à un coupleur télétype classique, placé sur un ordinateur, de faire fonction de commande d'«Interconnexion de branche CAMAC Série». Le dispositif d'adaptation réalise les fonctions d'insertion et de suppression du byte «Fin de Messages CAMAC», émission des signaux d'horloge, génération et contrôle de parité, ainsi que transposition de niveaux.

Riassunto

Un semplice adattatore a circuiti integrati MOS-LSI permette ad un convenzionale terminale per telescrivente di un calcolatore di fungere da elemento di comando del collegamento seriale CAMAC. L'adattatore ha funzioni di introduzione e di cancellazione del byte di delimitazione, di generazione del segnale di temporizzazione, di generazione e controllo della parità e di spostamento del livello.

Samenvatting

Een eenvoudige adaptor, uitgevoerd met standaard MOS-LSI schakelingen, maakt het mogelijk gebruik te maken van een normale teletype interface als driver voor de CAMAC serial highway. De adaptor verzorgt het invoeren en verwijderen van de delimiter bytes, het genereren van de kloksignalen, het genereren en controleren van het pariteits bit en het aanpassen van de signaal niveaus aan in- en uitgang.

Резюме

Простой адаптор применяющий стандартные схемы высокой степени интеграции позволяет использовать обычный интерфейс телетайпа как драйвер последовательной ветви САМАС. Адаптор выполняет следующие функции: добавляет или выбрасывает байт делimiters, генерирует тактовые импульсы, проверяет и генерирует биты четности и сдвигает уровни сигналов.

A CAMAC Multicrate System On-line to an HP2116B Computer

E. V. Chernykh, I. F. Kolpakov, N. M. Nikityuk, V. A. Smirnov

Summary

A CAMAC four crate system is described. Each crate uses a specialized controller for an HP2116B computer. The computer and the crate controller are coupled by a special branch driver. The interconnecting cable length of the system with the computer is not more than 4 m. The maximum rate of information exchange is 312 500 of 16-bit words a second.

Zusammenfassung

Es wird ein CAMAC-System mit vier Übertrahmeneinheiten beschrieben. Jeder Übertrahmen ist mit einer besonderen für die Anwendung des Rechners HP2116B geeigneten Rahmensteuereinheit ausgerüstet. Diese werden über einen speziellen Branch-Treiber an den Rechner angeschlossen. Das Verbindungskabel zwischen System und Rechner ist höchstens 4 m lang. Die maximale Rate für den Informationsaustausch beträgt 312 500 16-Bit-Worte je Sekunde.

Résumé

Description d'un système CAMAC à quatre châssis. Chaque châssis utilise un contrôleur spécialisé pour ordinateur HP2116B. L'ordinateur et le contrôleur de châssis sont couplés à l'aide d'une commande de branche spéciale. La longueur du câble utilisé pour relier le système à l'ordinateur ne dépasse pas 4 m. Le débit maximal des échanges d'informations est de 312 500 mots de 16 bits par seconde.

Riassunto

Si descrive un sistema CAMAC a quattro contenitori. Ciascun contenitore usa un modulo di controllo specializzato per un calcolatore HP2116B. Il calcolatore e il modulo di controllo sono collegati da uno speciale elemento di comando del ramo. La lunghezza del cavo che collega il sistema con il calcolatore non supera i 4 m. La massima cadenza di trasferimento per le informazioni è di 312 500 parole da 16 bit al secondo.

Samenvatting

Er wordt een beschrijving gegeven van een CAMAC systeem met vier rekken. Voor de koppeling van de CAMAC rekken met een HP 2116 B computer wordt gebruik gemaakt van een speciale branchdriver-crate controller combinatie. De lengte van de kabelverbinding tussen het systeem en de computer bedraagt niet meer dan vier meter. De maximale transfersnelheid bedraagt 312 500 16-bits woorden per seconde.

Резюме

Описана четырех-крейтовая система САМАС. Контроллеры крейтов и ветви специфические для ЭВМ HP2116B. Длина кабеля интерфейса ограничена до 4 м. Максимальная скорость передачи данных достигает 312 500 16 битовых слов в секунду.

Dedicated CAMAC Crate Controller with Autonomous Data Collection

F. Hübler, A. Krolzig and R. Pforte

Summary

This dedicated CAMAC crate controller suits the special requirements of many high energy nuclear physics experiments. It allows data collection from sources with arbitrary block lengths, and from a fixed array of sources. Several features minimise the load on the computer.

Zusammenfassung

Die beschriebene spezielle Steuereinheit für einen CAMAC-Übertrahmen wird den besonderen Erfordernissen für viele Experimente in der Hochenergiephysik gerecht. Sie ermöglicht die Erfassung von Daten mit unbestimmter Blocklänge und aus Datenquellen mit vorgegebener Konfiguration. Durch die Auslegung der Einheit wird eine minimale Belastung des Rechners gewährleistet.

Résumé

Ce contrôleur de châssis CAMAC spécialisé convient aux exigences spéciales d'un grand nombre d'expériences de physique nucléaire à haute énergie. Il permet l'acquisition de données en provenance soit de sources émettant un bloc de données de longueur variable, soit d'un ensemble de sources bien déterminé. Différents dispositifs permettent de réduire la charge de l'ordinateur.

Riassunto

Questo modulo di controllo CAMAC «dedicato» soddisfa alle particolari esigenze di molti esperimenti di fisica nucleare ad alta energia. Esso permette di raccogliere dati da varie fonti con blocchi di lunghezza arbitraria e da una schiera fissa di sorgenti. Vari dispositivi riducono al minimo il carico del calcolatore.

Samenvatting

Deze crate controller voldoet aan de speciale eisen van veel experimenten op het gebied van de hoge energie kernfysica. Een aantal ingebouwde features, zoals bloktransporten, adres scan, enz. beperken de computerbelasting tot een minimum.

Резюме

Контроллер крейта специального назначения выполняет особые требования многих экспериментов ядерной физики высокой энергии. Он обеспечивает сбор данных из источников при любой длине блока или из фиксированного набора источников. Некоторые приспособления облегчают работу ЭВМ.

CAMAC Multi-Branch System for Control Data 3100 Computers

W. Karbstein and B. Kögel

Summary

A CAMAC interface for the CDC 3100, handling up to eight CAMAC branches, is used in conjunction with a system controller that provides extensive LAM-handling and modes of operation. The system will be used to control the Karlsruhe Isochronous Cyclotron, and is programmed partly in CAMAC IML and partly in CDC Assembler.

Zusammenfassung

Eine CAMAC-Koppeleinheit für den Rechner CDC-3100, an welche bis zu 8 CAMAC-Branch-Systeme angeschlossen werden können, wird in Verbindung mit einer Systemsteuerung verwendet, die eine umfassende Verarbeitung von Anforderungen und zahlreiche Betriebsarten ermöglicht. Das System wird zur Steuerung des Karlsruher Isochron-Zyklotrons verwendet werden. Für die Programmierung wird einmal CAMAC IML und ausserdem die CDC-Assembler-Sprache angewendet.

Résumé

Une interface CAMAC destinée au CDC 3100, susceptible de traiter jusqu'à huit branches CAMAC, est utilisée en liaison avec un contrôleur de système qui permet un traitement des LAM puissant et divers modes d'exploitation. Le système sera utilisé pour le contrôle-commande du cyclotron isochrone de Karlsruhe; il a été programmé en partie en CAMAC IML et en partie en Assembleur CDC.

Riassunto

Un'interfaccia CAMAC per il CDC 3100, collegabile a otto rami CAMAC, è impiegata con un'unità di controllo del sistema, che fornisce vaste possibilità di trattamento dei richiami e modi di operazione. Il sistema verrà impiegato per controllare il ciclotrone isocrono di Karlsruhe ed è programmato in parte in CAMAC IML e parte in Assembler CDC.

Samenvatting

Een CAMAC interface, geschikt voor maximaal 8 CAMAC branches, wordt via een system controller gekoppeld aan een CDC 3100 computer. De system controller kent verschillende operation modes en heeft een uitgebreide interrupt verwerking. Het systeem zal worden aangewend voor de regeling van het isochroon cyclotron te Karlsruhe en is ten dele geprogrammeerd in CAMAC IML en ten dele in CDC assembler.

Резюме

Интерфейс САМАС для ЭВМ CDC 3100, обслуживающий до восьми ветвей САМАС, применен вместе с контроллером системы который обеспечивает широкую обработку запросов и многие режимы операции. Система будет применена для управления изохронным циклотроном в Karlsruhe. Програмное обеспечение на языке САМАС-IML или в ассемблере CDC.

Translating CAMAC Test Programs from Interpretive to Assembled Basic

B. Becks and H. Halling

Summary

Test programs for CAMAC modules and systems can be written and changed easily by using interpretive BASIC. A major disadvantage is the slow execution speed. A compiler has therefore been written for the PDP-11 to translate tested BASIC programs into macro-assembler programs.

Zusammenfassung

Testprogramme für CAMAC-Einheiten und -Systeme können unter Verwendung der interpretativen Sprache, BASIC leicht erstellt und geändert werden. Der Hauptnachteil ist die geringe Verarbeitungsgeschwindigkeit. Es wurde deshalb ein Compiler für die PDP-11 geschrieben, der ausgetestete BASIC Programme in Makro-Assembler Programme übersetzt.

Résumé

Des programmes de contrôle des modules et systèmes CAMAC peuvent être écrits et changés sans difficulté en utilisant le langage interpréteur BASIC qui présente néanmoins un grave inconvénient : la lenteur de l'exécution. C'est pourquoi un compilateur a été écrit sur PDP-11, en vue de traduire, après leur mise au point, les programmes BASIC, en programmes macro-assembleurs.

Riassunto

I programmi di prova per moduli e sistemi CAMAC possono essere facilmente scritti e modificati servendosi del BASIC interpretativo. Un notevole svantaggio è la bassa velocità d'esecuzione, per cui è stato scritto un programma compilatore per permettere al PDP-11 di tradurre programmi BASIC sperimentati in programmi macroassemblatore.

Samenvatting

Testprogramma's voor CAMAC modulen en systemen kunnen gemakkelijk worden geschreven en gewijzigd door gebruik te maken van BASIC. Een groot nadeel vormt de traagheid van de uitvoering. Dit is de reden waarom een compilatieprogramma werd uitgewerkt voor de PDP-11 voor het omzetten van geteste BASIC-programma's in macro-assembler programma's.

Резюме

Тестовые программы для блоков и систем САМАС можно просто писать и исправлять используя интерпретативный Базик. Недостатком является малая быстрота выполнения. По этому написана на ЭВМ PDP-11 программа перевода уже проверенных программ с языка Базик на программы использующие макро-ассемблер.

Implementation of CAMAC Intermediate Language (IML) in an Assembler Language Environment

W. Kneis

Summary

This paper describes the implementation of a subset of an early version of CAMAC Intermediate Language (IML) in the host language environment of the COMPASS assembler for the CDC 3100.

Zusammenfassung

Es wird die Einfügung eines Teils einer früheren Version von CAMAC-IML in die COMPASS-Assembler Sprache des Rechners CDC 3100 als übergeordnete Sprache beschrieben.

Résumé

Le présent article décrit la réalisation d'un sous-ensemble d'une première version du « CAMAC Intermediate Language (IML) » dans le cadre du langage hôte de l'assembleur COMPASS, conçu pour le CDC 3100.

Riassunto

Si descrive la realizzazione di un sottoinsieme di una prima versione del Linguaggio intermedio CAMAC (IML) nell'ambito del linguaggio ospite dell'assembleur COMPASS per il CDC 3100.

Samenvatting

Dit artikel beschrijft de implementatie van een vroegere versie van CAMAC Intermediate Language (IML) in de COMPASS assembler van de CDC 3100.

Резюме

Описана частичная имплементация предварительной версии языка IML-САМАС употребляемого совместно с языком COMPASS для ЭВМ CDC-3100.

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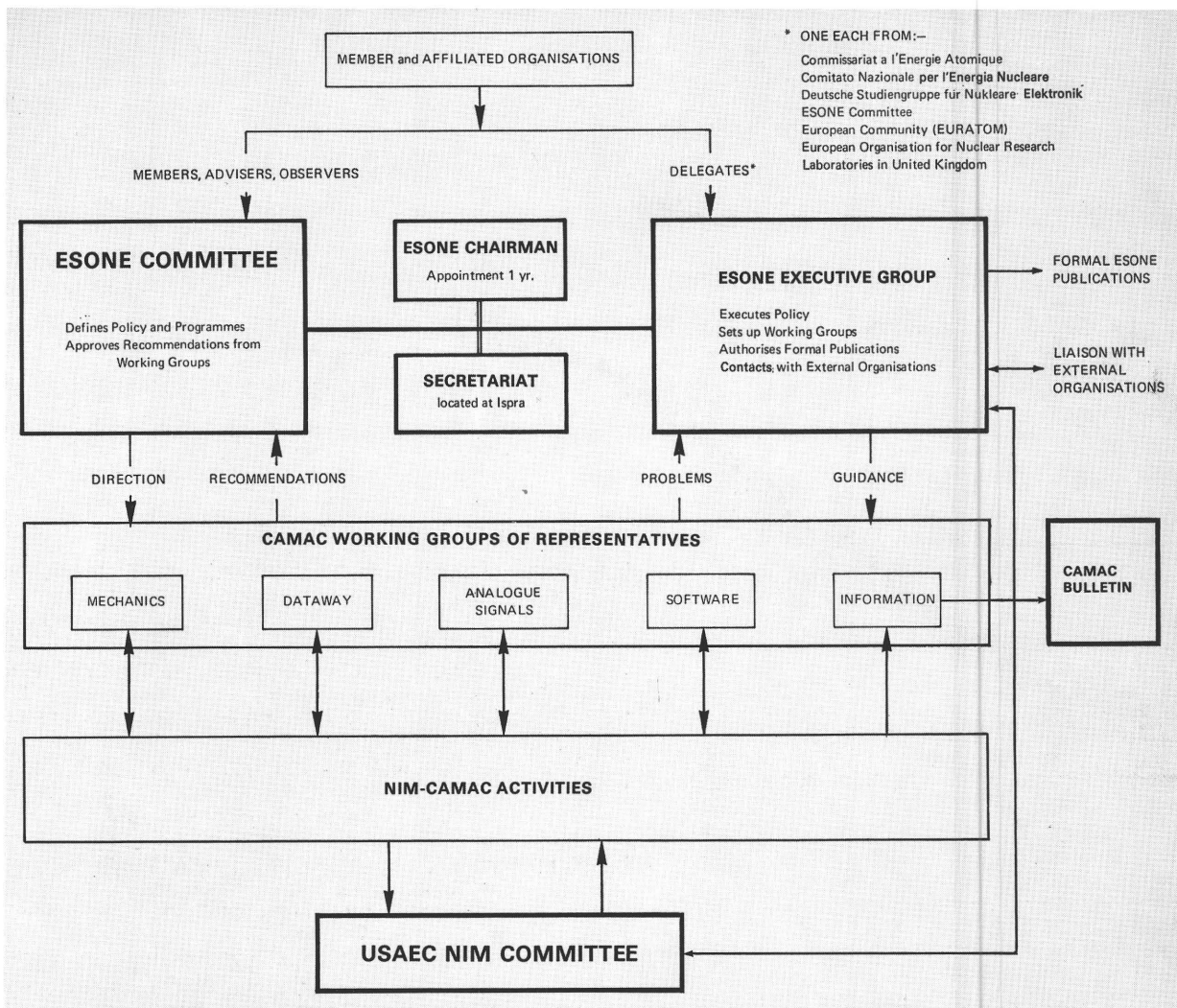
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