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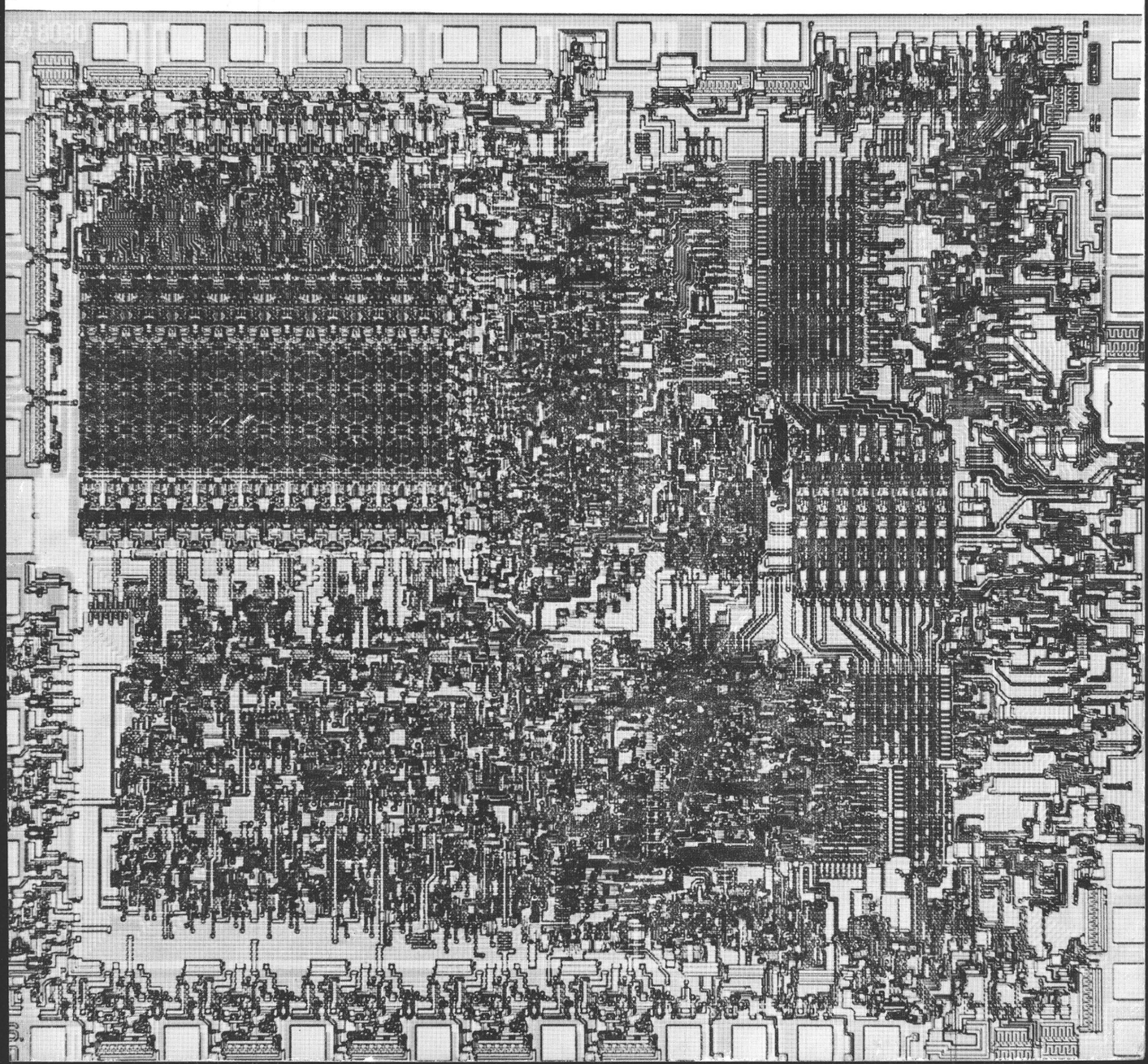

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On the cover: Enlarged view of the microprocessor chip, Intel 8080 (original size: 2 × 2 mm), of Intel Corporation.

CAMAC

bulletin

Editorial Working Group :

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P. Christensen
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Production Editor:

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Correspondence to:

the Secretary of the
ESONE Committee
New provisional address:
H. Meyer, CBNM EURATOM
B-2440 Geel, Belgium

Distributed by:

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CONTENTS OF ISSUE No. 14

NEWS

CAMAC SYMPOSIUM IN BRUSSELS

The Second International Symposium on CAMAC in Computer Applications was held in the Manhattan Center in Brussels from October 14-16th, 1975. The Symposium was jointly organized by the ESONE-Committee and the European CAMAC Association, and sponsored by the Commission of the European Communities.

536 participants from 25 countries registered and 77 papers were presented.

The main topics of the Symposium were concerned with the Application of CAMAC in Industrial Process Control, Laboratory Automation, Medicine and Health Services, Data and Computer Communications, Public Utilities, and Environmental Control.

The mornings were devoted to survey talks in plenary sessions, while parallel sessions were run in the afternoons. The afternoon sessions were aimed primarily at exchange of experience between users of CAMAC in the fields surveyed in the mornings.

The welcome address was given by Director General R.K. Appleyard of CEC, who expressed his belief that CAMAC will now be much more able to become independent than in 1973 at the time of the first Symposium. Among the opening speakers, Director Chr. Layton of CEC outlined the ideas for promotion of automation and data processing in Europe by CEC. In spite of some disappointments, the Commission still finds it extremely important to catalyze such activities on a European level (e.g. support to the development of a long term procedural language) and welcomed a collaboration with people engaged in CAMAC activities.

Three status talks by H. Bisby from Harwell, R. Trechcinski from Warsaw, and D. Horelick from Stanford Linear Accelerator described the worldwide status of CAMAC. These talks revealed a widespread use of CAMAC in many fields, although the nuclear field is still dominating. The pragmatic way of handling complex technical problems in the USA (e.g., the use of the serial highway in large industrial systems) once again was shown to be very successful.

From the CAMAC developments session, special attention was drawn to descriptions of systems with distributed intelligence and to extensions of BASIC for CAMAC. The proper use of microcomputers was widely discussed.

Survey speeches of CAMAC applications in Industrial Process Control, Laboratory Automation, and Medicine and Health Services were given by E.G. Kingham, CERL; R. Patzelt, Technical University Vienna, and H. Pangritz, HMI Berlin. 58 industrial applications of CAMAC are known in 12 different areas. In the industrial use of CAMAC, future interest is in the development of functional modules, and in defining practises for making connections to the processes. Similarly, CAMAC's entry into the area of medicine will occur via companies able to deliver complete systems.

The applications of CAMAC in Data and Computer Communications, Public Utilities, and in Environmental Control were reviewed by D. Reimer from Dornier; H. Lukacs from KFKI, Budapest and J. Landbrecht from the Landesamt für Umweltschutz, München, respectively.

Data Communications is a field in rapid growth, and the CAMAC serial highway offers a good answer to this challenge. Much work is being done for instance in Daresbury Laboratory for such type of applications. Environmental Control implies a good deal of data communications also, and the Bavarian system is a convincing example of the use of CAMAC in this field. The problem in using CAMAC in Public Utilities seem to be similar to those met in industrial environments.

There was a great interest in all sessions, and valuable discussions took place.

The Symposium was supported by a sizable exhibition. 31 Companies showed a vast display of CAMAC components, modules and complete systems. New trends were clearly indicated, such as the use of microcomputers, the CAMAC serial highway and also colour display systems. The directly controlled machine tools shown by RWTH Aachen and KFA Jülich were very impressive.

The Proceedings of the Symposium will be published by the Commission of the European Communities and are expected to be available in early 1976.

PROCEEDINGS OF THE SECOND CAMAC SYMPOSIUM

The Proceedings of the 2nd CAMAC Symposium are in preparation and will be published in early 1976 by the Commission of the European Communities. Registered participants of the Symposium will receive their copy of the proceedings free of charge.

Further copies can be purchased by everybody. Requests should be sent to the following address:

Commission of the European Communities
29 rue Aldringen
Luxembourg

MICROPROCESSORS FOR CAMAC

1

EDITORIAL: MICROPROCESSORS AND CAMAC

by
RCM Barnes
AERE, Harwell, England

A microprocessor performs the control and data-processing operations needed to execute a user's program, and is equivalent to the central processing unit (cpu) of a minicomputer. As a result of using large-scale integration (LSI) technology this complex device equivalent to many thousands of transistors occupies only one or two integrated-circuit packages. It is used in conjunction with LSI memory components, typically read-only memories for fixed programs and microprograms, and random-access memories for the user's programs and data. A paper by Stuckenberg in this issue of CAMAC Bulletin gives background information on microprocessors.

The typical CAMAC system is often described in terms of slave crate controllers, which transfer data between the Dataway and an external computer in response to commands generated by the computer. However, there are many systems where the CAMAC equipment is able to generate commands and process data. Some of these systems rely entirely on internal command-generation and data processing, and are used, without an associated external computer, as 'stand-alone' CAMAC systems. Others are used in conjunction with a computer, but have additional distributed processing capability at various points in the system.

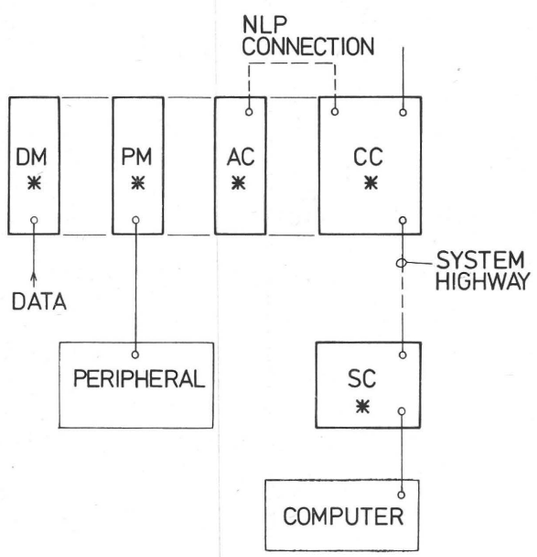

Fig. 1 Possible locations for microprocessors in CAMAC

SC = System Controller (Serial Driver, Branch Driver)
CC = Crate Controller
AC = Auxiliary Controller
PM = Module controlling a complex peripheral
DM = Data-reduction module

Processing and control capability within CAMAC has been provided in the past by plug-in units based on SSI/MSI components, for example those described by Ward[1] and Starzynski[2]. The microprocessors and memories that are now available as LSI components have opened the way to much cheaper and more powerful processing within CAMAC. Equipment incorporating microprocessors has been announced by several firms, and there is widespread interest in the possibilities (and problems) of CAMAC systems with distributed processing.

The first applications of microprocessors in CAMAC have been mainly in crate controllers, which occupy the control station and one or more normal stations. Such crate controllers may be intended for use in stand-alone CAMAC systems, without a separate computer, or may have ports for the Branch Highway or Serial Highway. For example, the papers in this issue by Gallice and Mathis and by Schöberl describe crate controllers for stand-alone systems, based on the Intel 8080 microprocessor. A Serial Crate Controller incorporating an Intel 8080 microprocessor is mentioned in a news item from Müller and Halling in this issue and has been described elsewhere by Halling[3]. The paper by Lecoq, Tedjini, Wendel and Metzger in CAMAC Bulletin No. 13 described a system using a crate controller based on the Intel 8080 microprocessor.

An alternative method of providing processing power within a CAMAC crate is to have a microprocessor in an auxiliary controller which occupies one or more normal stations. This has the advantage that additional processing power can be added to a system as a plug-in option, but there are difficulties because the auxiliary controller does not have direct access to the Dataway N and L lines, and competes with the crate controller for the use of the Dataway. The papers in this issue by Abbot and Barsotti describe CAMAC units, based on the Intel 8080 and Motorola 6800 microprocessors, that can be used either as crate controllers (in stand-alone systems) or as auxiliary controllers (for example, in Serial Highway or Branch Highway systems). The ESONE and NIM Committees are studying the possibility of a standardised connection between auxiliary controllers and the crate controller.

Yet another possibility for microprocessors in CAMAC is as part of the system controller, either to provide autonomous processing and control, or to carry out routine tasks such as the detailed message protocol for the Serial Highway. Finally, there are applications for microprocessors in CAMAC modules that control complex peripherals or pre-process data before it reaches the Dataway.

Such modules do not need to generate commands on the Dataway. A paper by Kollbach and Schmidt in this issue describes a CAMAC unit, including a Motorola 6800 microprocessor, which can be used as a data processing module or as an auxiliary controller.

A microprocessor-based CAMAC controller has advantages, compared with a separate computer, because it is housed in the CAMAC crate and is directly interfaced to the Dataway. The advantages of a 24-bit processor interfaced to the Dataway have been stressed by Cohn[4]. The microprocessor has fewer components and interconnections than the equivalent within-CAMAC processor based on 'random logic' SSI and therefore has potentially better reliability and lower assembly costs.

Because the high development costs of the LSI components are spread over a relatively large production, the microprocessor offers an advanced design of cpu at a reasonable cost.

One of the attractions of distributed processing (in either crate controllers or auxiliary controllers) is that it can significantly reduce the data traffic between the central computer and outlying parts of the system. This is particularly relevant to systems using the Serial Highway. For example, a microprocessor can substantially improve the data handling capability by performing data reduction, data filtering, and error control within the CAMAC crate, thus avoiding the overheads of transfers to and from the central computer. Another feature of such systems is that the distributed processing power can give greater security against total failure of the system.

At present, it is not possible to realise the full potential of microprocessors in CAMAC because the most readily available microprocessors are relatively slow, have short word-lengths that lead to clumsy handling of CAMAC 24-bit words, and have less generous software support than minicomputers. However, it would be unwise to ignore microprocessors on account of their present status. They are a young and vigorous section of the semiconductor and data processing scene, and it is reasonable to expect improvements in performance, falling costs, and more comprehensive software support. The paper by Bals, Caprini and Goran in this issue describes a crate controller in which there is a 24-bit processor, constructed from SSI and MSI components, because this is faster than currently available microprocessors.

Undoubtedly, many CAMAC controllers incorporating microprocessors will be used in individual systems, where the system-user tends to do the initial programming and the system is in a process of gradual development throughout its life. But microprocessors appear particularly attractive for small dedicated CAMAC systems, where the user is not expected to change the program, and also for subsystems within a larger systemwhich provides adequate facilities for program development in its central computer.

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2. Starzynski, A., A Modular Microcomputer in the CAMAC System. *CAMAC Bulletin*, No. 9, March 1974, p. 17.
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NEWS

"CAMAC BIBLIOGRAPHY" AND "CAMAC FOR NEWCOMERS"

These two supplements to CAMAC Bulletin no 13 were sent to all subscribers. Both papers were prepared by H.J. Stuckenberg of DESY, Hamburg, and additional copies are available from:

Sales Office for Official Publications of the Commission of the European Communities
Case Postale 1003
Luxembourg 1

The price including postage is:
BF 100 for Supplement A — "For Newcomers Only"
BF 50 for Supplement B — "Bibliography"
or an equivalent amount in any other currency.

A version in German of CAMAC for Newcomers is also available, and can be obtained from:

Zentralstelle für Atomkernenergie — Dokumentation ZAED
D-7514 Eggenstein-Leopoldshafen
Kernforschungszentrum

SERIAL CRATE CONTROLLERS

Christian Rovsing A/S, Copenhagen and Kinetic Systems International SA, Geneva have both a purchase order from CERN for the delivery of 52 serial crate controllers conforming to the latest ESONE/NIM recommendations (ESONE/SH/01, ESONE/SH/04).

Prototypes are to be delivered by October 1975.

2

MICROPROCESSORS

by

H. J. Stuckenberg

Deutsches Elektronen-Synchrotron DESY, Hamburg, F.R. Germany

Received 4th August 1975

SUMMARY Microprocessors are interesting alternatives to hard-wired logic for many control-oriented functions. This paper describes microprocessors and their related hardware and software problems.

INTRODUCTION

Microcomputers are general-purpose digital computers on a silicon chip. They have evolved from calculator chips because the semiconductor industry is able to put more and more logic on a chip. Today microcomputers are convenient 4 to 16-bit computers with a powerful instruction set, wide-range memory addressing, and interfacing facilities.

They are engaging the attention of equipment designers and manufacturers from a wide variety of industries. Before the invention of microcomputers designers had only the choice between 'random logic' (hardwired logic elements) and minicomputers, but now they have the ability to change the design or add new features to it merely by changing the program in an erasable and reprogrammable ROM. And by replacing many SSI and MSI logic packages with a few LSI chips they are saving money.

The main applications of microcomputers are:
— replacing random logic by freely programmable logic;
— autonomous 'intelligent' terminals.

Microcomputers consist of micro processors, ROM s and RAM s, and I/O-ports. We will discuss here only some properties of the micro processors.

Microprocessors are LSI circuits containing the arithmetic logic unit (ALU), accumulators, general-purpose registers, instruction decoder, program counter, timing, and connections to the I/O-bus.

THE HARDWARE

A basic processor, shown in Fig. 1, has three functional sections. The first one is the register-arithmetic-logic unit, or RALU, executing logic and arithmetic functions on data.

The control section contains a memory which provides the RALU with instructions for executing the different operations. The RALU sends back signals indicating the result of the previous or current operation so that the memory can modify its instruction sequence when appropriate.

The memory also opens or closes the gates of the interface logic, which is the third section of the processor connecting the system inputs and outputs.

The RALU replaces counters, shift registers and latches used in random logic, the control memory replaces gates, flip-flops, decoders and multiplexers.

The architecture of the various microprocessors is quite different, so that the user must notice the most significant characteristics.

Some very important characteristics are the addressing modes, the word-length of the internal bus and the interrupt structure. The actual number of instructions is not so important because of their different value. It is more realistic to compare the excecution time of a typical program together with the number of used external memory bits for different processors.

The more addressing modes and the more internal registers that are present in the processor, the less external memory capacity is likely to be required.

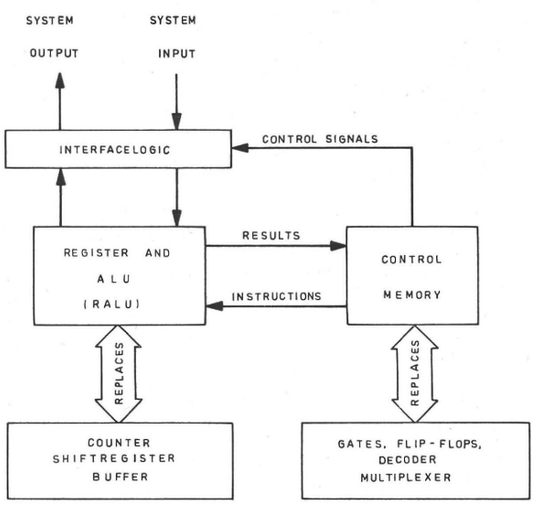


Fig. 1 The Basic Processor Blocks replace many Elements of Hardwired Logic.

Typical addressing modes used in microprocessors are:
— direct addressing, either via a memory location or internal register;
— immediate addressing, in which the processor executes the instruction on the operand code itself;
— indirect or pointer addressing which are similar, except that in the latter the address pointer is in an internal register instead of in a memory location;
— indexed addressing, in which the address contained in the instruction is added to the content of an index register; this result is then used to address the memory.

The word-length is normally fixed with the processor, but it may be variable if the design allows multiple processor chips in parallel. A variable data word is to be preferred when the needs of a variety of applications must be satisfied. For instance, a 16-bit processor chip can be programmed into 4-bit words for BCD display control, 8-bit words for CRT terminals, 12-bit words for handling the output of a-d converters, 16-bit words for general purpose computing and 24 to 32-bit words for high-accuracy applications.

If the microprocessor can handle interrupts, it can perform more than one task at a time. Today's possibilities range from simple reset of all registers to maskable multilevel interrupts with priority selection.

The first generation of microprocessors, made by a p-MOS process, is characterized by a small word-length (4-8 bit), slower speed (instruction execution time 5-40 µs) and a set of 40-50 instructions. Addition time per digit is of the order of 100 µs, programs computing exponential or angular functions may take 500 ms. Typical processors of this generation are the Intel 4004, Rockwell PPS, Intel 8008, National IMP-8/16.

INTEL 8080, a Typical Microprocessor in 1975

The second generation, made by the n-MOS process, has higher speed (instruction execution time 2-5 µs), a word-length of 8 bits and a set of about 80 instructions which are very powerful, together with an improved architecture. They are processors like the Motorola 6800 and the Intel 8080, which we will discuss in some detail because it is a frequently-used microprocessor. Fig. 2 shows the block diagram of the 8080.

The 8080 contains six 8-bit general purpose registers and an accumulator. The general purpose registers may be addressed individually or in pairs, for 1 or 2-Byte operations. The arithmetic and logic instructions set or clear four status flip-flops, a fifth flip-flop indicates a decimal arithmetic operation.

This processor has no build-in LIFO stack to save and restore the contents of the accumulator, program counter, status flip-flops and of the six general purpose registers, when interrupts occur. But the 8080 has a 16-bit stack pointer to address any portion of the memory. This external stack feature is useful for handling multilevel interrupts and for very large scale subroutine nesting.

The architecture of the 8080 is clear and transparent. There are 16 lines to address directly up to 64k Bytes of memory, or 256 input and 256 output ports. A sep rate 8-line bus is used for the bidirectional data transfer.

The general purpose register pairs B-C, D-E and H-L can be addressed by the register-select feature; they can be incremented and decremented with 16 bits in parallel, allowing easy manipulation of addresses and of the memory stack. The temporary register pair W-Z can be used as a program counter to hold a direct address to load or store the register pair H-L of the accumulator very rapidly. There is also the ability to do double precision additions between any register pair and the pair H-L, and fast parallel transfers from the pair H-L to the program counter or stack pointer.

The ALU section can execute decimal, binary and double precision arithmetic at about equal speed.

The 8080 has 78 instructions, which are very useful and extend the range of applicability of the processor. The instruction functions are as follows:

— data register and memory transfers;
— conditional or unconditional branches and subroutine calls;
— direct load or store accumulator;
— save and restore machine status;
— double length operations in data registers;
— stack pointer modification;
— logic operations;
— binary or decimal arithmetic;
— set and reset the interrupt-enable flip-flop;

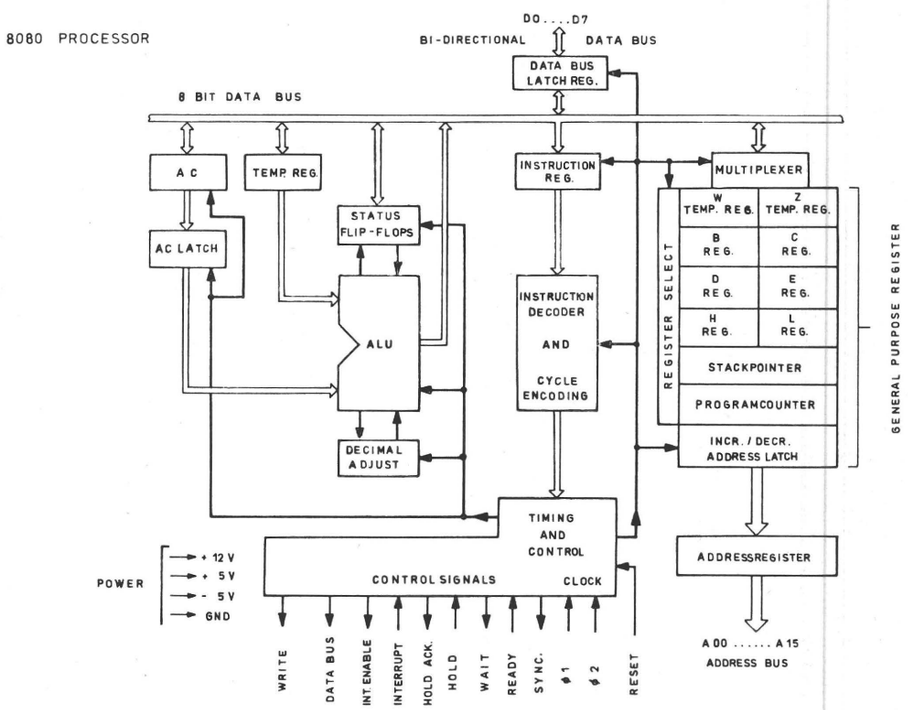


Fig. 2 The Internal Structure of the Intel 8080.

— increment or decrement the memory or data registers.

The instruction execution times range from 2μs, depending on the number of Bytes

Signals to control the interface to the memory and I/O-ports are provided directly by the 8080. All busses, including control, are TTL compatible.

BIPOLAR PROCESSORS

The processors we have mentioned so far are MOS types with clock frequencies up to 2MHz. For higher speeds two manufacturers are offering bipolar micro-processors, the Texas Instruments SBP 0400 and the Intel 3002/3001. Because of the relatively high power dissipation they are only 4 or 2-bit slices, but they can be connected in parallel. The clock can be as high as 10MHz. Motorola has announced the introduction in 1976 of a 4-bit slice processor with instruction execution in 55ns. All the bipolar processors mentioned are micro-programmable.

THE SOFTWARE

A program for use on microprocessors can be developed in different ways. Various time-sharing services are offering proprietary programs supplied by the micro-processor vendors, programs that allow the assembly of source programs into object code suitable for execution in a microprocessor. In developing a micro-processor program the first step is usually to establish the logical sequence of events in the form of a flow chart, and to convert each operation into one or more microprocessor instructions written in an assembly language. The sequence of instructions is then compiled in the time sharing computer into an object file in a suitable format for storage. The object file can be sent to a vendor to produce a usable ROM, but this procedure is very time-consuming and expensive, and nothing can be done to correct errors.

Time-sharing services also offer a simulation program that can execute the object program on a host computer in a manner similar to the actual micro-processor. The simulation program can stop operation at various places in the program. These features, combined with on-line editing programs, allow rapid modification or correction of the source program. This procedure seems to be ideal but expensive, because renting a time-sharing service can easily cost $1000-3000 per month.

But microprocessor manufacturers are also delivering prototype-development systems, assembled from their own microprocessors, ROM s, RAM s and I/O-ports. These systems have the capability of entering and editing source programs in assembly language and executing the object program with the actual microprocessor hardware.

One drawback compared with the time-sharing service is that these systems are much slower, because the editing capability is normally only a conventional teletype. Loading the assembler, assembly, loading the object tape and execution of the object is program can easily take form one to eight hours for a large program. It is faster if the assembler is stored in a PROM within a system and if one uses high speed I/O peripherals such as cassette tape systems CRT terminals or line printers. These devices can reduce the operating times by a factor of 100, but they are costly.

There is still another alternative, the use of an in-house computer system for program development. Microprocessor manufacturers offer assembly programs written in a language like FORTRAN, which can be used on a variety of computer systems. There is also a software group writing a high level programming language PL/M, problem-oriented and similar in complexity to BASIC and FORTRAN. To use this language one has to consider the amount of storage needed by the compiler.

Once the program is completely debugged, a PROM or EPROM can be used to store the object program and the operation of the system can start.

3

AUTONOMOUS CRATE-CONTROLLER (JCAM 10) WITH INTEL 8080 MICROPROCESSOR

by

P. Gallice and M. Mathis

Services d'Electronique, CEN Saclay, France

Received 1st July 1975

SUMMARY The autonomous crate controller JCAM-10 is designed around an Intel 8080 microprocessor, and is used with a 5k RAM and 4k REPROM memory. Data transfers between CAMAC modules and the memory are optimised with respect to software and execution time. The JCAM 10 is a microcomputer whose peripherals are all the commercially-available CAMAC modules.

INTRODUCTION

By combining the flexibility of the CAMAC international modular system and the power of integrated microprocessing circuits, the JCAM-10, 'Autonomous Crate Controller' with built-in micro-processor, allows small automatic data acquisition and processing systems, or industrial control systems, to be implemented with plug-in units chosen from among the 1 000 CAMAC modules available on the world market.

Designed around an INTEL 8080 microprocessor combined with RAM and REPROM memories, this module is in fact the central unit of a micro-computer of which the input/output/memory bus is the Dataway of the CAMAC Crate. Its technical specifications and price make it an attractive unit which compares favourably with the commercially available CAMAC interface and mini-computer assemblies.

UTILISATION

The autonomous crate controller can carry out the following functions:

- control of the installation by a program in REPROM or RAM memory;
- simple calculations on acquired data;
- print-out of results on a directly connected TTY printer or any other peripheral connected to a CAMAC module;
- data transfer from one CAMAC module to another thereby enabling the possibilities of the system to be increased;

It is above all employed as the central unit of small CAMAC single crate systems to which it gives complete autonomy. It can also be used in larger distributed systems, for which the CAMAC crate is an intelligent' terminal connected to the central computer by an asynchronous or fast link. It can be used too by the electronics engineer as a control unit for debugging modules and programs or for servicing CAMAC systems.

Naturally, in order to take advantage of all its flexibility in use, a simple software tool, such as a high level langage, will be needed to make programming easier for the user.

COMPOSITION OF THE JCAM-10 MODULE

The JCAM-10 is a 3/25 CAMAC module plugged in the Control Station of the crate. It essentially includes:

- an INTEL 8080 integrated microprocessor circuit with its associated logic system;
- a 9k 8-bit memory;
- an interface circuit to the CAMAC Dataway;
- a priority circuit for interrupt handling;
- an asynchronous coupler operating from 110 to 19,200 bauts.

The front panel comprises, in addition to the two console initialise and interrupt keys, a 16 position switch for selecting the various stored programs. The module includes three CAMAC printed boards.

The usual indicator lights and control keys of the operator console are transferred to a 2/25 ancillary module for use when debugging programs.

THE INTEL 8080 MICROPROCESSOR

Briefly, the INTEL 8080 microprocessor is an integrated MOS n-channel circuit in a DIL 40 pin case, comprising a central unit having the following main characteristics:

- memory addressing format: 16 bits;
- data format: 8 bits;
- basic cycle: 0.5µs — Duration of instructions: 2 to 8.5µs;
- 10 registers including:
  - 1 accumulator of 8 bits and 4 flags (Z, S, C, P),
  - temporary or address registers (BC, DE, HL),
  - 2 memory control registers (Program counter and stack pointer);
- 8 interrupt levels with automatic jump;
- 256 possible inputs/outputs;
- direct memory access capability;
- 74 instructions.

ORGANISATION OF THE JCAM-10 MODULE

A block diagram of the module is shown in Fig. 1.

Organisation criteria

The objectives set for the module were essentially:

- giving autonomy to the CAMAC crate;
- optimisation of data exchanges and simplicity of use.

The resulting organisational criteria are as follows:

- utilisation of the CAMAC Dataway as I/O busline;
- programming ease and flexibility of CAMAC commands;
- speed of execution of CAMAC commands, particularly of exchanges between the memory and CAMAC modules;
- optimising LAM search and handling;
- inclusion of an asynchronous coupler for the printer;
- easy use, and protection of programs by reprogrammable memory.

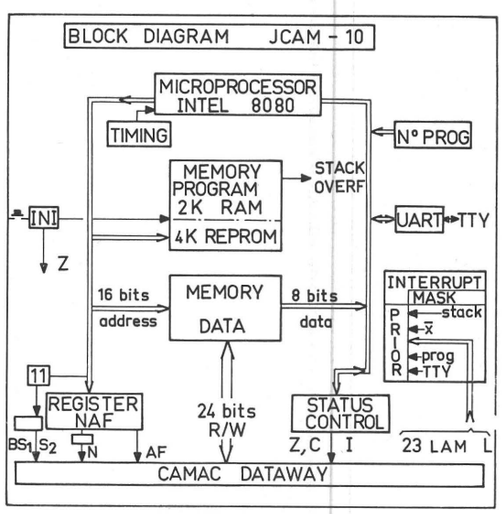


Fig. 1

Transmission of NAF

The programming ease and flexibility criteria of CAMAC commands, as well as the over-capability of the memory adress format of the microprocessor led us to make direct use of 14 of the 16 memory address bits for transmitting the CAMAC NAF instruction by neutralising 16K memory addresses among the possible 64K (2^{16}).

Hence any instruction of type | 11 | F | N | A |
having the 2 higher order bits in its address part, i.e. addressing the non-existent memory area from hexadecimal address CØØØ to FFFF, will have the effect of:

- loading the CAMAC instruction NAF register with the 14 low-order bits of the memory address generated by the 8080;
- carrying out the CAMAC cycle if this NAF represents a CAMAC control command (bit F8 = 1).

Data transmission

The second criterion, fast data exchanges between the CAMAC module and the memory, led us to organise a part of it as a double format main memory. To this effect, the area acts either as 1k 24-bit memory (CAMAC format) connected directly and in parallel to the R/W data bus lines of the Dataway, or as a 3k 8-bit memory connected to the 8 bit data bus-line of the microprocessor. The change of format is simply done by changing the memory reference address.

Thus 24 bits of information will be exchanged between a CAMAC module, designated by the content of the NAF register, and a memory position, by a simple memory reference instruction addressed to the 'page' the word length of which is 24 bits (for instance in $14ØØ_{(16)}$).

The direction of transfer is determined by the bit F16, indicating a CAMAC Read or Write command.

At data processing time, this 24-bit word will be exchanged between the memory and the 8080 central unit by 3 memory reference instructions addressed in turn to the 'hig-order' (14ØØ − 1k = 1ØØØ) 'medium-order' (14ØØ − 2k = ØCØØ) and 'low-order' (14ØØ − 3k = Ø8ØØ) pages.

This enables the JCAM-10 to be considered as a CAMAC central unit with double addressing allowing transfers to be made between the memory and CAMAC modules in two 8080 instructions only, of type:

- REFMEM ⟨NAF⟩ (Load NAF register);
- REFMEM ⟨24-bit memory address⟩ (execution of CAMAC cycle and memory transfer).

Further, according to the nature of the instruction used, i.e. M→A (or A→M), the two Q and X status bits received in answer to the CAMAC operation will (or will not) be entered in accumulator A and therefore can be tested immediately.

Organisation of the memory

In addition to this memory area, the JCAM-10 module includes a second area called program memory, itself composed of two parts:

— 2k 8-bit words of RAM memory at the beginning of which 64 locations are reserved for the immediate processing of the 8 automatic interrupt levels. The machine-context-saving push-down stack will generally be placed behind this area. Should it overflow an alarm interrupt is generated;

— 4k 8-bit words of reprogrammable memory (REPROM). This area is used for non-erasable programs.

On initialisation, the P-counter points automatically to the first address of this area.

The data memory can obviously be used also either totally or partially as an 8-bit program

Thus physically, the JCAM-10 module includes 9k 8-bit words of memory. It uses 9 + 1 + 16 = 26k addresses. This therefore leaves 38k available for memory extensions which can be connected to the JCAM-10 by a dedicated 52-line bus.

Interrupt circuit

The criteria of optimisation for LAM search and handling led us to build into the JCAM-10 a priority handling and individual masking circuit for the 8 interrupt levels accepted by the 8080, i.e.:

- 2 alarm levels: stack overflow and no CAMAC X response;
- 4 CAMAC levels, namely:
  - 2 high priority levels each of which can receive only one CAMAC LAM,
  - 1 graded LAM level with 8-bit read operation capability,
  - 1 common level receiving all the other CAMAC LAM's to be recognised by F(8) test operations;
- 1 console interrupt level;
- 1 Teletype level.

Thus 5 to 10μs after a high priority CAMAC LAM has been issued, the P-counter will point to the memory area reserved for the immediate processing of this level.

Ancillary circuits:

The JCAM-10 module also comprises:

- an asynchronous transmitter-receiver operating from 110 to 19,200 bauds, allowing direct connection with a teletype, a display or a computer asynchronous input;
- circuits for generating CAMAC signals (Initialise (Z), Clear (C), Inhibit (I)) and for reading the position of the program number switch located on the front panel;
- circuits enabling the module context to be read in case of interrupt.

PROGRAMMING PRINCIPLES

Microprocessor instructions

The 74 instructions of the INTEL 8080 microprocessor can be used in the JCAM-10:

- immediate loading or transfer between Lr_1r_2 registers (with $r = A, B, C, D, E, H, L$ or M);
- single length arithmetical or logical instructions: ($r \pm 1$, $A \pm r$, $A.+ \lesseqgtr r$, A) or double length;
- ($r_1r_2 \pm 1$, $HL \pm r_1r_2$);
- save (and restore) double length registers in the push down stack, located in the main memory;
- jump or call sub-routines and return, unconditionally or conditionally on the four flags Z, C, S, P;
- transfer of 8 bits between accumulator A and the memory by immediate addressing, indirect on HL addressing or extended addressing as from the 3 double-length BC, DE and HL registers;
- inputs/outputs and general interrupt masking.

CAMAC programming:

As a CAMAC command is represented by a memory address, and as the data memory is in direct communication with the R/W lines, it is possible to:

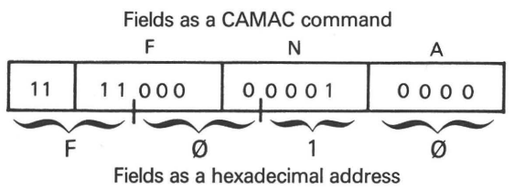
- execute commands defined by immediate values or by their storage address;
- exchange information between a CAMAC module and a memory position defined by an absolute address or an indirect address which might be indexed.

Thus, CAMAC command instructions are of the type:

- MAI ⟨11 FNA⟩, or (AMI⟨11 FNA⟩), which has the format of an instruction to transfer from A to the (non-existant) memory address 11 FNA;
- or HLM ⟨LOC⟩: loading HL registers with the content of memory LOC;
- LMr: theoretical transfer of register r to the memory addressed by HL;
- LOC DC2 ⟨11 FNA⟩.

These instructions will not affect the processor in any way but will load the NAF register. The same instructions accompanied by an address corresponding to the 24 bit page will exchange data between memory and CAMAC module.

Hence:



MAI/FØ1Ø or
AMI/FØ1Ø
will carry out the CAMAC command $N_{(1)}$ $A_{(0)}$ $F_{(24)}$
and MAI/CØ1Ø
MAI/SCAL
will carry out the command $N_{(1)}$ $A_{(0)}$ $F_{(0)}$ and will store the 24R data in the SCAL memory location.

The characteristics of the various CAMAC operations are shown in figure 2.

CAMAC command	NAF addressing	Data addressing	Mem. (8 bits)	Duration (μs)
Control	Value	—	3	7
	Indirect	—	5	13
	Preloaded (programming block)	—	1	4.5
Test	Value (or indirect)	—	7	14
Read/Write	Value	immediate	6	14
	Indirect	immediate	9	18
	Indirect	indirect	12	24

Fig. 2 Programming of CAMAC operations

Service instructions

These are conventional microprocessor input/output instructions and concern:

- transfers with the teletype: control, status and data words;
- the status of the CAMAC crate and control signals Z, C, I, (Q, X), loading and reading of interrupt mask register;
- reading the graded LAM configuration of the third CAMAC interrupt level;
- reading the position of the program number switch;
- reading the NAF register (for saving the contents).

Software

The currently available software comprises:

- A FORTRAN cross assembler operating on IBM 360;
- a TTY operating system (1 KREPROM) for loading binary tapes from the TTY reader or a fast reader (CAMAC module), debugging and running programs, as well as programming REPROM memories.

We shall shortly have a local assembler and we are starting on the study of a BASIC compiler for very simple user programming, with execution times consistent with real-time operation.

ADDITIONAL DEVELOPMENTS

Apart from implementing the software system to which we are devoting our main effort, we are currently designing general purpose CAMAC modules to increase the capacity and performance of the system: RAM (12k) or REPROM memory extensions, interleaving direct memory access control module, floppy disk interface module, floating-point operation module, REPROM programming module, as well as a module enabling the JCAM-10 to control up to 8 CAMAC crates.

CONCLUSION

The autonomous CAMAC crate controller JCAM-10 with built-in microprocessor is a CAMAC system controller which is easy to use, both from the engineering point of view and from the end user point of view. Attractive automatic systems can be built very quickly for use in scientific, industrial or medical laboratories by bringing together two powerful 'tools':

- the INTEL 8080 micropressor, the performance of which is very much akin to that of available minicomputer central units;
- the CAMAC system which gives to users a very large range of compatible and commercially available peripherals.

4

CAMOPS — CAMAC MODULAR PROCESSOR SYSTEM

by

D. Kollbach and V. Schmidt

Hahn-Meitner Institut für Kernforschung Berlin GmbH F. R. Germany

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SUMMARY A microprocessor-controlled set of CAMAC modules, linked by a private bus, has been developed for use as 'intelligent' hardware.

GENERAL DESCRIPTION AND APPLICATIONS

A CAMAC processor module which can be inserted into any station of a CAMAC crate is able to replace in many cases special and complicated hardware. This module will be used for the following applications in the medical field:

— Processing data from measuring devices in a laboratory for clinical chemistry and hematology, e.g. calculation of the hematocrit from pulse heights and number of pulses generated by a Coulter Counter D.
— Recognition and encoding of output signals from a bar-code reading pen which will be used for sample-identification in the clinical lab.
— Processing of biosignals with the aid of special ADC-modules, e.g. for electrocardiography.
— Interactive control of a video display for brightness-modulated presentation of pictures using a CAMAC refreshing memory, e.g. for presentation of scintigraphic data.

Besides, a CAMAC single-crate or even multi-crate system can be driven by such a processor module if an appropriate crate controller is employed. It seems that the 'Type U' crate controller, designed by J. Bobbitt (1), will meet the requirements.

A CAMAC Modular Microprocessor System (CAMOPS) for use in the cases mentioned above is under development by the CAMED (CAMAC in Medicine) group of the Hahn-Meitner Institute Berlin.

COMPONENTS OF THE CAMOPS

The processor module consists of sub-units communicating with an internal CAMOPS-bus. This bus is accessible on the rear panel and can be connected by a flat cable to additional modules which make use of this bus port (see figure 1).

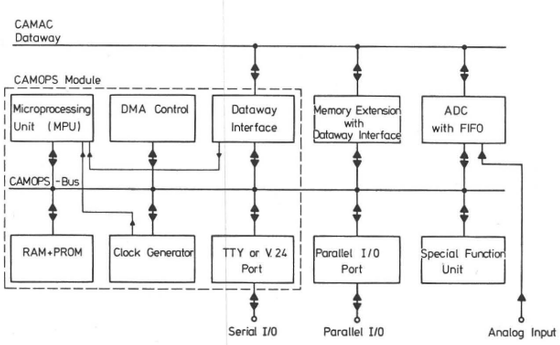

Fig. 1 CAMOPS Block Diagram

— *Microprocessing unit* (MPU) The Motorola MC6800 one-chip micro-processor is used. It is an n-Mos 8-bit device with a separate 16-bit address bus.
— *Glock* A two-phase clock generates non-overlapping pulses for the MPU and other devices. The clock frequency is about 0.6 MHz. However, the clock phases may be stretched temporarily by other devices pulling down the Memory Not Rady' line of the bus. This feature was mainly provided to meet the requirements of memories with different access times.
— *Memory* PROMs and RAMs with access times up to 3µs may be used. The word length is 8 bits. Since there is a 16-bit address bus, up to 2^{16} bytes (less any assigned for hardware addresses) may be directly addressed.
— *Dataway Interface.* This interface permits bidirectional transfer of 8-bit data or status information between the Dataway and the CAMOPS-bus. Its heart is a Motorola MC6820 Peripheral Interface Adapter ('PIA'). For synchronization, it uses the well-known LAM-features of the Dataway and the interrupt facilities of the processor. DMA may be provided.
— *Serial I/O-Port.* This TTY or RS 232 interface consists mainly of the Motorola MC 6850 Asynchronous Communications Interface Adapter ('ACIA'). It can also be equipped with DMA features.
— *Parallel I/O-Port.* This dual 8-bit TTL-level port (16-bit In or 16-bit Out, or 8-bit In plus 8-bit Out, with external handshake) consists of a Motorola PIA plus some additional hardware. DMA can be provided.
— *DMA Control.* If provided, this unit controls DMA transfers between specially equipped I/O-ports and the memory. It consists of presettable counters for word count and current address. The DMA cycles are interleaved with the program controlled transfers, so that the MPU remains totally unaffected by DMA transfers. At any one time, only one device may be enabled for DMA. During DMA cycles, the DMA control generates the appropriate memory addresses and the read/write control signal on the bus. At the end of the transfer (word count = 0), an Interrupt Request is sent to the MPU.
— *Memory Extension.* For storage of large amounts of data a separate memory extension module with an associated Dataway interface can be used.
— *ADC with Fifo-memory.* This extra CAMAC module digitizes and buffers biosignals with presettable time periods between samples.

Designation	Quantity	Signal level	Function	generated by	received by
A15 ... AØ	16	TTL	16 bit address	MPU or DMA Control	all addressable components
D7 ... DØ	8	3 state TTL	8 bit data	MPU or memory or input	any components
R/$\overline{W}$	1	TTL	read/write control	MPU or DMA control	any components
ϕ1	1	TTL	2 phase non-overlapping clock signals	clock generator	components with DMA-features
ϕ2	1	TTL			any components
$\overline{RESET}$	1	TTL	Reset	DW-interface	all components
$\overline{IRQ}$	1	TTL,Intrinsic OR	Interrupt Request	I/O-ports	MPU
$\overline{DMARQ}$	1	TTL,Intrinsic OR	DMA Request	I/O-devices with DMA features	DMA Control
$\overline{VA}$	1	TTL,Intrinsic OR	Valid Address	MPU or DMA-Control	all addressable components
$\overline{MNR}$	1	TTL,Intrinsic OR	Memory Not Ready	slow memories	clock generator
$\overline{GND}$	1	-	Ground	-	-

Fig. 2 CAMOPS Bus Signals

— *Special Function Unit.* Within the processor system, special additional hardware units for fast preprocessing of data can be provided, e.g. a fast arithmetic logic unit or a function generator. These units are not yet under development.

CAMOPS-BUS

The bus is derived from the Motorola M6800 Microprocessor System Bus. 32 signal lines, 1 return line and 1 reserved line are provided. All levels are TTL compatible. (See figure 2).

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5

CMC 8080: A CAMAC CRATE CONTROLLER WITH INTEL 8080 MICROPROCESSOR

by

E. Schöberl

Österreichische Studiengesellschaft für Atomenergie GmbH Elektronik-Institut, Forschungszentrum Seibersdorf, Austria

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SUMMARY In this 'intelligent' CAMAC crate controller there is a microprocessor (INTEL 8080 CPU) as well as a Random Access Memory (RAM) and a programmable and UV-erasable Read Only Memory (PROM). It has a serial interface by which it can be linked to a Teletype or minicomputer.

INTRODUCTION

The use of microprocessors in systems for digital control and processing offers a number of advantages such as efficiency, reliability, incremental expansion, and adaptability to other requirements. With second generation microprocessors many applications are now possible where the use of computers was previously too expensive or too complicated.

Therefore a microprocessor has been built into in the crate controller of a standardized data aquisition system (CAMAC).

The CAMAC crate controller microcomputer (CMC8080), including an INTEL 8080 CPU, can operate as a 'stand alone microcomputer system' or as a peripheral computer in conjunction with a main computer. The interconnection between the two computers can be realized serially (like a Teletype link) or in parallel (DMA channel).

In distributed systems the CMC 8080 can reduce the data stream to be handled by the main computer, make a selection of data, etc. In cases of emergency (such as interruption of the link, or first priority demand handling in process control) the CMC8080 can execute programs independently of the main computer.

The CMC8080 is built around the INTEL 8080 8-bit parallel central processing unit. Program and data storage is possible in 2k-bytes of PROM and 2k-bytes of static RAM. The memory capacity may be expanded over a 'private bus' with additional CAMAC memory modules.

The serial interface is built with a universal asynchronous receiver transmitter (UART) MOS integrated circuit.

The CMC8080 is built on two CAMAC printed-circuit boards and includes CPU, 2k-bytes of RAM, 2k-bytes of PROM, serial interface (UART), crystal controlled clock generator for CPU, Baud rate generator for UART, programmable real time clock and CAMAC logic with LAM priority encoder and interrupt vector generator. For start up procedures and test purposes a manual control console may be connected to the CMC8080.

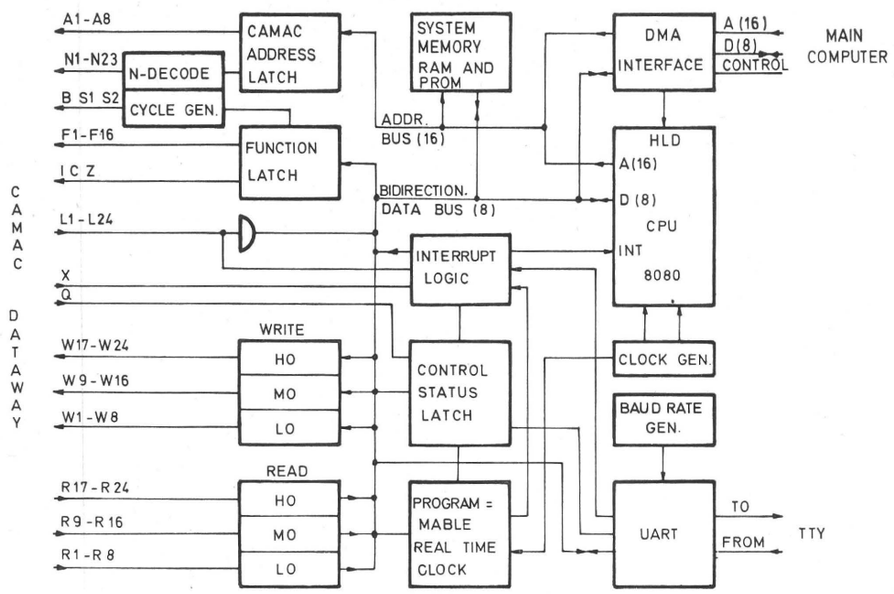

Fig. 1 CMC8080 Block Diagram

FUNCTIONAL DIAGRAM

The block diagram is shown in Fig. 1. There are four major parts, the central processing unit (CPU), the system memory, the serial interface (UART) and the CAMAC logic.

Microprocessor

The INTEL 8080 8-bit parallel central processing unit contains six 8-bit data registers, an 8-bit accumulator, four flags that can be tested, an 8-bit parallel binary arithmetic unit, a 16-bit program counter and a 16-bit stack pointer to control the addressing of the external stack.

System Memory

The system memory contains 2k-bytes of static RAM (Type 2102) and 2k-bytes of electrically programmable and UV-erasable ROM (Type 1702A). The memory is expandable to 60k bytes with additional memory modules. The upper 4k bytes are reserved for the CAMAC address.

Serial interface

One pair of ports is used for a serial communication link. Data to the UART transmitter is transfered via output port O with an output instruction. Serially received data are transfered from the UART receiver via input port O with an input instruction. The UART flags (transmitter ready, receiver ready, error) can be read with an input instruction via input port 4. An interrupt generated by the UART is fed to a priority encoder, and an automatic interrupt vector transfer to the CPU occurs, permitting a teletype service routine call. Standard transmission rates may be selected in the range 110 to 9600 baud.

CAMAC-logic

The CAMAC address and function latches are loaded if the four CPU address bits A12, A13, A14, A15 are logical 1. The CAMAC address and function transfer is realized with a memory reference instruction (called the CAMAC function operation). The low order byte of the address bus, containing the coded station number N, and the high order byte, containing the coded Subaddress A are loaded into the address latch. The remaining 3 bits of the address bus may be used in future developments for CAMAC crate addresses or special functions etc.

The data byte is latched in the function latch which then contains the CAMAC function code F, Inhibit I, Clear C, and Initialize Z. After latching FICZ the CAMAC cycle generator is started and Busy B and Strobe pulses S1, S2 are generated.

CAMAC Write and Read operations are performed with three pairs of ports.

24-bit CAMAC write data are transfered via output port 1, output port 2 and output port 3 with three corresponding output instructions. When the 24-bit write data are transfered to three output ports a following CAMAC function operation starts the CAMAC cycle and the 24 bits are moved to the addressed CAMAC module. A 24-bit read data operation may be performed with a preceding CAMAC function operation. The read data are now present at input port 1, input port 2 and input port 3. With three corresponding input instructions the read data can be transfered to the CPU accumulator. Input or output instructions do not start a CAMAC cycle.

The control status latch determines the state of the controller and it can be read via input port 4 and can be overwritten via output port 4. It contains bits for CAMAC interrupt enable- disable, X-interrupt on-off, real time clock on-off, Teletype enable-disable, reader on-off, response Q, command accepted X, ORed LAM, transmitter ready, receiver ready, and error.

The LAM pattern is available at input port 5, input port 6 and input port 7. Six specified LAMs are connected to a priority encoder and the interrupt vector generator allows six LAM-service routines to be called. The other LAMs are ORed and connected to another input of the priority encoder.

The X interrupt and the UART interrupt are ORed and connected to the highest priority input of the priority encoder.

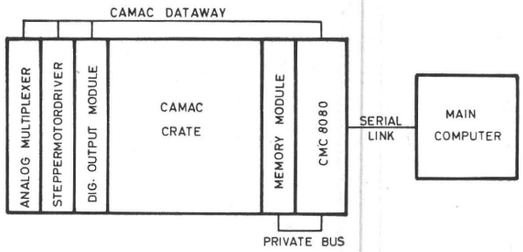

Fig. 3 Distributed Computer System (Serial)

APPLICATIONS

A typical single crate system contains the CMC 8080 crate controller, additional memory modules, a DMA interface module and conventional CAMAC modules.

The stand alone system in Fig. 2 represents a complete microcomputer system with the flexibility of the CAMAC system. A system monitor contained in PROMs functions as follows; load RAM memory from keyboard, paper tape or magnetic tape cassette; write the content of the memory on a printer, on paper tape or magnetic tape cassette; modify bytes of RAM memory; execute the program stored in the memory; and program PROMs (Type 1702A) with the CAMAC PROM programmer module.

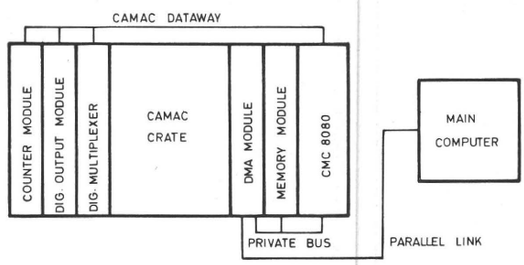

Fig. 4 Distributed Computer System (Parallel)

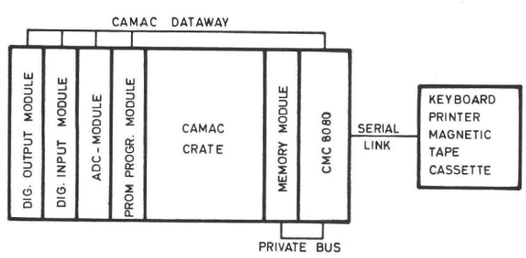

Fig. 2 Stand-Alone System

With the INTEL 8080 assembler it is possible to edit and assemble programs on the CMC8080.

The system in Fig. 2 can be used in laboratory automation, process control, etc. with the ability to develop and test software and hardware.

In distributed computer systems the interconnection can be either serially (Fig. 3) like a Teletype link or in parallel (Fig. 4) via a DMA channel.

To simplify the serial link between the two computers and to make the link computer-independent only ASCII characters are transferred, because most minicomputers use the ASCII code in serial links.

Where high data transfer rates are necessary via the DMA interface module, data transfers to and from the CMC8080 RAM are possible.

ACKNOWLEDGEMENTS

The author expresses thanks to Mr. Marschik who assembled and tested the prototype.

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6

THE MIK-X AUTONOMOUS CRATE CONTROLLER

by

D. L. Abbott

Standard Engineering Corporation, Fremont, California, USA

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SUMMARY The outstanding features of Standard Engineering Corporation's MIK-X Autonomous Crate Controller are described. This is the first commercially-available microprocessor-based CAMAC crate controller.

INTRODUCTION

A number of microprocessor-based CAMAC Crate Controllers utilizing the Intel 8080 chip have been described. The MIK-X is another 8080-based Crate Controller, but has the distinction of being first to be offered commercially. Although it shares many characteristics in common with other implementations, the MIK-X has several features worthy of note and these are the subject of this paper.

ORGANIZATION

The basis MIK-X controller consists of three printed circuit boards as shown in Figure 1. These are from right to left: The Dataway Interface board including N, A, F, and L registers plus Dataway timing and control; the Processor board including the 8080 Processor and its support logic plus a 24 bit Read/Write Data register; and either a Memory Card with up to 16K bytes of semiconductor RAM or a Block Transfer DMA Controller. All three cards are interconnected by a high speed asynchronous Memory Bus which is also brought to the outside for connection to extended memory. In addition, the Processor and Dataway Interface boards are interconnected by a separate I/O Bus for the execution of normal input/output instructions.

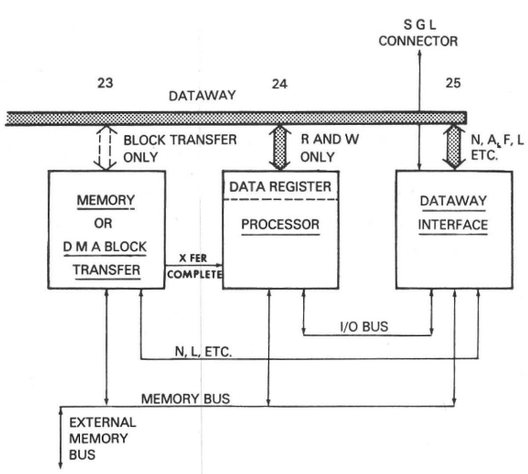

Fig. 1 Basic Organization of MIK-X Crate Controller

The Memory Bus is designed to maximize DMA data transfer rates by interleaving the Processor and a DMA Controller on a cycle by cycle basis. The Processor typically requires about 2 microseconds to execute a memory cycle. However, only about 500nsec. of this time is used to access the memory. With a properly designed Memory Bus, the remainder of this time is free to be utilized by a DMA device without interfering with the Processor. In this way, DMA operation may be made almost totally 'transparent' to the Processor. See Figure 2.

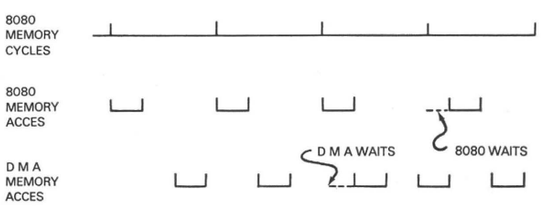

Fig. 2 Interleaving of Processor and DMA on Memory Bus

MEMORY

The Memory Bus is brought outside the Crate Controller module via arear panel edge card connector. This permits the expansion of memory by plugging in additional single-width CAMAC Memory Modules with identical edge card connectors. Several Memory Modules are available to suit different applications. These include:

- 16k bytes dynamic semiconductor RAM;
- 8k bytes static semiconductor RAM;
- 4k bytes static RAM plus 4k bytes reprogrammable PROM;
- 8k bytes reprogrammable PROM.

The memory can be expanded to 64k bytes utilizing any combination of the above modules. Any of these boards may also be used as the third card of the basic Crate Controller.

It should also be noted that the programming procedure for the recently introduced Intel 2704 and 2708 UV-erasable PROMs is sufficiently simple that programming circuitry may be included on the memory board itself. Thus the PROM may be programmed by writing to memory exactly as if it were RAM. The cycle time is of course much longer, about 500 microseconds, but the Memory Bus is asynchronous and can handle devices of any speed.

DMA BLOCK TRANSFER CONTROLLER OPTION

The memory board in slot 23 may be replaced by an optional DMA Block Transfer Controller, in which case all memory is then external to the basic Crate Controller Module. This device is in

itself a microprogrammed controller implemented with a bipolar microprocessor chip set. It implements all of the block transfer modes defined in EUR 4100-Q-Stop, Q-Repeat, and Address Scan as well as LAM triggered block transfer.

In Stop mode, it may be programmed to interpret Q = 0 as either the last valid transfer or as invalid data. In addition, it may be programmed to transfer 8, 16, or 24 bits per Dataway cycle.

DATAWAY ADDRESSING

The MIK-X Controller treats the Dataway as a block of memory locations occupying the upper 512 memory addresses. This approach derives primarily from the architecture of the PDP-11. Several other implementations similarly treat the Dataway as some subset of memory address space. Its principal feature is efficient execution of Dataway cycles, especially non-data transfer functions which may be efficiently coded in-line and execute in approximately 21 microseconds.

The data returned by a Read access to the Dataway address space is actually the Dataway Status Register including Q and X from the just completed Dataway cycle. Data transfer is accomplished through a 24-bit Read/Write register referenced by three In/Out codes. Likewise, the F code register is loaded via an output command. The Dataway Status Register is also accessible through a pair of I/O instructions.

INVISIBLE BOOTSTRAP

Another novel feature of the MIK-X is an 'invisible' bootstrap. This is implemented in a PROM chip on the Processor board. When the bootstrap mode is enabled, by depressing the front panel Bootstrap Switch, all Read accesses to memory are to the bootstrap PROM while Write accesses continue to be to the main memory. The principal function of the bootstrap is to transfer a loader program from itself to main memory and then exit from bootstrap mode by executing a Halt instruction. The loader program is then started by activating the front panel Reset Switch. In this way, a workable system may be configured in which main memory is entirely RAM.

AUXILIARY OPERATION

The most important feature of the MIK-X is its ability to operate either as a stand-alone autonomous controller or as an auxiliary to a Type L or Type A controller (Figure 3). With this capability, the MIK-X becomes the basis for modular distributed intelligence systems.

When operating as an auxiliary controller, the MIK-X is plugged into three normal module positions and connected to the master crate controller through a 52-pin connector identical to the SGL connector defined for the Type L-1 Serial Controller.

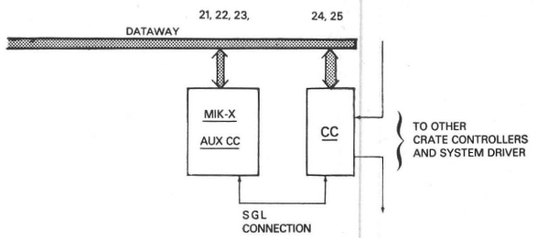

Fig. 3 The MIK-X as an Auxiliary Controller. The Crate Controller (CC) can be SCC-L1 or a variant of CC-A1

This connection provides access to the N and L lines plus priority arbitration for access to the Dataway. In addition to the Auxiliary Lock-Out signal defined for the type L-1 controller, a pair of request and grant signals is defined whereby the auxiliary controller requests Dataway access and receives acknowledgment from the master before executing its cycle. This mode is useful for Type-A and Type-U controllers which receive no warning of an impending Dataway cycle as does the Type-L.

Standard Engineering is currently developing a modified Type-A Crate Controller which includes this function. All of SEC's Type-U controllers also implement the auxiliary arbitration feature.

In this configuration, LAMs are primarily the responsibility of the Auxiliary Controller. The MIK-X detects a LAM on the SGL connector and determines through its program whether it is to be serviced locally, by the MIK-X itself, or sent on to the system driver for servicing. In the latter case, the MIK-X loads a 5-bit register with an encoded LAM number and asserts the Demand Message Initiate signal on the SGL encoder connector. This further implies that the MIK-X is capable on its own of generating demands to the system driver.

The objective of this approach is to reduce the burden on the system driver by handling locally as many service requests as possible. Demands passed on to the system driver will usually be higher level functional service requests rather than LAMs from individual modules.

CONCLUSION

By providing a conveniently packaged increment of programmable intelligence smaller than a minicomputer, the microprocessor has great potential for expanding the applications of CAMAC to real-time instrumentation systems with low performance requirements. With the features outlined above, the MIK-X is intended to satisfy a wide range of applications ranging from small stand-alone systems to large distributed intelligence networks. The data rate limitations normally associated with microprocessors are minimized through the block transfer DMA option. The MIK-X is the first in what will undoubtedly be a long line of microprocessor-based CAMAC products.

7

AUXILIARY/MASTER MICROPROCESSOR CAMAC CRATE CONTROLLER

by
E. J. Barsotti

Accelerator Division, Controls Group Fermi National Accelerator Laboratory, Batavia, Illinois, USA

Received 8th July 1975

SUMMARY This microprocessor-based CAMAC unit can be used as a crate controller or auxiliary controller. It has been developed for the serial CAMAC control system of the Fermilab experimental beam line, for applications that require local intelligence in CAMAC crates.

INTRODUCTION

In early 1972 Fermilab commissioned its serial CAMAC control system for use in the three experimental areas[1]. The first approach to a serial system was to use a serial driver connected through repeaters to several branch drivers, each controlling up to seven Type A crate controllers. Data handling requirements lead to the replacement of serial branch drivers by an in-house designed CAMAC Serial Crate Controller with block transfer capabilities[2]. As the system developed, experimenters and operators requested more and more complex data gathering and handling operations from the system[3]. Input and output block transfer operations were increased in an effort to reduce the burden on the CPU of the system computer. Crate-to-crate block transfers were provided for graphics and sophisticated console requirements. It soon became evident that 'local intelligence' in a CAMAC crate was necessary. Applications such as closed loop control and status and alarm checking of a few devices could more easily be handled by an intelligent auxiliary crate controller (ACC). As the ACC was being developed new applications emerged, some requiring an auxiliary controller and some requiring a stand-alone or master crate controller (MCC). Controlling the focusing horn in the Neutrino Experimental Area and controlling an entire experiment in the Internal Target Area of the Main Accelerator were two additional applications for the newly named Auxiliary/Master Crate Controller (A/MCC)[4].

MICROPROCESSOR HARDWARE

The auxiliary/master crate controller contains a Motorola 6800 microprocessor, $1\frac{1}{8}$k bytes of Motorola 6810 RAM and up to 8k bytes of Intel 2708 PROM memory. The microprocessor cycle time is presently 1.25 microseconds for internal memory and can be phase-modulated to 1.75 microseconds for slower external memory or peripheral addressing.

When used as an auxiliary crate controller, the A/MCC time shares the Dataway with Serial Crate Controller (SCC) block-transfer and normal-transfer Dataway cycles. At all times other than during Dataway cycles, the A/MCC can be using the Dataway for memory expansion and peripheral addressing.

Memory Expansion

Since the microprocessor is a byte (8-bit) oriented machine with capability of addressing 64k bytes of (65,536 bytes), twenty-four lines in addition to a few control lines are required to extend memory. By lowering the Dataway Busy signal while addressing memory, the A/MCC is able to use the 25 Dataway read lines for address and data along with four other bussed Dataway lines to extend memory. The only requirement is that the microprocessor be held in an inactive state during SCC or A/MCC generated Dataway cycles. This feature allows peripheral addressing and extension of memory through the Dataway to CAMAC modules without the need for external cabling.

Time sharing the Dataway between SCC programmed-transfer and block-transfer Dataway cycles and A/MCC operations still allows 99% microprocessor-CPU busy time.

Peripheral Addressing

The 6800 microprocessor allows for 256 bytes of directly addressable memory, of which 96 bytes are used for addressing peripherals and 32 are used for registers internal to the A/MCC. Using directly-addressable locations for the most frequently used memory locations allows for more efficient operation of the A/MCC by saving both program bytes and MPU cycle times.

Interrupt Handling

The microprocessor has one non-maskable and one maskable vectored interrupt. The non-maskable interrupt has three sub-levels of vectored interrupts, one each for communications from an SCC to the A/MCC, block transfer operations and, if used, a 60 Hz real time clock. The maskable interrupt has 8 sublevels of vectored interrupts. Any combination of four front panel or eight LAM signal interrupts, or a hardware timeout can be wired to the eight maskable interrupts. Sublevels of vectored interrupts are derived by latching and priority encoding the interrupts. An add instruction to the prioritized interrupt is then used to obtain a vector for servicing the interrupt. This hardware/software trade off provides relatively fast servicing of interrupts without a large amount of hardware.

Memory Allocation

The basic A/MCC contains $1\frac{1}{8}$k bytes of RAM and up to 8k bytes of PROM memory in addition to 32 bytes of internally addressed registers. The table below specifies the memory allocations for these locations in addition to that for the remaining 54k (64 − |8 + 2|) bytes of memory.

Hexadecimal Addresses	Description	Bytes
0000-007F	Directly Addressable A/MCC Internal RAM Memory	128
0080-009F	Directly Addressable A/MCC Internal Register	32
00A0-00FF	Peripheral Addresses	96
0100-07FF	A/MCC Internal RAM Memory	1792
0800-DFFF	External PROM, ROM, or RAM Memory	54k
E000-FFFF	A/MCC Internal PROM Memory	8k

A/MCC CONSTRUCTION

The A/MCC consists of two modules, one single-width and one double-width. The double-width module contains the crate controller hardware, i.e., read/write registers, station number registers, Dataway cycle timing generator, etc., in addition to hardware providing input and output block transfer capabilities through the SCC. When the A/MCC is functioning as an auxiliary controller, the single-width module contains the microprocessor, RAM, PROM, MPU clock and the timing and logic circuitry required for interleaving A/MCC and SCC Dataway cycles and extending memory via Dataway lines. A second single-width module may be used in place of the module described above when the A/MCC is used as a master controller. This module omits the timing and logic circuitry used to interleave Dataway cycles but contains circuitry for performing cycle-stealing DMA transfers. Both single-width modules may contain drivers and receivers for extending microprocessor control to additional local crates.

The A/MCC resides in any group of three slots while functioning as a master crate controller and in any three slots excluding those occupied by SCC while functioning as an auxiliary controller.

Changing from an auxiliary to a master crate controller or vice-versa is easily accomplished by the insertion or extraction of six actual dual-in-line packages. The six packages, when inserted, connect the Dataway LAM and station number lines to the A/MCC.

Access to Station Number (N) and LAM (L) Lines

A rear I/O connector and harness from the A/MCC double-width module to the control station of the crate allows the A/MCC to access station number and LAM lines when not occupying the three rightmost slots.

SCC Auxiliary Controller Lockout Signals

Five signals are required from the SCC to allow the A/MCC, to time-share the Dataway, when functioning as an auxiliary controller. These five signals tell the A/MCC when a Dataway cycle generated by the SCC is imminent. Since the SCC is the master controller, the A/MCC must relinguish the use of the Dataway until that Dataway cycle is complete. The lockout signals are transmitted to the A/MCC via the five patch pins of the Dataway. The A/MCC is held in an inhibited state by phase modulating and staticizing the microprocessor clock for a period not exceeding 2.75 microseconds.

Communications Between Auxiliary A/MCC Controller and SCC

Whenever the A/MCC is addressed by the SCC, the function code and sub-address code are stored in internal A/MCC registers along with the write data for a write function code. The latching of this data triggers the microprocessor's non-maskable interrupt, thereby initiating an application or 'type code' program predefined via A/MCC software. Thus, the F, A, and W lines define an extremely large set of 'type code' operations for various A/MCC applications.

The A/MCC communicates with the SCC via four 24-bit SCC readable registers. Four flip-flops, one for each register, are used to indicate to the A/MCC that the registers have been read by the SCC. For example, a flip-flop is set when its corresponding register is loaded and cleared when that register is read by the SCC.

Remote Device Control and Monitoring

The serial system at Fermilab allows easy communication between the experimenter computers and the main system computer by the use of two bi-directional buffered memory modules[3]. By using the same system software and making the A/MCC respond identically to one of these modules the A/MCC can control and/or monitor any device in any crate in the serial system.

ADDITIONAL FEATURES

Software/hardware trade-offs in any system are always difficult to evaluate. To ease the software burden, a 60Hz real time clock and a hardware timeout, each driving interrupts, have been incorporated into the A/MCC. Some additional features are described below.

I/O Block-Transfer Capabilities

Input block-transfers from an ACC are accommodated via circuitry and software which sequentially load one of the 24-bit registers, halt the microprocessor, and wait for a SCC-generated block-transfer read operation. This operation then takes the MPU out of the halt state and the process is repeated until the transfer is completed.

Block-transfer data operations to the ACC are accomplished in much the same manner, except that data enters the controller via a special front panel input port.

Local Multi-Crate Expansion

For systems requiring locally more than one crate of hardware, the single-width module of A/MCC can interface to a group of 'daisy-chained' crate controller interface modules. These modules are used to control an A/MCC double-width module residing in each of these 'daisy-chained' crates.

Maintenance and Testing

The front panel indicators, test points, and switches allow for simple program testing and maintenance. A program may be single-stepped or restarted periodically via front panel controls.

A/MCC APPLICATIONS

Figures 1 and 2 show typical applications[4] for the A/MCC. Figure 1 depicts the hardware necessary for operating an experiment without the aid of a large or mini-computer. Figure 2 shows a more complex system which is interconnected via an ACC to a large serial CAMAC system. This application also uses the ACC to drive two additional CAMAC crates via interface modules and double-width modules of an A/MCC.

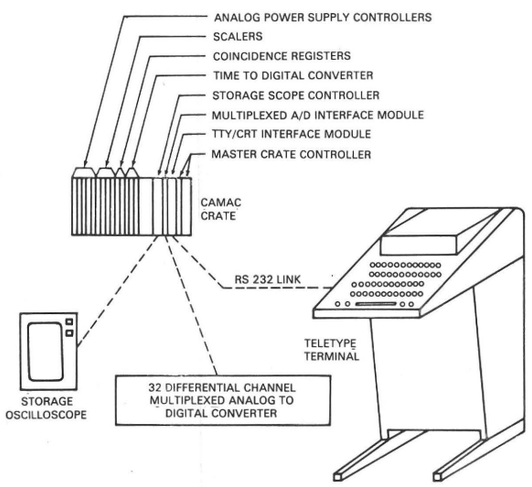

Fig. 1 Master Crate Controller Application–Stand-Alone Experiment

FUTURE DEVELOPMENTS

One of the main concerns with a device such as the A/MCC is how to test the system software initially and, if changes are required, how to make those changes easily. A CAMAC module and accompanying software will be developed to program PROM's for the A/MCC. Teletype, digital cassette, and paper tape reader interfaces will need developing to make initial software checking simpler. For large temporary bulk storage, a module containing 4-8 k of RAM memory will be developed.

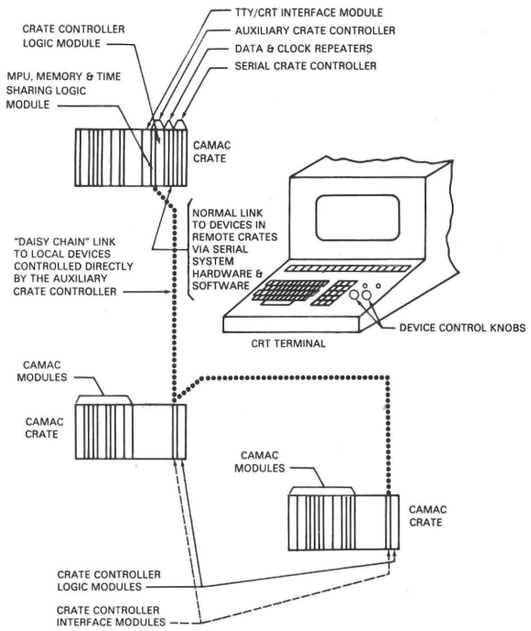

Fig. 2 Auxiliary Crate Controller Application–System with Local and Remote Microprocessor-Control

CONCLUSIONS

Microprocessors and intelligent crate controllers have indeed opened another phase of developments in the expanding world of CAMAC.

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2. E.J. Barsotti, *CAMAC Serial Crate Controller*, CAMAC Bulletin No. 6, March 1973.
3. E.J. Barsotti, *Operational Aspects of a Serial CAMAC Control System*, Nuclear Science Symposium, 1973.
4. E.J. Barsotti, *Auxiliary/Master Microprocessor CAMAC Crate Controller Applications*, submitted paper, 1975 Nuclear Science Symposium.

NEWS

CAMAC — IEEE FULLY APPROVED

CAMAC is now a fully approved IEEE standard, contained in publication IEEE Std 583. This, to a large extent, replaces USAEC Reports TID-25875 (derived from EUR 4100e) and TID-25877 (referenced in Supplement to CAMAC Bulletin No. 6) which are to be phased out.

Louis Costrell (Chairman, US NIM Committee), in announcing this, expresses the hope that the wider availability of this publication should result in expanded use of CAMAC in disciplines outside the nuclear area.

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FAST AUTONOMOUS CRATE CONTROLLER

by

I. Bals, M. Caprini, B. Goran

Institute for Atomic Physics, Bucharest, Romania

Received 12th May 1975

SUMMARY This CAMAC crate controller includes a processor constructed from SSI and MSI components. It is intended for small single-crate systems where a computer would be too expensive and an LSI microprocessor too slow.

SYSTEM DESCRIPTION

For many applications where a single CAMAC crate is used the cost of a computer and specialized sofware will be more than the cost of a specialized non-CAMAC instrument doing the same work. To keep down the price of the system while maintaining CAMAC versatility, various systems without computers were designed[1–4], where the function of the computer is taken over by a special controller.

Our controller is a four-width CAMAC module and occupies the control station and three adjacent normal stations. The module contains the following sections:

- CAMAC section, which fulfils the functions of a Crate Controller, including the Hold facility[5].
- CPU, which provides arithmetic and logic operations, conditional and unconditional jumps, besides the generation of a sequence of CAMAC commands; the unit is organized like a minicomputer CPU but has the CAMAC Dataway as I/O bus.

To keep the size of the module small and to allow more flexibility to the system, the controller has no other internal memory, except 8 internal registers. For data handling, the controller works with data memory modules (24-bit words), connected through the Dataway as any other CAMAC module, practically without any capacity restrictions. Programs are stored in memory modules (16-bit words), connected via a special bus with a 31-pin connector on the rear panel. Speed is improved by means of this connection, because no CAMAC cycle is needed to fetch the next instruction, and overlapping is allowed. The maximum number of words for the program memory is 1024. For testing purposes, and in small systems, a diode ROM module with 256 words has been developed. A configuration with ROM (for bootstrap loading) and Read-Write program memory modules may be used, special facilities being implemented for loading the control store from the front panel switch register or from other modules such as controllers for magnetic tape units or paper tape readers.

CPU STRUCTURE

The CPU is designed around an Arithmetic and Logic Unit (ALU) with two data buses (Source and Destination) and a set of registers. The ALU performs parallel operations between 24-bit words, thus providing high speed manipulation of full CAMAC words.

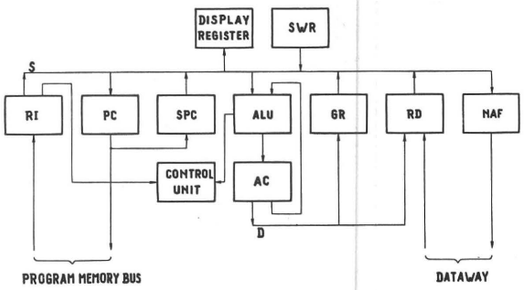

Fig. 1 Processor Structure

The general structure of the controller is presented in Fig. 1. It contains the following registers:

- RI (16-bit) – Instruction Register – contains the current instruction;
- PC (10-bit) – Program Counter;
- SPC (10-bit) – Save Program Counter Register – contains the old contents of the PC for jumps at subroutines and interrupts;
- AC (24-bit) – Accumulator (used also in shifts);
- GR (24-bit) – 8 General Registers;
- SWR (16-bit) – Front Panel Switch Register;
- RD (24-bit) – Data Register – connected with Dataway Read and Write lines;
- NAF (14-bit) – CAMAC Command Register.

The control unit generates all the micro-orders for instruction execution by decoding through random logic the various fields of the instruction; the code for the ALU is generated by means of a table written in a 32-word 8-bit PROM, to save space in the instruction.

The timing of the unit is achieved using a 10 MHz clock and a synchronous decade, providing a fixed cycle of 1 μsec for normal instruction and a variable cycle of at least 1.2 μsec for CAMAC instructions (a handshake principle is used to allow the Hold mode).

The control unit stores the status of the ALU after each instruction (overflow, carry, sign, zero) as well as Q status, seven L signals (selected by patching) and their sum D from the CAMAC unit; there are also two flags F1 and F2 available to the programmer and another one controlled by a front panel switch. The D signal (masked by F1) interrupts the program, saves the contents of PC and starts the execution of the instruction stored in the first address of the program memory.

INSTRUCTION SET

The set contains 4 classes of instructions:

- CAMAC instructions, which provide CAMAC commands NAF (16-bit);
- FUNCTION instructions – a total of 18 types of

arithmetic and logic operations are performed (Addition, Difference, Increment and Decrement Source Register, Increment Accumulator, Clear, Transfer, Complement, Two's complement, AND OR, Exclusive OR, arithmetic shift left or right, logical shifts left or right, rotate shift left or right);

- JUMP instructions;
- CONTROL instructions.

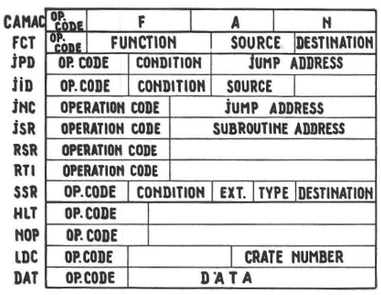

Fig. 2 Instruction Fields

Field Structure

The field structure of the instructions is shown in fig. 2 and has the following meaning:

- CAMAC – command (NAF);
- FCT – the DESTINATION register will contain the results of the operation (specified in the FUNCTION field) on the contents of SOURCE and AC registers;
- JPD – Direct conditional jump; the tested conditions are zero in accumulator, carry or overflow after an arithmetic or shift operation, sign of the results, Q after a CAMAC instruction, D signal (logical sum of L lines) and the flags F1 and F2;
- JID – Indirect jump; the jump address is contained in the SOURCE register;
- JNC – Unconditional jump;
- JSR – Jump to subroutine;
- RSR – Return from subroutine;
- RTI – Return from interrupt;
- SSR – Conditional skip, set or reset of a flag specified by DESTINATION field; the cordition can be extended over 8 externaly accessible flags (seven from the L lines and one from the front panel);
- HLT – stops the program;
- NOP – No operation instruction;
- LDC – Load crate register; this instruction was introduced to allow future development of a multicrate system by changing the number of the addressed crate;
- DAT – Data transfer from program to RD register.

IMPLEMENTATION AND EXTENSION

The controller is implemented on four boards using SSI and MSI bipolar integrated circuitry achieving a higher speed than the presently commercially available LSI CPUs.

The front panel is provided with a Switch Register for loading the start address of programs, for loading constants in General Registers and for examining the contents of General Registers or memory addresses, depending on the push button pressed (START, LOAD ADDRESS, LOAD CONTENT or EXAMINE). 26 LED s are used to display the PC register and the 16 less-significant bits of the SOURCE bus. For debugging a single-instruction mode is provided.

For early applications of the PCC, where a more sophisticated interrupt system was not necessary, programmed demand servicing was used. In later versions we will use a specialised LAM Grader for vectorized interrupt servicing.

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4. Biswell, L.R., Rajala, R.E., Design and Operation of a Micro-programmed Branch Driver for a PDP-11 Computer, Los Alamos Sci. Lab., LA-5144, May 1973.
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NEWS

USE OF CAMAC IN EUROPEAN SPACE AGENCY DATA HANDLING SYSTEMS

Mr. D. Deaney of ESRO has revealed a fairly extensive use of CAMAC in Satellite check-out as follows:

For the spacecraft integration, testing and launch phases, ESA is using a computer-based check-out system to control and monitor the spacecraft. Currently eleven such systems are in use and they have been standardized to simplify all the logistics concerned with their deployment and utilisation. CAMAC is used extensively in these systems where special peripheral assemblies such as telemetry, telecommand, timing etc. (see figure 1) have to be interfaced to the controlling computer.

In most applications a CAMAC branch highway controller is interfaced to a Modular One dual processor computer system. The CAMAC modules are connected to the various special peripherals which communicate with the spacecraft under test (see figure 2).

The specially designed controller is interesting because it incorporates a maximum of four autonomous transfer units with automatic register switching and these units may be software assigned to any CAMAC normal station. They were incorporated in the design both to cope with the data transfer rates and to permit the maximum use to be made of the flexible direct memory access features of the Modular One store units.

The systems have been developed to European Space Technology Centre (ESTEC) specification, by Logica under sub-contract to Computer Technology Limited.

Given the requirement for flexibility and the involvement of different manufacturers' subsystems, CAMAC is a great help to achieve as closely as possible the desired standardization of the systems.

For the future there are proposals to interface experiment payloads to the manned SPACELAB LABORATORY data handling facility via a CAMAC system. In this case a true CAMAC is foreseen for the ground preparation phases which would be replaced for flight by a system completely CAMAC signal compatible but packaged to flight standards.

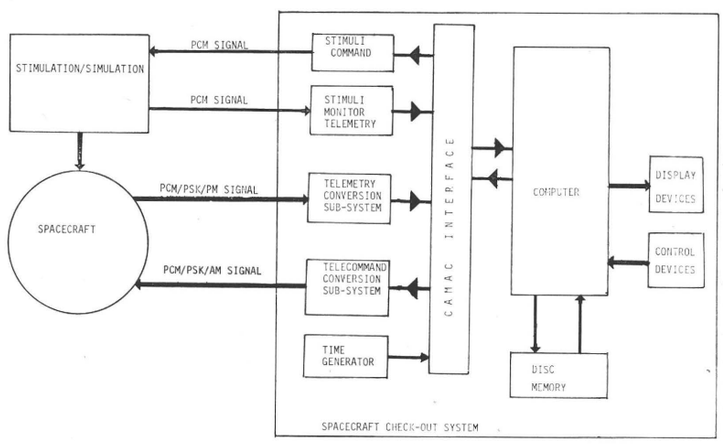

Fig. 1 Spacecraft check-out configuration

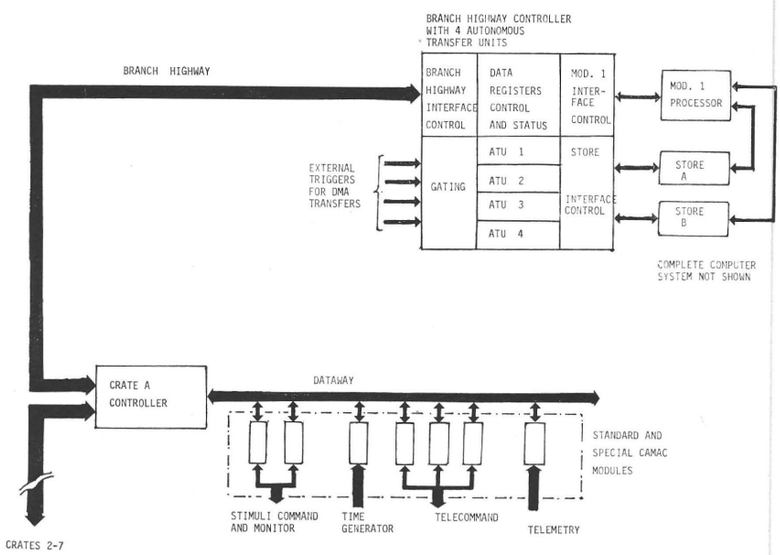

Fig. 2 CAMAC Interface configuration

ESONE-NIM COMMITTEES

ACTIVITIES OF THE CAMAC WORKING GROUPS

The ESONE Committee in Europe and the U.S.AEC NIM Committee in America have both authorised different working groups to investigate specific aspects of CAMAC. The European and American working parties are performing their activities in close collaboration.

NIM-CAMAC WORKING GROUPS

Data Working Group

Chairman: F. Kirsten, Lawrence Berkeley Laboratory, USA.

The NIM Dataway Working Group held its summer meeting on July 22 and 23 at the facilities of the National Bureau of Standards, Boulder, Colorado. We were pleased to have Rupert Patzelt, chairman of the ESONE Dataway Working Group, at the meeting.

It is clear that the end of the first phase of the Serial Highway System work is in sight. At Boulder, only two or three points were discussed which involved possible amendments to the Serial Highway Description. The Description therefore seems to have reached maturity.

Attention is now turning to the work of transferring the technical definitions of the Description into the more formally written Specification. The progress of the draft of the Specification, which is being prepared by R.C.M. Barnes, is being followed very carefully. At Boulder, the Working Group reviewed the present draft and will continue this work in future meetings.

The Working Group has recently begun discussions on the topic of Distributed Intelligence in CAMAC. The group feels that the continued vitality of CAMAC depends on developing procedures and techniques for accomodating intelligent modules and controllers (e.g., microprocessors) in the CAMAC system. Some of these techniques will develop naturally; others may require definition.

One of the first tasks undertaken is the extension of the multiple crate controller concept, which is now supported by the Serial Highway System, into other areas of CAMAC. Other tasks are being formulated and examined. Paul Kunz of SLAC is organizing this work.

Software Working Group

Chairman: R.F. Thomas, Jr., Scientific Laboratory, Los Alamos.

The NIM Software Working Group met in Boulder, Colorado, on July 23rd to 25th. The latest draft of a document describing recommended block-transfer modes was discussed in a joint meeting with the Dataway Working Group. Other items discussed included new drafts of a proposed CAMAC Software Handbook, recommendations for FORTRAN subroutines, and recommendations for extensions to BASIC.

ESONE-CAMAC WORKING GROUPS

Analogue Signal Working Group

Chairman: T. Friese, Hahn-Meitner-Institute, Berlin.

During the AWG-meeting on 28/29th of Nov. 1974 at MPI (Munich-Garching) the specifications, presented to the ESONE-meeting at Warsaw, have been revised once more because, until now, only a small number of applications in CAMAC systems exist. For some of the larger instrumentation systems, special standards have been used and this shows that specific technical circumstances or demands of peripherals may hinder the introduction of common obligatory specifications. The AWG therefore decided to make only recommendations and to separate the current- and voltage-signal specifications. These however do refer to signal transmission between CAMAC units and between CAMAC units and external devices and should be used on all CAMAC analogue modules in common usage. They also should be applied to the instrumentation of larger measuring systems, if no other conditions are prescribed by the peripherical equipment. The separation of the recommendations into current- and voltage-signals will make the work on changes and supplements easy for one or both signal systems in the future.

A special problem was encountered in the overvoltage protection of the CAMAC inputs and outputs connected to external equipment and measuring systems. The short recommendations on this point surely may be improved in the future. The minimum demand should be kept in mind that the crate detaway is not allowed to be damaged or disturbed under any circumstances. In addition to the recommendations some comments and remarks have been worked out, which may be helpful for the design engineer as well as for the user.

With the presentation of these recommendations, the work of the AWG has now come to a conclusion. Further questions referring to CAMAC analogue signals for measurement and control should be discussed between representatives of CAMAC producers and large user companies taking advantage of the interaction between practical usage and the definition of extended or new recommendations.

MEMBERSHIP OF THE ESONE COMMITTEE

This list shows the member organisations and their nominated representatives on the ESONE Committee. Members of the Executive Group are indicated thus*.

International	European Organization for Nuclear Research (CERN)	*F. Iselin**	Genève, Suisse
	Centro Comune di Ricerca (EURATOM)	*L. Stanchi*	Ispra, Italia
	Bureau Central de Mesures Nucléaires (EURATOM)	*H. Meyer**	Geel, Belgique
	Institut Max von Laue - Paul Langevin	*NN*	Grenoble, France
	Joint Institute for Nuclear Research	*B.V. Fefilov*	Dubna, USSR
Austria	Studiengesellschaft für Atomenergie	*W. Attwenger*	Wien
	Inst. für Elektrische Messtechnik, T.U.	*R. Patzelt*	Wien
Belgium	Centre d'Etude de l'Energie Nucléaire	*L. Binard*	Mol
Denmark	Forsögsanläg Risö	*P. Christensen**	Roskilde
England	Atomic Energy Research Establishment	*R.C.M. Barnes*	Harwell
	Culham Laboratory	*A.J. Vickers*	Abingdon
	Daresbury Nuclear Physics Laboratory	*A.C. Peatfield**	Warrington
	Rutherford High Energy Laboratory	*M.J. Cawthraw*	Chilton
	University of Oxford	*R. Hunt*	Oxford
	University of York	*I.C. Pyle*	Heslington
Finland	Institute of Radiation Physics	*B. Bjarland*	Helsinki
France	Commissariat à L'Energie Atomique	*M. Sarquiz**	Paris
	Centre d'Etudes Nucléaires de Grenoble	*J. Lecomte*	Grenoble
	Centre de Recherches Nucléaires	*G. Metzger*	Strasbourg
	Laboratoire d'Electronique et d'Instrumentation Nucléaire du Centre Universitaire du Haut Rhin	"	Mulhouse
	Laboratoire des Applications Electroniques de l'Ecole d'Ingénieurs Physiciens	"	Strasbourg
F.R. Germany	Deutsche Studiengruppe für Nukleare Elektronik c/o Physikalisches Institut der Universität	*B.A. Brandt*	Marburg
	Deutsches Elektronen-Synchrotron	*H.-J. Stuckenberg*	Hamburg
	Hahn-Meitner-Institut für Kernforschung	*K. Zander**	Berlin
	Kernforschungsanlage Jülich	*K.D. Müller*	Jülich
	Gesellschaft für Kernforschung	*J.G. Ottes*	Karlsruhe
	Institut für Kernphysik der Universität	*W. Kessel*	Frankfurt/Main
	Max-Planck-Institut für Plasmaphysik	*D. Zimmermann*	Garching
Greece	Demokritus' Nuclear Research Centre	*Ch. Mantakas*	Athens
Hungary	Central Research Institute for Physics	*J. Biri*	Budapest
Italy	Comitato Nazionale Energia Nucleare (CNEN)	*B. Rispoli**	Roma
	CNEN Laboratori Nazionali	*M. Coli*	Frascati
	CNEN Centro Studi Nucleari	*F. Fioroni*	Casaccia
	Centro Studi Nucleari Enrico Fermi	*P.F. Manfredi*	Milano
	Centro Informazioni Studi Esperienze	*G. Perna*	Milano
	Istituto di Fisica dell'Università	*G. Giannelli*	Bari
Netherlands	Reactor Centrum Nederland	*A.T. Overtoom*	Petten
	Instituut voor Kernphysisch Onderzoek	*E. Kwakkel*	Amsterdam
Poland	Instytut Badan Jadrowych	*R. Trechciński**	Swierk K/Otwocka
Romania	Institutul de Fizica Atomica	*M. Patrutescu*	Bucaresti
Sweden	Aktiebolaget Atomenergi Studsvik	*Per Gunnar Sjölin*	Nyköping
Switzerland	Schweizerische Koordinationstelle für die Zusammenarbeit auf dem Gebiet der Elektronik	*H.R. Hidber*	Basel
Yugoslavia	Boris Kidrič Institute of Nuclear Sciences	*M. Vojinovic*	Vinča Belgrade
Affiliated Laboratories			
Canada	TRIUMF Project, University of British Columbia Simon Fraser University, University of Victoria, University of Alberta	*W.K. Dawson*	Edmonton
	Laboratoire de l'Accélérateur Linéaire	*M. Truong*	Orsay
German Dem. Rep.			
	Akademie der Wissenschaften der DDR	*J. Lingertat*	Berlin

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L. COSTRELL (Chairman) National Bureau of Standards – Washington, DC.

APPLICATION NOTES

1

A FAST DATA ACQUISITION PATH BASED ON A CAMAC MEMORY SYSTEM

by
R. Klesse and A. Axmann
Institut Lave-Langevin, Grenoble, France

Received 16th June 1975

SUMMARY High data rates, up to 500 kHz, are handled by this CAMAC-based data acquisition system, which also meets a need for on-line data reduction. By using new MOS technology, a memory with 4 k × 16-bit words is contained in a reasonably priced single-width module. On-line data reduction minimises the memory needed for multi-channel analysis.

INTRODUCTION

A neutron small-angle scattering instrument using a plane multidetector and facilities for time-of-flight analysis of scattered neutrons is operational at the High Flux Reactor in Grenoble[1]. The considerable amount of data to be collected on line required the development of a special data acquisition system which will be described below.

Fig. 1 shows the general experimental layout. The instrument of a total length of 80 m is located at the end of a curved neutron guide tube transmitting neutrons moderated in a cold source at 25 °K. The neutron flux at the sample can vary between 10^5 and 10^8 n/cm^2/sec in a wavelength range from 2 to 20Å. Sample-detector distances between 0.7 and 40 m are possible.

The multiple information at the multidetector emanating from a single neutron capture event is amplified and discriminated by amplifiers associated with each line and column. These pulses are treated by a coding unit which gives a binary word corresponding to the address of the event (4096 cells, requiring 12 bits for address).

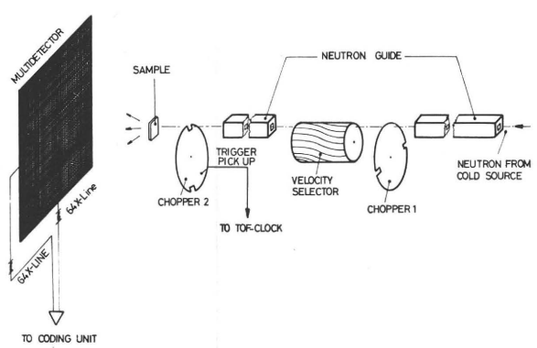

Fig. 1 Basic layout of the neutron small angle scattering, instrument D 11 at the high flux reactor (ILL, Grenoble)

FAST DATA ACQUISITION PATH

Because of the high incident neutron flux we obtain data rates up to 300 KHz (events/second) and large spectrum widths (up to 512k channels). This requires considerable activity in on-line data reduction (to reduce the spectrum width) and on-line data acquisition. An event is determined by the multi-detector address of 12 bits, plus time-of-flight information of up to 7 bits. This gives a total word length of 19 bits which would give a spectrum width of 512k if no data reduction were performed. However, the multidetector word of 12 bits can often be reduced by taking advantage of the symmetry of the spectrum.

Fig. 2 shows an original spectrum of the multidetector with 4096 points. As the spectrum has rotational symmetry, the multidetector address of 12 bits can be reduced to a word of 5 bits representing only the distance between the symmetry center and the multidetector cell. In general, for a specific experiment, the parameters concerning the symmetry properties of the expected spectrum are fed into the computer. The computer itself calculates the list of channels to be regrouped and loads the CAMAC Memory Module (MM) (initialization of electronics).

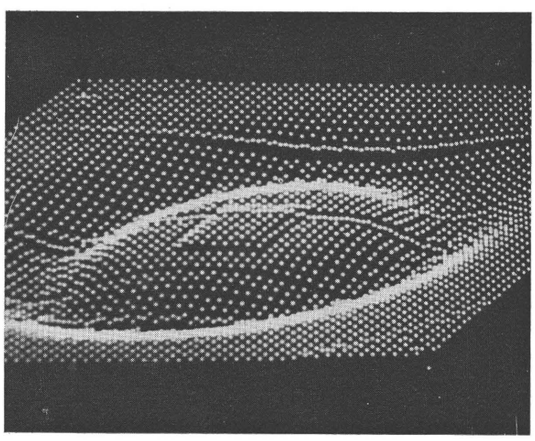

Fig. 2 Three-dimensional display of data collected with the multidetector. The intensity for each cell is given in the vertical direction. The unscattered neutron beam has been suppressed by a beam trap.

Instead of performing repetitive calculations for on-line data reduction (e.g $.r = |\sqrt{x^2+y^{2'}}|$) we now use the CAMAC Memory Module (MM), which contains only the corresponding radius for all cells of the multidetector. Thus, data reduction is simply done by a read cycle of the MM. Furthermore, the replacing data word can also determine that all events corresponding to a certain multidetector address are ignored.

Fig. 3 shows the whole data path. The next step after data reduction by the MM is the Bit Handling Module (BHM) where the final data wordt is built.

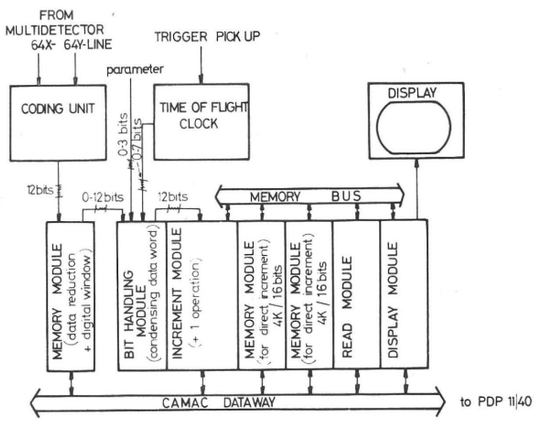

Fig. 3 Fast data path for the small angle scattering instrument

Data from three possible data sources are collected: Multidetector (reduced addresses), time-of-flight and optional parameters (sample). A control word given by the computer indicates the valid bits for each data source, and the final condensed data word is built by a simple shift operation.

The BHM sends the condensed data word to a multichannel analyser.

Fig. 4 shows this part of the data acquisition in more detail. The multichannel analyser consists of one or more (up to 16) Memory Modules, and Access Modules such as Increment Module. Read Module and Display Module. The whole system consists of fully programmable CAMAC modules which are connected by a Front Panel Bus (FPB). This FPB contains 16 lines for address, 16 lines for data, 1 'access demand' line, 1 'receipt' line, 1 'demand accepted' line, 1 'read/write' line and 1 'busy' line. Priority for access to the MM is given to the unit which is physically nearest to the MM. Three types of MM access can be performed: Read cycle (450nsec), write cycle (450nsec) and read/modify/write cycle (900nsec).

The MM is a single-width CAMAC module and has a capacity of 4096 words of 16 bits and is built from dynamic MOS memory chips.

The Increment Module performs the +1 operation to update the spectrum.

The Read Module offers a block transfer facility for memory data, which are read out during data acquisition via the FPB.

The Display Module monitors the live data acquisition into the memory.

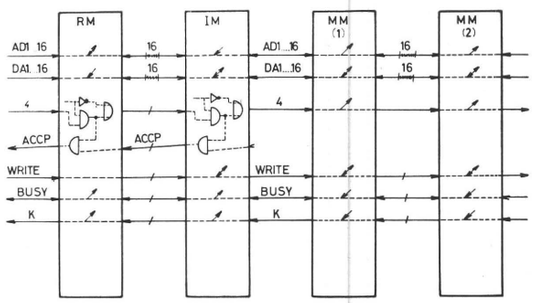

Fig. 4 Memory Bus System — detail of fast data path

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1. Schmatz, W., Springer, T., Schelten, J. and Ibel, K. (1974), *J. Appl. Cryst.*, 7, pp. 96-116.
2. Allemand, R., Bourdel, J., Roudaut, F., Jacobe, J., Ibel, K., Convert, P., Farnoux, B., Coton, J.-P., (1975), *Nucl. Instr. and Methods*, to be published.

NEWS

CAMAC Survey 1974

One of the first tasks of the EUROPEAN CAMAC ASSOCIATION, after its formation in May 1974, was to establish a datum of existing uses of the CAMAC Standard Interface.

From the responses received on the CAMAC SURVEY 1974 proforma, which has been distributed to CAMAC users and manufactures in the beginning of 1975, an analysis of usage has been done and the results, given in the final report, should guide the future programme of the Association and other interested orginazations.

All those who have returned the questionaires of the proforma will receive their copy of the final report free of charge, Others may order the report from the address given below:

European CAMAC Association
c/o Dr. H. Meyer
Commission des Communautés Européennes
CRC-BCMN
B 2440 Geel (Belgium)

The price per copy is: 150 Belgian Francs

2

CAMAC LINK BETWEEN TWO PDP-8 COMPUTERS

by

P. Daujat

Département de Physique Nucléaire — Service de la Métrologie
et de la Physique Neutroniques Fondamentales, CEN Saclay, France

Received 5th May 1975

SUMMARY A CAMAC intercommunication link between a PDP-8E and PDP-8I is described. The link consists mainly of standard CAMAC modules, and is adaptable to the particular needs of on-line measurements and control of photonuclear experiments.

INTRODUCTION

Recently initiated photonuclear experiments of the (γ, xn) type, performed at the 600 MeV Linac at Saclay, use a continuously variable energy monochromatic photon beam ($20\,\text{MeV} \leqslant E_\gamma \leqslant 120\,\text{MeV}$) obtained by the annihilation-in-flight technique of a monochromatic position beam. These experiments led to the simultaneous use of two computers:

- A PDP8(E) which controls the position and photon beam behaviour and associated equipment.
- A PDP8(I) which is used for the acquisition, preliminary mathematical evaluation and storage on DECTAPE units of the pertinent photonuclear experimental results such as photon spectra, neutron counts, several background measurements and associated cross-section computations.

The ultimate aim of automatic control of such experiments, and in particular the change in energy of the photon beam, would then require intercommunication between these two computers. Since the computers were already equipped with CAMAC interfaces an adaptation of listed and available CAMAC units proved to be an inexpensive and rapid means of attaining this objective.

LINK DESIGN

Single-width, '9013 Driver/Input 24 bit' modules from Nuclear Enterprises are used for each computer (Fig. 1). Since transfer synchronization requires a SYN signal which, on the above modules is not available with 24 bits, a dual monostable multivibrator SN 74-123 is inserted into each module so as to produce the missing signal. A pin on the connector gives access to this signal.

The CAMAC function F(16) triggers the first monostable and loads the output register in such a way that the scond monostable, which produces SYN, can only be triggered after an appropriate time delay thus assuring a proper loading of the output register.

The connection between the 9013 modules consists of 48 data, 2 sync and 2 earth lines. Each 9013 module consists of; a 24-bit output register, 24 input gates, a LAM flip-flop and a SYN pulse generator. Input lines to the 9013(E) are connected to outputs of 9013(I), and the LAM of 9013(E) is connected to SYN of 9013(I). Similarly for the (I) to (E) connection. The 24-bit transfer is performed in parallel. F(16) is used either for emitting or for acknowledging the reception of a 24-bit word. F(1), as usual, performs the reading of any word and F(8, 10, 24 and 26) are involved with the LAM only.

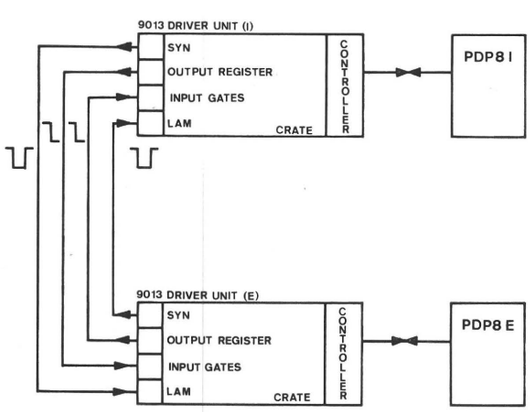

Fig. 1 Layout of the Link.

LINK PERFORMANCE

Both computers operate on 12-bit words whereas the corresponding 9013 modules have 24-bit words. Hence one could transmit two PDP8 words simultaneously. However the transmission reliability is greatly improved if one uses the 12 low-order bits for data transmission and the 12 high-order bits for identification purposes only.

Word Transfer

The sequence of operation is shown in Fig. 2. Function F(16) loads the output register of the 9013(I) with a word to be transferred. Once loaded, the module emits SYN towards 9013(E), and

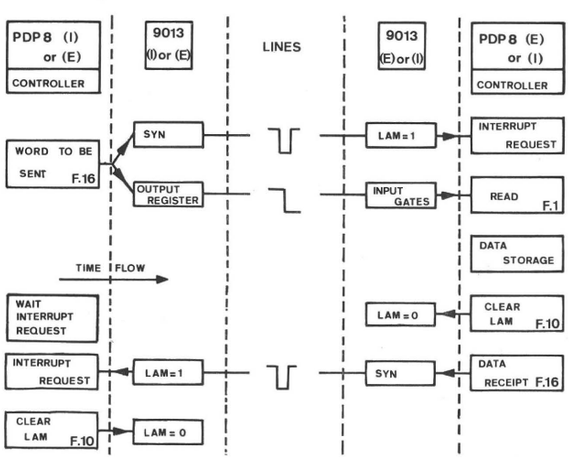

Fig. 2 Sequence of Operations in the Link.

causes a LAM in the latter. The PDP8(E) now reads the transmitted word with F(1) and memorizes it, clears the LAM, and emits SYN to the PDP8(I) by means of F(16). The receipt of this signal by the PDP8(I) is in turn acknowledged as a DATA RECEIPT. The process can then be repeated.

Block Transfer

The same procedure is used to transfer a block of words, but the sequence is labelled with the following identification codes;

1 = start of block; 0 = data; 2 = end of block.

With identification 1 and 2 one sends the number of words in the block and parity control respectively, so as to make control of the block transmission by the receiving computer possible.

Transfer Performance

The bidirectional connection transmits 24 bits in a parallel asynchronous mode. The distance between the modules can exceed 100 meters and the transfer speed, which in our experimental set-up is approximately 100 microseconds per word, depends essentially on the associated software.

If one were prepared to use the 12 bits assigned to identification words for the transfer of additional data one could then nearly double the transmission speed at the price of a loss in reliability of the transfer as a whole.

CONCLUSION

The particular example of a link described here seems to indicate that the complexities and continual evolution of nuclear experimental techniques can be met successfully by the application of properly adapted modular CAMAC systems, which are neither subject to excessive cost nor to overlong development and testing time. The standardization of both the computer and associated CAMAC modules have made the application of such intercommunication techniques possible.

NEWS

REMOTE AUTONOMY WITH INTELLIGENT SUBSYSTEMS ON THE CAMAC SERIAL HIGHWAY

The following information has been received from K.-D. Müllerhof Kernforschungsanlage Jülich.

The CAMAC Serial Highway has already proved to be a low cost solution for connecting CAMAC systems over long distances to a computer, for data acquisition and process control.

The general disadvantages of serial transmission systems in comparison with parallel transmission are, for instance, lower data rates and longer reaction times. On the other hand, the possibilities of applying modern microprocessors and small semiconductor storage elements – the microcomputer in a CAMAC module – has encouraged development work on remote autonomy with intelligent subsystems.

An autonomous crate controller for connecting a CAMAC crate to a computer via the Serial Highway has been developed at the KFA Jülich.

The equipment allows peripheral units connected to CAMAC modules in a crate to be controlled via the Dataway.

The conversation with the central computer via the Serial Highway can to a great extent be restricted to block transfers of data and program statements.

At the Interkama (Düsseldorf, F.R. Germany in October 1974) an intelligent subsystem was demonstrated which showed its potentialities by controlling the movements of model railway waggons in a station.

DEVELOPMENT ACTIVITIES

1

A DIFFERENTIAL DISCRIMINATOR IN CAMAC

by

D. Kollbach and H.-U. Nachbar

Hahn-Meitner-Institut für Kernforschung Berlin GmbH, Germany

Received 26th February 1975

SUMMARY This CAMAC module discriminates the ampli udes of analogue inpu signals, up o −1 v or +5 v in ei.her differen.ial or dual integral mode, and generates standard NIM output pulses of −16 mA. The modes of operation, the thresholds, and other features are selected by CAMAC commands.

INTRODUCTION

In nuclear physics and nuclear-medical diagnosis applications it is often necessary to measure the activity of a radiation source within a certain energy range.

The discriminator which is described here accepts fast pulses with a minimum pulse width of 30 ns in the −1 V/50 Ohm range. Slower input signals may be connected to the +5 V/5 kOhm input. [See CAMAC specification EUR 5100 (1974)].

In a well known manner the circuit compares the amplitude of input pulses with two inherent thresholds in differential or dual-integral discriminator mode. All outputs are standard NIM −16 mA signals of 50 ns width. The pulse pair resolution is about 150 ns. The mode of operation and threshold levels are controlled via the Dataway.

MODES

Dual Integral Discriminator Mode

In this mode the unit works like two independent integral discriminators with the thresholds UØ and U1. An additional output (Out 3) delivers pulses if the pulse amplitudes are within the window U1 − UØ, (U1 > UØ) (Fig. 1). The output signals are generated when the trailing edges of the pulses have crossed the thresholds.

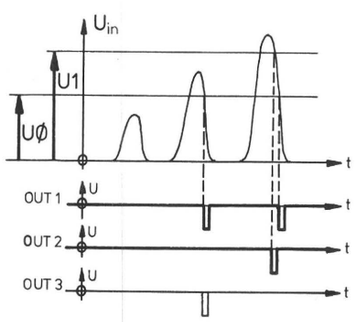

Fig. 1 Dual Integral Discriminator

Symmetrical Window Dicriminator Mode

In the other mode of operation the center of the window is controlled by UØ while the width of the symmetrical window equals 1/8 U1 (Fig. 2). By this the setting of window width and window center are independent of each other. The reduced window range results in higher resolution and lower temperature drift.

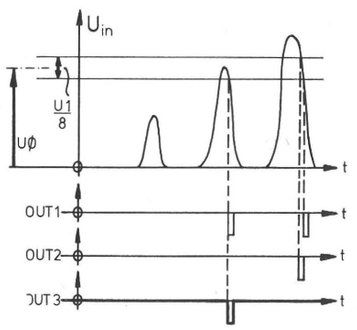

Fig. 2 Symmetrical Window Discriminator

DESCRIPTION OF THE BLOCK DIAGRAM

Generation of the Threshold Voltages

Two registers of 10 bits each are loaded, with the commands F(16)·A(Ø) and F(16)·A(1). Their outputs are converted into the analogue voltages −UØ and −U1 by two integrated-circuit DACs.

These voltages are converted into the actual thresholds for the discriminator circuit depending on the different modes of operation: In the mode: 'DID' (dual integral discriminator) the output voltages of the DACs are inverted by two summing amplifiers with unity gain. In 'SYD' (symmetrical window discriminator) the thresholds UØ + U1/16 and UØ − U1/16 respectively are generated by driving the operational amplifiers in two different configurations: the first amplifier works as a summing amplifier and the second as a differential one.

Operation Mode Register

The relay REL 1 is set to the appropriate position by loading two bits of the operation mode register. Two of the possible four combinations of these bits result in an inhibit, i.e., no output pulses are generated.

A third bit in this register drives another relay for selecting one of the two imputs provided for analogue input voltages, of max. amplitude −1 V or +5 V.

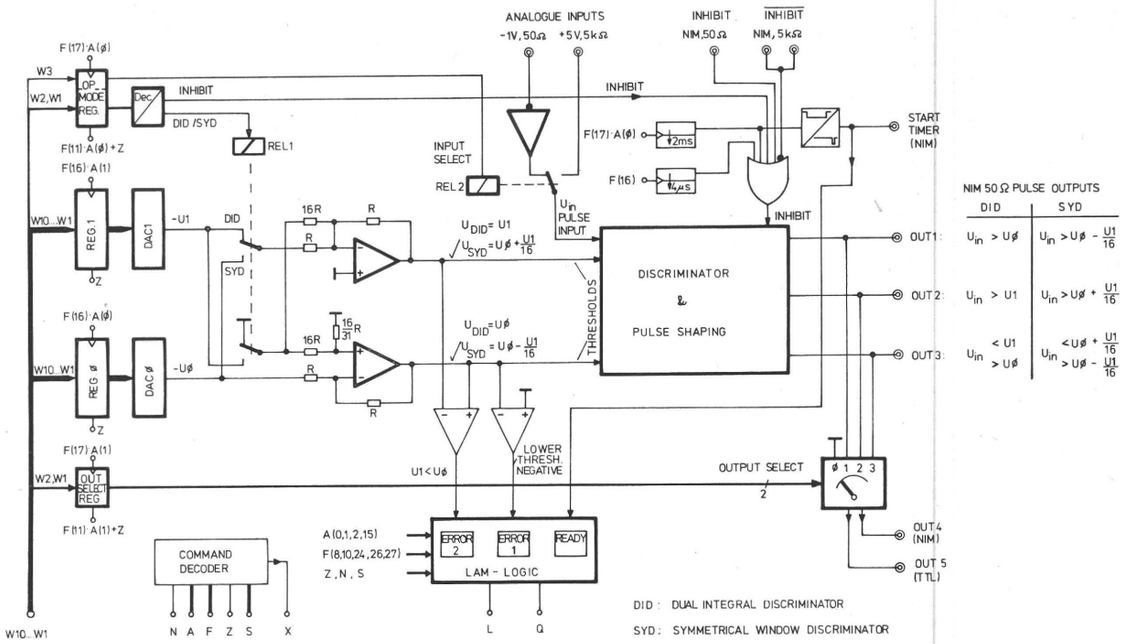

Fig. 3 Block Diagram of the CAMAC Differential Discriminator

Output Select Register

Although up to three scalers or other units may be connected simultaneously to the outputs Out 1 to Out 3 it is generally sufficient to have one scaler connected to output 4, the desired output signal being selected by an internal multiplexer. The position of this MUX is controlled by the 2-bit Output Select Register. In the condition (O, O) no output signals are generated at Out 4. This feature may be used for software 'gating'.

LAM — Logic

Three LAM Sources are provided:

- After selecting the mode of operation and the appropriate input a 'Ready' LAM indicates that the contact bounce time is over and the discriminator is ready for use.
- A 'Lower Threshold Negative' LAM is generated if in the symmetrical window discriminator mode U1/16 is greater than Uø i.e. the lower threshold has become negative.
- In the dual integral discriminator mode, the condition 'U1 < Uø' leads to an Error LAM. This LAM may be disabled if the window output is not in use, so that U1 < Uø is permitted.

APPLICATIONS

At present, some of these discriminators are used in the nuclear medicine department of the Rudolf-Virchow-Hospital in Berlin in a project 'CAMAC' in Medicine'. Measuring apparatus for well-known nuclear-medical diagnosis methods (renal and thyroid function diagnosis) is coupled to a Siemens S 301 computer via the CAMAC system.

The discriminators are used in conjunction with NaI scintillation crystals, pre-amplifiers and DDL-amplifiers, together with a CAMAC scaler-timer system, and are adjusted to the appropriate energy-ranges, depending on the nuclides that are employed.

Of course, the discriminators are applicable in many other cases of nuclear electronic measurements where amplitude discrimination is needed.

ACKNOWLEDGMENTS

Part of this development was done by C. Kordecki and D. Krohne.

2

A BRANCH HIGHWAY DRIVER FOR THE PDP-11 COMPUTER

by

B. Bricaud, J. Durruty, J.C. Faivre, J. Pain

Département de Physique Nucléaire, CEN Saclay, France

Received 8th July 1975

SUMMARY The CAMAC Branch Highway driver described in this paper controls up to seven crates, and transfers data via the UNIBUS of a PDP-11 computer. A 16-bit CAMAC operation needs only one computer instruction.

This paper describes a branch highway driver for the PDP 11/40-45 computers used in the 1 GeV spectrometer QD2 experiment at Saclay. The branch highway driver conforms to the EUR 4600 CAMAC Specification.

SOFTWARE

CNA definition.

The branch driver can control up to seven crates and needs 4k peripheral device addresses. Each crate uses 512 addresses (9 bits). The crate address C(Ø) is used for the specialised functions of the branch driver. The bits A_{13}-A_{17} define the first address of the 4k CAMAC area. The bit A_{00} is used to select some special functions (Fig. 1).

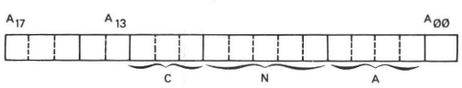

Fig. 1 Control Word for Branch Driver

CAMAC functions.

Each CAMAC function needs only one computer instruction for 16-bit data; it is defined by the type of data transfer and by the state of the A_{00} address bit.

A Data Buffer Register (DBR) allows the eight most-significant bits of the CAMAC data to be loaded or read, either by the computer or by the Read/Write CAMAC functions:

Read function F(Ø)
  MOV @ # CNA, X.
  MVB @ # DBR, Y (if 24-bit transfer).
Write function F(16)
  MOVB Y, @ # DBR (if 24-bit transfer).
  MOV X, @ # CNA.

CAMAC-to-CAMAC module transfer
  MOV @ # CNA_1, @ CNA_2 (24-bit transfer).
Command Functions
  MOVB # F, @ # CNA.
Fast Q Test ?
  TSTB @ # CNA+1: the state of the Q line is loaded into the N control bit of the PSW register. This instruction will be followed by a conditional branch instruction.

The F(1)-F(7) Read and F(17)-F(23) write functions are selected by three bits of the Data Buffer Register (D_{08}-D_{09}-D_{10}).

In the normal use, the DATIP phase of the instruction does not generate a CAMAC cycle; however, this phase can be enabled. With this possibility, all the PDP-11 instructions apply to the CAMAC modules.

Example: INC @ # CNA.

This instruction:

- reads the sixteen less-significant bits of the data;
- increments the data by one in the CPU;
- writes the result back into the module.

Interrupt System

The BD line is directly connected to the interrupt system of the PDP-11 computer; it can be enabled or disabled. A priority encoder CAMAC module allows coding of the L-lines (L_1-L_{23}).

BX Line

The BX line can generate an interrupt in the computer, independently of the BD interrupt.

MECHANICS

We use a CAMAC crate with a special Dataway construction: one Dataway for the unibus of the PDP-11 computer, and one Dataway for the Branch Highway signals.

It is possible to have two Branch Highway drivers in the same CAMAC crate.

NEWS

1st GENERAL ASSEMBLY OF THE ECA

The first general assembly of the European CAMAC Association (ECA) took place in Brussels, Sheraton Hotel on October 17th., following immediately after the 2nd International Symposium on CAMAC in Computer Applications. Around 100 persons were present.

The audience was welcomed by Chr. Layton, Director of the Directorate General Industry and Technology, Commission of the European Communities. Chr. Layton said that it was the right time to start ECA, and stated that the European Commission appreciated contacts with practical data processing people, because this fitted well into the Commissions work with a policy of data processing in Europe. Mr. Layton praised the independence of ECA, and promised all possibly support from CEC.

The opening speech was given by K. Zander, Chairman of the management board of the Interim Council of ECA, who expressed his faith in the future of CAMAC within medicine and industrial process control.

P. Gallice resumed the history of the Interim Council and its work with setting up statutes and standing orders. The ECA secretariat and working groups were also mentioned.

E. Rehse, Chairman of the ECA Medical Applications Working Group reported on the work of the group; this is especially related to intensive care in hospitals and automated clinical laboratories. Safety specifications are an important task of the future for this group.

E.G. Kingham outlined the work of the ECA Industrial Applications Working Group; this group is investigating the possibilities of CAMAC in industrial process control. Problems were defined and stated as a number of separate items; e.g., signal conditioning and cabling.

H. Meyer resumed the activities of the Information Working Group, which happens to be identical with the ESONE-IWG. Its main concern has been in the past the CAMAC-Bulletin for which it was planned to place greater weight in future on application reports and multilingual tutorial papers.

A.C. Peatfield, Chairman of the United Kingdom CAMAC Association reported on the work in this sizable regional group, while K.D. Müller explained that the "Deutsche Studiengruppe für Nuklearelektronik" is acting temporarily as a regional group in Germany and Austria.

D. Horelick, US-NIM Committee, described the work of the CAMAC Industrial Applications Group (CIAG) in USA.

The more formal part of the Assembly comprised an unanimous accept of the proposed statutes and standing orders and the election of members of the Council.

The first ordinary ECA council has 25 members as follows:

Council Members elected at the General Assembly (17th October 1975)

Austria
ATTWENGER, W., SGAE, 1082 Wien, Lenaugasse 10
CLAASSEN, D.P., AVL, 8020 Graz, Kleiststrasse 48

Belgium
STEYAERT, J., U.C.L.-SC 1-CH-Cyclotron 2, 1348 Louvain-La-Neuve

Denmark
CHRISTENSEN, P., Danish AEC, 4000 Roskilde, Res. Est. Risö

France
BOUET, L., Saphymo-Stel, 75013 Paris, 51 rue de l'amiral Mouchez
GALLICE, P., CEN de Saclay, 91190 Gif sur Yvette
OLIVIER, M., O.S.L., 06340 La Trinité, Avenue du Général de Gaulle
SERVENT, J.M., Compteurs Schlumberger 92222 Bagneux, B.P. n° 47

F.R. Germany
CREUTZBURG, U., Dornier System GmbH, 7990 Friedrichshafen, Postfach 648
HEIDEPRIEM, J., Gesamthochschule Wuppertal, 56 Wuppertal 1, Fuhlrottstrasse 1
OFFER, M., Siemens AG, 852 Erlangen 2, Postfach 325
ZANDER, K., H.M.I., 1 Berlin 39, Glienickerstrasse 100

Great Britain
BISBY, H., AERE Harwell 347.2, Harwell, Oxfordshire OX11 ORA
HILTON, K., GEC-Elliott Proc. Aut., Leicester New Parks LE 3 1UF
KINGHAM, E.G., CERL Control Comm. Div., Leatherhead, Surrey, Kelvin Avenue
PEATFIELD, A.C., Daresbury Lab., Daresbury, Warrington WA4 4AD

Italy
FORNACIARI, P., ENEL, 00198 Roma, V. Regina Margherita 137
RISPOLI, B., CNEN, 00198 Roma, V. Regina Margherita 125

Netherlands
OVERTOOM, A., Reactor Centrum Nederland, Westerduinweg 3, Petten

Switzerland
BESSE, L., SIN, Inst. f. Nuklearforschung, 5234 Villingen
LIEBENDORFER, H., Borer Electronics AG, 4500 Solothurn 2

Other Countries
HERMAN, M., Nucl. Equipm. Est. Polon, 00-901 Warszawa, Palace of Cult. & Science, Poland
HULTBERG, S., Res. Inst. f. Physics, 10405 Stockholm 50, Roslagsvägen 100 Sweden
LILJA, I., Valmet oy Rautpohja Works, 40101 Jyväskylä 10, P.O. 158 Finland
LUKACS, J., Zentralforschungsinstitut f. Physik, 1525 Budapest PF 49, Hungary

The General Assembly was rounded off with a general discussion about the future aims of ECA which has shown a great interest in the continuation of a periodical on CAMAC in some form.

Work with safety regulations, both in hospitals and in industrial plants, was recommended.

The Council was asked to publish a reference list of all existing CAMAC-applications.

In Hungary a 400 page handbook will appear shortly from H. Lukacs, while H.J. Stuckenberg of DESY, Hamburg, has recently generated his "CAMAC for Newcomers" in English and German. This kind of work was felt to be very important.

Pilot projects were considered valuable even when the applications were discontinued; in the latter case, a good deal of information was still disseminated.

ECA has many ties with other organizations and confirmed the interest in organizing presentations at topics oriented conferences, on applications where CAMAC could be of use.

SOFTWARE

COMAC — AN EDUCATIONAL PROGRAM FOR MANUAL CRATE CONTROL

by

B. Bjarland

Institute of Radiation Safety, Helsinki, Finland

Received 12th May 1975

SUMMARY A program in Nova assembler language allows CAMAC commands to be input from a Teletype. The L-pattern can be printed out on request. Fast and slow repetitive modes are provided. The program has been used for teaching and demonstrating CAMAC to students, and for module development and testing.

INTRODUCTION

When presenting CAMAC to students or people not previously familiar with the standard, a means of manually generating specific commands has proved most instructive. In an earlier issue of the Bulletin a hardware implemented Teletype-controlled crate controller has been described (1). Because of the inherent disadvantages of a hardware solution and because in most CAMAC environments there is a computer somewhere anyway, the software approach has been chosen. The features of the program developed are:

- all addressed and unaddressed commands can be generated;
- normal, repetitive, variable-incrementing and data-repetitive input modes;
- error messages on non-acceptable input;
- printout to a large extent self-explanatory;
- fast and slow cyclic repetitive modes;
- flexibility: absolute, relocatable binary or source versions are available, and can be used as subroutines called from Basic, etc.

The program has proved very useful also as a tool for module development and testing purposes.

DESCRIPTION

COMAC is implemented in extended assembler for the Nova computer, and occupies less than 3k words of core memory. The program can be run on any Nova type minicomputer connected to a CAMAC crate via the SEN 2023 CC crate controller. The standard teletypewriter (ASR 33) is used as input and output device. The program is self-starting and can be restarted at location 3 after power switch-offs for inserting or removing modules from crate.

OPERATION

Upon loading, COMAC first outputs a brief instruction for use, see fig. 1. Addressed CAMAC commands are input as six decimal integers, variables being separated by program-supplied dots for easier read-out. A non-integer input results in an error message. Input variables are checked against limits ($O \leq N \leq 23$, $O \leq A \leq 15$, $O \leq F \leq 31$) and an excess results in an error message. When the command has been verified as correct, different actions are taken depending on the type of command.

If the input command is found to be a write command, COMAC immediately requires that data for the W lines be input. For read commands, data is output after the CR key has been struck. The data representation format is octal.

Command input modes

In the normal input mode, addressed commands are input as previously described and executed by carriage return. Subsequent carriage returns will re-execute the last typed correct command. Write commands will be re-executed with the same data.

A partly repetitive mode can be used for write commands. Striking the line-feed key will cause the last executed write command to wait for data input. New data can then be supplied.

Striking the CR key on a write command data request will cause the command to be executed with the data last read or written, thus enabling data transfers between modules.

To facilitate module and crate testing routines, an incremental command input mode is provided. Typing N, A or F causes the corresponding command variable to be incremented and the updated command will be executed by cariage return. Write commands incremented in this way will request that new data be input.

Unaddressed commands

All the single-crate unaddressed commands can be generated. Typing Z generates the initialising command and C generates a clear operation. The inhibit signal can be set, reset and tested by typing IS, IR and IT, respectively. By default (after start and restart) the inhibit signal is reset.

Responses

By typing either X or Q the appropriate response can be selected for monitoring. When a command receives a logic '1' response it will be announced by a ring on the teletype bell and by a star appearing in the command line. By default the X response will be monitored.

Repetitive modes

Two cyclic repetitive modes are provided. The faster, which will repeat at 10kHz the last correct addressed command that has been input is entered by typing RF and the slower, with a repetition rate of 10Hz by typing RS. From both modes return to normal mode will occur on striking any key.

```
TYPE ADDRESSED COMMAND TO FORMAT
BELOW AND EXECUTE BY CARRIAGE RETURN.
COMMAND CAN BE REPEATED BY SUBSEQUENT
CR: S. USE LF IF DATA WILL BE CHANGED.
TO USE LAST DATA READ OR WRITTEN TYPE
OR ON W-REQUEST.
N, A OR F INCREMENTS THE CORRESPONDING
VARIABLE.
X OR Q SELECTS RESPONSE MONITORED BY*
Z AND C GENERATE CORRESPONDING UN-
ADDRESSED COMMANDS.
IS SETS, TR RESETS AND IT TESTS INHIBIT SIGNAL.
RS OR FR SETS AND ANY KEY RESETS REPEAT
MODE.
L WILL OUTPUT L PATTERN.

  FF.NN.AA DATA
Q  RESPONSE MONITORED
  00.21.22 ARGUMENT OUT OF RANGE
  00.21.02* R: 00000123
  16.03.00 W: 00000123*
  26.03.03*
L  PATTERN: 00000010
X  RESPONSE MONITORED
  16.03.00 W: 00000123*
A16.03.01 W: 00000123*
A16.03.02 W: 00000123
```

Fig. 1 Example of communication with COMAC. User inputs underlined.

L Pattern

The L pattern of the crate will be output on typing L provided that LAM's are enabled.

AN EXAMPLE

A sample printout from a session with COMAC is shown in Fig. 1. Inputs from the student are underlined.

With Q response monitored, data is read from a word generator at N = 21. The command, first erroneously input, is corrected after an error message. The data that has been read is then transferred to a step moter driver at N = 3. After enabling LAM from this module the L-pattern of the crate is requested and output.

The X-response is then selected for monitoring and the step motor driver is investigated using the incremental input mode. As A = 2 produces no response the module apparently has two registers that can be written into, at subadresses A = 0 and A = 1.

REFERENCE

1. D. Kollbach, A teletype-controlled CAMAC Branch Driver. *CAMAC Bulletin 9/74.*

NEWS

CAMAC APPLICATIONS WORKING GROUPS

ECA INDUSTRIAL WORKING GROUP

Chairman: K. Hilton, CEC-Elliott Process Automation Ltd., England.

The Industrial Working Group met in Brussels in June 1975 to examine the response to the Bulletin requests for views and comments, replies to the letter which had been separately circulated and to consider a number of detail topics.

These were:

- recommendations for plant termination and connections to CAMAC modules
- recommendations made by the ESONE Analog working group
- consideration of the possibilities of holding meetings and Seminars.

The response to the letter and the Bulletin requests was less than had been hoped. There were some useful points made by the people and organisations who did reply, but the extent of the response was not sufficiently broad to permit any significant conclusion to be drawn.

Methods of connection of CAMAC modules to plant were discussed at some length and two lines of thought emerged. Broader consideration is necessary before these lines of thought can be turned into recommendations. The Working Group would be grateful for views and opinions from users in particular on this point.

The Group's view on the Analogue Working Group's recommendation was that a basis had been laid in that document but that for industrial applications, some specific areas needed to be considered and clarified. This will be the subject of further discussion.

The Group thought that there would be value in organising meetings or seminars, probably on a one or two country basis, rather than on a true European basis at which common problems and experiences could be exchanged.

IDEAS AND TECHNIQUES

SYSTEM APPROACHES TO ANALOGUE MEASUREMENTS

by

H. Liebendörfer and C. Manning

Borer Electronics AG, Solothurn, Switzerland

Received 8th July 1975

SUMMARY CAMAC is essentially a digital system concept, and therefore digital-analogue converters (DACs) are needed to handle analogue outputs, and analogue-digital converters (ADCs) for analogue inputs. Because ADCs are rather complex instruments this paper is intended to clarify some questions that may arise.

PRACTICAL APPROACHES

ADC's have to be complex principally because noise and other interference signals are always present at their inputs. Special procedures have to be used to ensure that only the wanted signal is treated.

A particularly effective technique is to arrange the input circuitry in a differential manner i.e. symmetrically about earth and, so far as possible, free of it. Measurements down to a few micro-volts can be realised if the whole of the analogue circuitry is floating free from earth. Connection to the CAMAC digital output part of the instrument can be made, for example, optically using opto-isolators. In addition, the ADC should operate on a dual-slope principle and integrate incoming signals over a period of 20ms (16,66ms for America) which eliminates mains pick-up. The addition of one or more relay multiplexers which operate in automatic synchronism with the ADC permits up to about 30 measurements per second to be made, provided that no change of range has to be made between one measurement and another.

Quite different conditions-apply, however, if a large number of measurements have to be made in a very short period of time. Switch-over times of relays in multiplexers and integration time in the ADC cannot be tolerated. High sensitivity ADC inputs are also not possible, so that the analogue signal to be measured should be of the order of volts, even if this means prior amplification (preferably at the signal source).

A number of high speed ADC's offering a choice of resolution are currently available.

They are ideally suited for jobs where, for example, either a large number of values must be measured quickly or a large number of spot-checks on a single constantly varying value must be made for computer analysis (especially of transient events).

Of special interest is the combination of one of the fast ADC's with one or more fast multiplexers. These instruments are normally so closely matched to one another that only the very minimum of time is lost between individual measurements. A sample and hold circuit in the input of an ADC permits a number of modes of operation which are described briefly below.

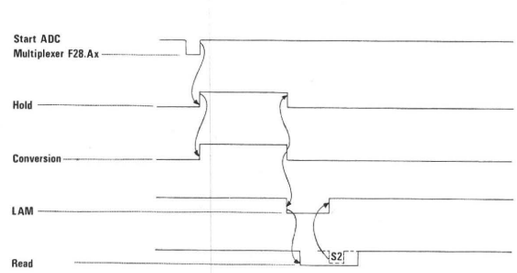

Fig. 1 Single Conversion Sequence.

PROGRAM-CONTROLLED SINGLE MEASUREMENT

Fig. 1 shows the basic operation from which it can be seen that the various actions follow each other logically and consecutively. The cycle can be started by a front panel signal or by the command $F(25)\cdot A(\emptyset)$ and ends with the read-out command $F(\emptyset)\cdot A(\emptyset)$. This mode of operation can also be used when one or more multiplexers are in use and individual channels must be selected under program control.

SEQUENTIAL MEASUREMENT

An arbitrary number of analogue values can be examined sequentially by putting an ADC-multiplexer combination into a Scan-mode. This mode is typically effected by enabling a Scan flip-flop in the ADC after which the operation can follow the sequence shown in the time diagram, Fig. 2.

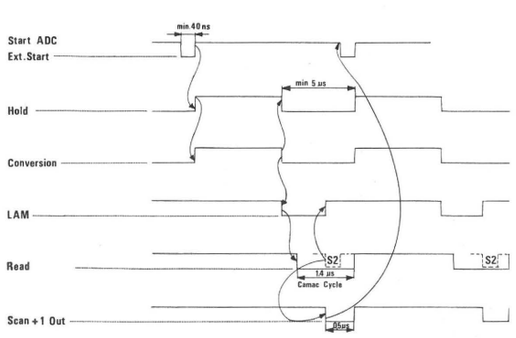

Fig. 2 Conversion Sequence with an External Multiplexer.

Once the cycle is begun (either by a CAMAC command or by an external signal) the operation is continuous and automatic without any further intervention by the computer. One analogue channel after another is selected, the value digitized and the

completion of the conversion notified by means of a LAM. 'Scan+1' signals produced by the ADC cause a multiplexer to step from one channel to next until it reaches the multiplexer's last channel. If a further Multiplexer follows, the 'Scan+1' signal passes to channel 1 of Multiplexer 2 and so on until no more channels are left, when a LAM is given. The first and last channels in a sequence can be chosen by software.

The computer can use the read command F(Ø)·A(3) for this mode of operation, for example. Each word read out needs about 25 μs plus the time taken by the computer for the LAM-handling and the read-out cycle. Together, this means normally about 70 μs (depends on software conditions) or about 14,000 words or measurements per second.

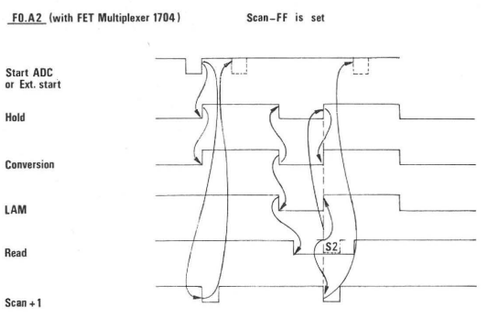

Fig. 3 High Speed Conversion showing how Conversion and Channel Switching can be overlapped by using Sample and Hold.

HIGHEST DATA RATE

The highest data rate is obtained when the sample-and-hold feature is brought even more into play. Using this feature it is possible for the multiplexer to progress to its next channel while the ADC is still busy converting a previously obtained value. The useful overlapping so obtained can be seen in the time diagram, Fig. 3. Full use of the time gained can only be effectively realized, however, when the ADC has an even shorter conversion time. Such super-fast ADC's are available having conversion times of as little as 5 μs (10-bit) or 7 μs (12-bit).

The advantages possible will be fully exploited, for example, by CERN when the new accelerator currently under construction goes into operation. Here, the data collected from the many installations will be handled in a DMA mode so that every 20 μs a value will be selected, digitized (12-bit) and stored in the computer, i.e. 50,000 measurements per second. The quantity of data that will come from the new system will be so great that no other mode of operation would be possible.

When measurements on a varying analogue value or signal are being made it is important that, besides obtaining sufficiently accurate absolute values, sufficient points should be obtained from fast or steep parts to be meaningful. With the operation mode described abouve (but without a multiplexer) it is possible to obtain up to 20 measurement points on each cycle of a signal having a frequency of 3 kHz. The actual number of points obtained will, however, be greatly influenced by the type and organisation of the computer.

NEWS

VIII INTERNATIONAL SYMPOSIUM ON NUCLEAR ELECTRONICS

Dubna — USSR, 24-29 June 1975

150 participants attended this Symposium, organized by the Joint Institute for Nuclear Research — Dubna — USSR, where 85 papers were presented, the majority of which dealing with CAMAC. The Vector System, used in Serpukhov, which is a metricated adaptation of the CAMAC Standard, due to the absence of inch machine tools in USSR, was also presented.

The recent development of CAMAC modules and equipments in the Eastern Countries, in the field of nuclear research was reviewed and the importance of this was demonstrated by the papers presented as well as by the small exhibition.

Five sessions were held:

— Modules for analogue and multi-channel measurements;
— Controllers and microprocessors;
— Visual data presentation and software;
— Electronic systems and installations for nuclear physics research.

The IML language was presented by M. KUBITZ of HMI, Berlin. A noteworthy point of interest is that a CAMAC crate is now on display at the permanent 'economical' Exhibition Park in Moscow.

NEW PRODUCTS

DATA MODULES (I/O Transfers and Processing)

Digital Serial Input Modules

Ref. No. 14.0101

Display Scaler

The single-width CAMAC Scaler, Model C-SD-24 is a presettable binary scaler with decimal readout. The scaler operates from D.C. up to 50MHz with a fixed dead-time of 20nsec.

Internally it contains two scalers (24-bit binary and 7 1/2 digits BCD) with parallel operation of both scalers for all statistical conditions even during an overflow of the binary scaler. Readout of the binary scaler is via the dataway, with the BCD scaler on the front-panel LED display.

For preset operation, the binary scaler starts counting from the preset number whilst the BCD scaler starts always from Zero displaying real-time counts. The module may also be used in the preset mode as a timer driving other slave scalers (using the rear panel inhibit signals). The front panel input 'GATE' may be used in the preset mode as a timer driving other slave scalers (using the rear panel inhibit signals). The front-panel input 'GATE' may be used in the inhibit or gate mode, controlled internally by the control status register via the dataway. Both front-panel inputs (SIGNAL and GATE) may be operated in the terminated or unterminated mode.

Ref. Wenzel Elektronik

Ref. No. 14.0102

Incremental Encoder Input

The encoder, Model IE, accepts two quadrature signals from a position encoder. It determines whether the signals are clockwise or counter-clockwise and counts them in a 24-bit up-down counter. The counter may also be preset to a predetermined number and when that number is reached an interrupt will be generated. This feature could be used both for position selection or as a limit condition. A gate input is also provided to disable the counter input.

Ref. Joerger Enterprises, Inc.

Digital Parallel Input Modules

Ref. No. 14.0103

Dual Input Register

The single-width module, type C-IC-48 is for processing a maximum of 48 inputs from one or more external instruments. The module contains two separate 24-bit input registers. The logic level for each of the 24 bits can be preselected via internal links.

The data flow timing routine between the CAMAC dataway, the module and external instruments is controlled by signals 'T_{in} and T_{out}' together with 'STATUS and COMMAND'.

The layout is to the EUR 4100e standard, unterminated signals are negative.

Ref. Wenzel Elektronik

Ref. No. 14.0104

Quad 24-Bit Input Register

This input register, Model QIR, is a four-channel input register packaged in a single-width CAMAC module. Each channel contains 24 bits. Data may be loaded continuously, strobed or single shot. This last method ensures that data cannot be lost by inhibiting a data update until the previous data has been read by the system. Data may also be loaded efficiently using a Handshake Mode Made up of the strobe input and the acknowledge output. Data is clocked into the registers approximately 2µsec after the leading edge of the strobe so that data and the strobe may be transmitted at the same time and loaded correctly. When a register is clocked it's LAM flip-flop is set and an acknowledge signal is generated to indicate that the data has been loaded. When that channel's data has been read, the LAM-flip-flop is reset and the acknowledge signal returns to zero indicating that new data can be accepted. To ensure error-free readout of data, the clocks are inhibited when the module is being read so that the data cannot change.

Ref. Joerger Enterprises, Inc.

Ref. No. 14.0105

Interrupt Request Register

This module Type 9608, embodies 8 interrupt-request channels. Each channel comprises a Status Buffer register, Status register, Mask register, and Request. Status and Mask information can be selectively set or cleared and Status, Mask and Request can be read via the dataway at the ESONE recommended sub-addresses.

LAM can be enabled or disabled by command. The Status Buffer ensures that no input event is lost while the module is being addressed. Pulse or level inputs are accepted and provision is made for input integration if required.

A front-panel output conveys the L signal for connection to further interrupt-request modules.

The state of the Mask register, L requests and Dataway L are displayed by front-panel indicators together with a module-addressed indicator.

Input levels are never lost even during initialization and, in the event of unsuccessful service routine, are re-entered, a major requirement for SAFETY INTERLOCKS.

Level or pulse inputs are not lost during Read and Clear operations.

'Time Out' option to re-enter current data. This can save software generation of Read-Clear delay and prevent Status lockout due to software error.

Full sub-address structure.

Visual indication of Mask, L requests, and LAM.

Output LAM to enable cascading of units.

Economy to allow grouping of interrupts at different priority levels.

Ref. Nuclear Enterprises, Inc.

Digital Output Modules

Ref. No. 14.0106

Watchdog Timer

This Timer, Model WT, is a single-width CAMAC module. It monitors system activity and generates an alarm if there is a system failure. The unit must be strobed periodically by a dataway command, N.F25.AO. Timing periods can be set to be 100 msec, 1 sec, 10 sec or 1 minute. If a strobe does not come within the specified period the module will 'time-out'. At this time it will generate a dataway inhibit signal, generate an audio alarm and provide a contact closure for use externally. Redundancy is used extensively to improve the module's reliability.

Ref. Joerger Enterprises, Inc.

Ref. No. 14.0107

Quad 24-Bit Output Register

This output register, Model QOR, is a four-channel output register packaged in a single-width CAMAC module. Each channel contains 24 bits. Error-free data transfer at maximum speed is provided by the use of a handshake mode in conjunction with the interrupt line L. Handshake is accomplished by generating a 'data ready' signal when that channel's register is loaded. In response to this, the output device would return a 'busy' signal indicating that it acknowledges 'data ready' and is processing the information. Upon receipt of the 'busy' signal, 'data ready' is reset. While the busy line is down, that channel will not be able to update and so output data stability is insured. If an update command is received at this time, it will return a Q = 0 response. When the busy line comes up, indicating the device is finished with the data, the LAM flip-flop is set. If the unit is enabled, it will generate an L signal which indicates to the controller that new data can be accepted. If the handshake logic is not required, then data may be outputed at the maximum CAMAC data-rate. An update pulse is also generated to indicate when a channel has been overwritten.

Output polarity selection is available as an option. This allows the polarity of the data to be inverted by the use of solder links or under program control. This is accomplished by allowing bit 24 (or 16) to select the polarity of the output data.

Ref. Joerger Enterprises, Inc.

Digital I/O, Peripheral and Instrumentation Interfacing Modules

Ref. No. 14.0108

X-Y Recorder driver

This single-width module Type XY2074 is designed to drive any graphic recorder from the CAMAC dataway; however, in its basic form it is immediately compatible with the Hewlett Packard 7004B.

Several working modes are available, depending on the contents of a two-bit control register.

Mode 0: X-Y point-by-point plot.
Data is loaded into the X-Y registers alternatively.

Mode 1: Y versus X diagrams, coarse X.
The load command always puts data into the Y-register, increments X by 16 elementary steps and unblanks the spot.

Mode 2: Y versus X, fine X.
Same as mode 1, but the X scale has the full 1024 point resolution. Any single-valued X(Y) functional relationship can be represented with full resolution.

Another control register contains 'pen-down' information, and three delay values are provided.

Ref. SEN Electronique

Ref. No. 14.0109

On/Off-Controller

The Model C-PC-16 On/Off-Controller is a single-width module capable of controlling 16 external devices in an ON-OFF manner. Each channel is independent and may be selectively set (ON) or reset (OFF) by using two separate commands. For each channel there is a 'STATUS' signal. The output signal is maintained until the 'STATUS' signal confirms that the command has been executed. Should a channel fail to respond within one second a 'LAM' flag will be set.

Each channel has five lines allocated to it at the front panel connector. These are as follows: ON and OFF commands, common return, STATUS positive and negative.

To avoid ground loop problems the STATUS input signals are optically isolated.

Ref. Wenzel Elektronik

Digital Handling and Processing Modules

Ref. No. 14.0110

Dual TTL Fanout

This fan-out unit, Model FT, has two channels packaged in a single-width CAMAC module. Each channel has two 'OR' ed' inputs, four normal

outputs and one complement output. Output polarity may be inverted manually or optionally under program control. Outputs may also be individually enabled under program control. Programming is accomplished by a control register that may be selectively set, reset or overwritten, thus offering a great degree of flexibility. Each output can sink 50 mA. 100 mA sink capability is available as an option.

Ref. Joerger Enterprises, Inc.

Ref. No. 14.0111

Hex Converters

These Models CT/N and CN/T are six-channel converters in a single-width CAMAC module. Two channels have both normal and complement outputs, the remaining four having normal outputs only. Polarity of all the outputs may be inverted either manually, by a toggle switch, or optionally under program control. Each channel may also be enabled and disabled under program control. This is accomplished with a control register that may be selectively set, reset, overwritten, and read out. These modules therefore not only convert signals but select polarity and gate the signals on or off.

Model CT/N Hex TTL to NIM Converter
Model CN/T Hex NIM to TTL Converter

Ref. Joerger Enterprises, Inc.

Analogue Modules

Ref. No. 14.0112

Isolated A/D Converter

This differential input 12 bit A/D converter, Model IADC 2069, is fitted in a double-width standard CAMAC module, and is intended for operation with high common-mode voltages. For this reason, both the converter, which is of the successive approximations type, and the power supply are completely isolated from the rest of the module and CAMAC system. The convert instruction can be given by a CAMAC dataway command or by an internal TTL signal, and a register permits a digital offset to be added to the onversion value.

A connector is fitted on the rear panel which provides for a hook-up between the 2069 and the SEN Digital Window Discriminator (DWD 2046): when operated in this way, unwanted values are rejected before they can take up valuable core memory, and computer time is saved by the use of the DWD's block transfer capability.

The input amplifiers and the ADC chip are fully insulated up to ±400 V with respect to chassis and logic ground. However, the input signal common mode should not exceed ±300 V.

Ref. SEN Electronique

SYSTEM CONTROL

(Computer Couplers, Controllers and Related Equipment)

Interfaces/Drivers and Controllers

Ref. No. 14.0201

Branch Highway Controller

The 20368 Autonomous Branch Highway Controller provides an interface between a CTL Modular One System and the CAMAC Branch Highway and allows up to four simultaneous, high speed block transfers between CAMAC modules and computer store.

It is a 19-inch rack-mounting unit with interface links to the processor and one or two store modules. One group of processor commands enables Branch Highway transfers to be set up and initiated singly. A second group of commands enables an autonomous transfer unit (ATU) to be set up to independently transfer data between a specified data buffer in store and the Branch Highway. The ATU uses automatic double buffering in store to allow large blocks of data to be transferred at high speed with minimal system loading. A processor interrupt is generated when buffer switching occurs. Transfers may be triggered from an external source or allowed to free run. Up to four ATU's may be fitted to the controller and function independently of each other and of the processor interface which may still be used to initiate single transfers.

Ref. CTL (Computer Technology Limited)

Ref. No. 14.0202

Single-Crate I/O Controller

The Model CA-11-FP provides connects a CAMAC crate to a PDP-11 family computer for programme controlled I/O transfers. It consists of a double-width CAMAC unit and connects directly to the PDP-11 UNIBUS via its front panel connector. Power for the Controller may be supplied by an external power supply, thereby providing for power-fail detection. On the Controllers' rear panel, a DMA connector is mounted to allow connection of an optional CA-11-FN Controller for DMA transfers.

Only six UNIBUS addresses are used by the Controller including a NAF register, a LAM register and a 24-bit Buffer register. LAM interrupts may be controlled using a single or variable vector mode. The latter assigns its own interrupt vector address for each LAM including priority generation, at which the vector addresses are programmable, using a vector offset register. During a 24-bit Data Transfer, interrupts are automatically inhibited.

Any number of CA-11-FP Controllers may be connected to the UNIBUS. The device address is easily selectable by the user through a switch in the Controller.

Ref. Digital Equipment G.M.B.H.

PAPER ABSTRACTS TRANSLATIONS

Microprocessors
Hans-Joachim Stuckenberg

Zusammenfassung

Mikroprozessoren bilden bei zahlreichen Steuerfunktionen interessante Alternativlösungen zur Festverdrahtetenlogik. In diesem Beitrag werden Mikroprozessoren und ihre Hardware- und Solftwareprobleme behandelt.

Résumé

Les microprocesseurs constituent une alternative intéressante des logiques câblées pour un grand nombre de fonctions de contrôle-commande. Cet article décrit des microprocesseurs et expose les problèmes de matériel et de logiciel qui leur sont liés.

Riassunto

I microcalcolatori rappresentano un'interessante alternativa alle logica hardware per molte funzioni di controllo. Il presente studio descrive i microcalcolatori ed i relativi problemi di hardware e software.

Samenvatting

Microprocessors vormen een interessant alternatief voor veel hard-wired logische stuurschakelingen. In dit artikel wordt een beschrijving gegeven van deze microprocessors en de hard- en software problemen die hiermee verband houden.

Резюме

Микропроцессоры являются интересной альтернативой жесткой логики во многих розличных Функциях управления. В статии описаны микропроцессоры и связанные с ними проблемы оборудования и програмирования.

Autonomous crate controller (JCAM 10) with Intel 8080 microprocessor
P. Gallice and M. Mathis

Zusammenfassung

Die autonome Rahmensteuerung JCAM-10 ist für einen Mikroprozessor Intel 8080 entwickelt worden und wird mit einem 5k-RAM- und 4k-REPROM-Speicher betrieben. Die Datenübertragung zwischen den CAMAC-Modulen und dem Speicher ist hinsichtlich software und Durchführungszeit optimiert. Die JCAM 10 ist ein Mikrocomputer, dessen periphere Einheiten alle im Handel erhältliche CAMAC-Module sind.

Résumé

Le contrôleur de châssis autonome JCAM est conçu à partir d'un microprocesseur Intel 8080 associé à une mémoire vive (RAM) de 5k octets et une mémoire REPROM de 4k octets. Le transfert des données entre les tiroirs CAMAC et la mémoire est optimalisé tant du point de vue du logiciel que du temps d'exécution. Le JCAM 10 est un micro-ordinateur dont les périphériques sont tous les tiroirs CAMAC commercialisés.

Riassunto

Il modulo di controllo autonomo JCAM-10 è progettato per un microcalcolatore Intel 8080 ed è impiegato con una memoria RAM a 5k e REPROM a 4k. I trasferimenti di dati fra i moduli CAMAC e la memoria sono ottimizzati per quanto riguarda il software ed il tempo d'esecuzione. L'JCAM-10 è un microcalcolatore che utilizza como periferiche tutti i moduli CAMAC esistenti in commercio.

Samenvatting

De zelfstandige crate controller JCAM-10 bestaat uit een INTEL 8080 microprocessor en wordt gebruikt in combinatie met een 5k RAM en 4k REPROM geheugen. De gegevensoverdracht tussen CAMAC-modules en geheugen is zowel uit het oogpunt van de software als van de uitvoeringstijd aanzienlijk verbeterd. De JCAM-10 is een microcomputer waarop alle op de markt zijnde CAMAC-modules als periferie-apparaten kunnen worden aangesloten.

Резюме

Автономный контроллер крейта JCAM-10 разработан с микропроцессором Intel 8080 и применен вместе с памятю 5 к РАМ и 4 к ПРОМ. Передача данных между блоками и памятью оптимизирована с точки зрения программирования и время исполнения. JCAM-10 это микро-ЭВМ которой периферииами являются все доступные модули CAMAC.

The MIK-X Autonomous crate controller
Douglas L. Abbott

Zusammenfassung

Die besonderen Eigenschaften der autonomen Rahmensteuerung der Standard Engineering Corporation werden beschrieben. Es handelt sich um die erste im Handel erhältliche CAMAC-Rahmensteuerung auf Mikroprozessorbasis.

Résumé

Description des principales caractéristiques du contrôleur de châssis autonome MIK-X de Standard Engineering Corporation. Ce contrôleur de châssis CAMAC est le premier contrôleur à microprocesseur existant sur le marché.

Riassunto

Si descrivono le caratteristiche essenziali del modulo di controllo autonomo MIK-X prodotto dalla Standard Engineering Corporation. Si tratat del primo modulo di controllo CAMAC, a microcalcolatore, messo in commercio.

Samenvatting

In dit artikel worden de uitstekende eigenschappen van de zelfstandige crate controller MIK-X van Standard Engineering Corporation beschreven. Dit is de eerste CAMAC-crate-controller met microprocessor die op commerciële schaal verkrijgbaar is.

Резюме

Описаные отличительные достоинства автономного контроллера крейта MIK-X фирмы Standard Engineering Corporation. Он является первым торгово доступным контроллером базированным на микропроцессоре.

Auxiliary/Master microprocessor CAMAC crate controller
E. J. Barsotti

Zusammenfassung

Diese CAMAC-Einheit auf Mikroprozessorbasis kann als Rahmensteuerung oder Hilfssteuerung eingesetzt werden. Sie ist für das serielle CAMAC-Steuerungssystem des Strahlungsweges für Experimente im Fermilaboratorium für Anwendungen mit örtlichem Computerbedarf im CAMAC-Rahmen entwickelt worden.

Résumé

Cette unité CAMAC comprenant un microprocesseur peut être utilisée comme contrôleur de châssis ou contrôleur auxiliaire. Elle a été mise au point pour le système de contrôle CAMAC série du faisceau expérimental du laboratoire Fermi, pour les applications qui requièrent l'autonomie locale dans les châssis CAMAC.

Riassunto

Questa unità CAMAC, basata su un microcalcolatore, puo essere impiegata quale modulo di controllo del contenitore o modulo di controllo. ausiliario. É stato sviluppato per il sistema di controllo seriale CAMAC della traiettoria del fascio sperimentale del Fermilab, per applicazioni che richiedono una intelligenza locale nei contenitori CAMAC.

Samenvatting

Deze CAMAC crate controller met microprocessor werd ontwikkeld voor het bij het Fermilab gebruikte CAMAC-seriesysteem voor de besturing van experimenten waarbij "lokale intelligentie" in de CAMAC-rekken vereist is.

Резюме

Этот блок CAMAC содержащий микропроцессор может быть использован как контроллер крейта или вспомагательный контроллер. Он разработан для посследовательной системы CAMAC управляющей линей экспериментального пучка в применениях требующих локальной интеллигентности в крейтах CAMAC.

CAMOPS — CAMAC modular processor system
D. Kollbach and V. Schmidt

Zusammenfassung

Eine mit Mikroprozessor gesteuerte und durch eine private Sammelleitung verbundene Serie von CAMAC-Module ist für den Einsatz als "intelligente" Hardware entwickelt worden.

Résumé

Un ensemble de tiroirs CAMAC, commandé par un microprocesseur, relié à un bus spécialisé a été développé pour être utilisé comme matériel "intelligent".

Riassunto

Una serie di moduli CAMAC, controllati da un microcalcolatore e collegati da una linea omnibus privata è stata sviluppato per l'impiego quale hardware "intelligente".

Samenvatting

Een door een microprocessor gestuurde serie CAMAC-modules, verbonden door een afzonderlijke IO-Bus, werd ontwikkeld voor toepassing als "intelligente" hardware.

Резюме

Разработан набор блоков CAMAC управляемых микропроцессорами и соеденных отдельными шинами. Они используются как интеллигентное оборудование.

CMC 8080: A CAMAC crate controller with INTEL 8080 microprocessor

E. Schöberl

Zusammenfassung

Diese "intelligente" CAMAC-Rahmensteuerung umfaßt einen Mikroprozessor (INTEL 8080 CPU) sowie einen Speicher mit wahlfreiem Zugriff (RAM) und einen programmierbaren und UV-löschbaren Lese-Spreicher (PROM). Sie ist mit einer seriellen Schnittstelle ausgestattet, mit der sie an einen Fernschreiber oder Minicomputer angeschlossen werden kann.

Résumé

Ce contrôleur de châssis CAMAC "autonome" est équipé d'un microprocesseur (INTEL 8080 CPU) d'une mémoire vive (RAM) et d'une mémoire morte reprogrammable effaçable par UV (REPROM). Il est équipé d'une interface série grâce à laquelle il peut être relié à une télétype ou à un mini-ordinateur.

Riassunto

Questo modulo di controllo "intelligente" CAMAC comprende un microcalcolatore (Unità Centrale INTEL 8080), una RAM (memoria ad accesso casuale) ed una PROM programmabile e cancellabile a UV. Esso dispone di un'interfaccia seriale mediante la quale puo essere collegato con una telescrivente o con un minicalcolatore.

Samenvatting

Deze "intelligente" CAMAC crate controller bestaat uit een microprocessor (INTEL 8080 CPU), een Random Access Memory (RAM) en een programmeerbaar en uitwisbaar Read Only-Memory (PROM). Door middel van een serial interface kan de controller rechtstreeks aan een teletype of minicomputer worden gekoppeld.

Резюме

В этом интеллигентном контролиере крейта находится микропроцессор Intel 8080, оперативные памяти РАМ и программированные памяти ПРОМ сбрасываемые ультрафиолетом. Он снабжен посс едовательном интерфейсом для телетайпа или мини-ЭВМ.

Fast autonomous crate controller

I. Bals, M. Caprini, B. Goran

Zusammenfassung

Diese CAMAC-Rahmensteuerung umfaßt einen aus SSI- und MSI-Komponenten gebauten Prozessor. Sie ist für kleine Einrahmensysteme bestimmt, für die ein Rechner zu teuer und ein LSI-Mikroprozessor zu langsam wäre.

Résumé

Ce contrôleur de châssis CAMAC est équipé d'un processeur construit à partir de composants SSI et MSI. Il est destiné à de petits systèmes monochâssis dans lesquels un ordinateur serait trop onéreux et un microprocesseur LSI trop lent.

Riassunto

Questo modulo di controllo CAMAC contiene un calcolatore costituito da componenti SSI ed MSI. E previsto per piccoli sistemi monocontenitore, per i quali un calcolatore sarebbe troppo caro ed un microcalcolatore LSI troppo lento.

Samenvatting

Deze CAMAC crate controller bevat een processor bestaande uit SSI en MSI componenten en is bestemd voor kleine single-crate systemen waarbij het gebruik van een computer te duur is en een LSI-microprocessor een te geringe snelheid heeft.

Резюме

Этот контроллер крейта CAMAC содержит процессор построен из интегральных схем малой и средней степени интеграции. Он предназначен для небозьших одно-креймных систем, где ЭВМ является слишком дорогим устройством, а микропроцессор большой степени интеграции медленным.

A fast data acquisition path based on a CAMAC memory system

R. Klesse and A. Axmann

Zusammenfassung

Mit diesem Datenerfassungssystem auf CAMAC-Basis können hohe Übertragungsgeschwindigkeiten bis zu 500kHz verarbeitet werden; es entspricht auch der anforderung einer "on-line"-Datenverdichtung. Die Anwendung einer neuen MOS-Technologie ermöglicht den einsatz eines Speichers für 4k × 16-bit-Wörter in einem Modul (Brete: eine Einheit) in einer vernünftigen Preislage. Die "on-line"-Datenverdichtung beschränkt die für die Mehrkanalanalyse erforderliche Speicherkapazität auf ein Minimum.

Résumé

Les taux élevés de données — jusqu'à 500 kHz — sont traités par ce système d'acquisition CAMAC, qui répond en outre à un besoin de réduction des données en ligne. Une mémoire de 4k × 16 bit, utilisant la nouvelle technologie MOS, a été réalisée dans un tiroir une unité pour un prix raisonnable. La réduction des données en ligne permet de diminuer le volume de mémoire nécessaire à l'analyse multi-canal.

Riassunto

Questo sistema per l'acquisizione di dati basato sul CAMAC tratta dati a frequenze elevate (fino a 500 kHz) e soddisfa inoltre alle esigenze della riduzione dei dati in linea. Impiegando la nuova tecnologia MOS si è riusciti ad introdurre una memoria da 4k parole da 16 bit in un modulo di larghezza unitaria e di prezzo ragionevole. La riduzione dei dati in linea riduce al minimo lo spazio di memoria necessario per un'analisi multicanale.

Samenvatting

Met dit uit CAMAC-modules bestaande data-acquisitiesysteem zijn hoge transfersnelheden tot 500 kHz mogelijk. Het systeem zorgt bovendien voor on-line gegevensreductie. Door toepassing van nieuwe MOS-technieken is in een 1/25 CAMAC-module een redelijk goedkoop geheugen van 4k × 16-bit woorden opgebouwd.

Резюме

Большие скорости передачи данных порядка 500 kHz достигаются в описываемой системе сбора данных и редукции он-лайн. Используя технологию МОС получают в блоке одиночной ширины 16-разрядную память 4 к по разумной цене. Предварительная обработка уменьшает обём памяти в много-канальном анализе.

CAMAC link between two PDP-8 computers

Pierre Daujat

Zusammenfassung

Eine CAMAC-Verbindung zwischen einem PDP-8E und PDP-8I Rechner wird beschrieben. Die Verbindung besteht hauptsächlich aus Standard-CAMAC-Modulen; sie kann an die besonderen Anforderungen von "on-line"-Messungen und von photonuklearen Experimenten angepaßt werden.

Résumé

Description d'un système d'intercommunication entre un PDP-8E et un PDP-8I. Ce système est constitué essentiellement de tiroirs CAMAC normalisés; il peut être adapté aux besoins particuliers des mesures en ligne et au contrôle des expériences photonucléaires.

Riassunto

E descritto un canale di collegamento CAMAC fra un PDP-8E ed un PCP-8I. Il collegamento consiste principalmente di moduli stantard CAMAC et è adattabile alle esigenze particolari delle misure in linea e del controllo degli esperimenti fotonucleari.

Samenvatting

Beschreven wordt een CAMAC-datatransmissieverbinding tussen een PDP-8E en een PDP-8I. Deze verbinding bestaat hoofdzakelijk uit standaard CAMAC-modules en kan worden aangepast aan de specifieke eisen die worden gesteld in verband met de on-line besturing van photonucleaire experimenten.

Резюме

Описана связь между компутерами ПДП-8 Е и ПДП-8И. В большой части она составлена из блоков CAMAC и приспособлена к прямым измерениям и управлениям фото-ядерным экспериментом.

A differential discriminator in CAMAC
D. Kollbach and H.-U. Nachbar

Zusammenfassung

Diesen CAMAC-Modul selektiert die Amplituden analoger Eingabesignale von 0 bis −1v oder von 0 bis + 5 vwahlweise differentiele oder integral (2 fach) und erzeugt Standard-NIM-Ausgabeimpulse von −16mA. Die Betriebsarten, Schwellenwerte und andere Einzelheiten werden mittels CAMAC-Befehlen gewählt.

Résumé

Ce tiroir CAMAC effectue la discrimination en amplitude des signaux d'entrée analogiques jusqu'à −1v ou +5v, en mode différentiel ou en mode double intégration; il émet des impulsions de sortie NIM de −16mA. Les modes opératoires, les seuils et les autres caractéristiques sont choisis par des commandes CAMAC.

Riassunto

Il presente modulo CAMAC discrimina le ampiezze dei segnali analogici d'ingresso, fino a −1v e +5v in modo differenziale o integrale doppio, e genera impulsi d'uscita standard NIM da −16mA. I modi di funzionamento, le soglie e le altre caratteristiche sono selezionati da comandi CAMAC.

Samenvatting

Dit CAMAC-module discrimineert de amplituden van analoge ingangssignalen (−1v of +5v) en genereert standaard NIM uitgangspulsen van −16mA. Met behulp van CAMAC-opdrachten worden werkwijze, drempels en andere functies gekozen.

Резюме

Этот блок CAMAC дискриминирует амплитуды аналоговых входных сигналов до —1 V или +5 V либо в дифференциальном либо двойном интегральном режиме и генерирует стандартные, 16 mA импульсы NIM. Режимы работы, пороги и другие свойства выберается командами CAMAC.

A Branch Highway driver for the PDP-11computer
B. Bricaud, J. Durruty, J. C. Faivre, J. Pain

Zusammenfassung

Der in diesem Beitrag beschriebene CAMAC-Branch-Highway-Treiber steuert bis zu sieben Rahmen und überträgt die Daten über den UNIBUS auf einen PDP11 Rechner. Für einen 16-bit-CAMAC-Operation ist nur ein Computerbefehl notwendig.

Résumé

La commande d'interconnexion de branche CAMAC décrite dans cet article permet de contrôler jusqu'à sept châssis; elle transfère les données par l'intermédiaire de l'UNIBUS d'un ordinateur PDP-11. Une opération CAMAC 16 bits ne nécessite qu'une seule instruction machine.

Riassunto

L'elemento di comando del ramo principale CAMAC, descritto nel presente studio, controlla fino a sette contenitori e trasferisce dati attraverso l'UNIBUS di un calcolatore PDP-11. Per un'operazione CAMAC da 16 bit basta una sola istruzione del calcolatore.

Samenvatting

De beschreven CAMAC branch highway driver is ontworpen voor het besturen van ten hoogste 7 rekken en voor het overbrengen van gegevens via de UNIBUS van een PDP-11 computer. Met één enkele computeropdracht kan een CAMAC-bewerking van 16 bit worden uitgevoerd.

Резюме

Контроллер ветви CAMAC управляет до 7 крейтов и передает данные по магистрали UNIBUS компутера ПДП-11. Для одной 16 разрядной операции CAMAC нужна только одна комманда ЭВМ.

CAMAC - An educational program for manual crate control
B. Bjarland

Zusammenfassung

Ein Nova-Assembler-Programm ermöglicht die Eingabe von CAMAC-Befehlen durch einen Fernschreiber. Das Look at me Munster kann auf Verlangen ausgedruckt werden. Schnelle und langsame wiederholbare Betriebsarten sind möglich. Das Programm ist für den Unterricht und für die Demonstration des CAMAC Standards, sowie für die Entwicklung und das Testen von Modulen angewandt worden.

Résumé

Un programme en langage assembleur NOVA permet d'introduire les commandes CAMAC à partir d'une télétype. La configuration des L peut être imprimées sur demande. Des modes répétitifs rapides et lents sont prévus. Le programme est utilisé pour l'enseignement et la démonstration de CAMAC aux étudiants, ainsi que pour le développement et le contrôle des tiroirs.

Riassunto

Un programma redatto nel linguaggio assemblatore NOVA permette l'ingressodei comandi CAMAC da una telescrivente. La configurazione dei LAM puo essere stampata su richiesta. Sono disponibili modi ripetitivi veloci e lenti. Il programma è stato impiegato per insegnare e dimostrare il CAMAC a studenti, nonchè per applicazioni e prove dei moduli.

Samenvatting

Dit programma, dat in Nova assemblertaal is geschreven, maakt het mogelijk CAMAC-opdrachten via een teletype in te voeren. Het L-patroon kan desgewenst worden afgedrukt en zowel snelle als trage herhaling van de opdrachten is mogelijk. Doel van het programma is het demonstreren van CAMAC aan studenten, alsmede het ontwikkelen en testen van modulen.

Резюме

Программа в ассемблере Nova позваляет принимать комманды CAMAC из телетайпа. Слово L-сигналов может быть отпечатано по требованию. Предусмотрены быстрый и медленный режимы работы. Программа была применена для обучения и показа CAMAC — а студентам и для разработки и проверки модулей.

System approaches to analogue measurements
H. Liebendörfer and C. Manning

Zusammenfassung

CAMAC beruht im wesentlichen auf einer digitalen Systemkonzeption, weshalb Digital-Analog-Umsetzer (DACs) zur Behandlung von Analog-Ausgabedaten und Analog-Digital-Umsetzer (ADCs) für die Analog-Eingabedaten notwendig sind. ADCs sind ziemlich komplexe Anlagen, und dieser Beitrag soll zur Klärung einiger anstehender Fragen dienen.

Résumé

CAMAC est un système de conception essentiellement numérique; c'est pourquoi, il nécessite des convertisseurs numérique-analogique (DAC) pour le traitement des sorties analogiques, et des convertisseurs analogique-numérique (ADC) pour les entrées analogiques. Les convertisseurs ADC étant des instruments d'une relative complexité, cet article tente d'éclaircir les problèmes susceptibles de se poser.

Riassunto

Il CAMAC è sostanzialmente un sistema digitale, per il quale occorrono convertitori digitali-analogici (DAC) per trattare uscite analogiche, e convertitori analogico-digitali (ADC) per trattare ingressi analogici. Data la complessità degli ADC, il presente studio si propone di spiegare alcuni problemi che potrebbero presentarsi.

Samenvatting

CAMAC is in wezen een digitaal systeem. Voor de behandeling van analoge uitvoergegevens zijn bijgevolg digitaal-analoog-omzetters en voor analoge invoergegevens analoog-digitaal-omzetters vereist. Daar deze laatste nogal ingewikkelde instrumenten zijn, wordt in dit artikel getracht een aantal problemen op te lossen die in dit verband kunnen rijzen.

Резюме

Так как CAMAC является цифровой системой требуются АЦП для аналоговых входов и ЦАП для аналоговых выходов. В статии пояснены некоторые вопросы связаные с АЦА-ми, которые являются сложными приборами.

CAMAC PRODUCT GUIDE

CAMAC Bulletin No. 14

CAMAC PRODUCT GUIDE

HARDWARE

This guide consists of a list of CAMAC equipment which is believed to be offered for sale by manufacturers in Europe and the USA. The information has been compiled by CERN–NP–Electronics and is mainly based on information communicated by manufacturers and available up to the 20th September 1975.

Every effort has been made to ensure the completeness and accuracy of the list, and it is hoped that most products and manufacturers have been included. Inclusion in this list does not necessarily indicate that products are fully compatible with the CAMAC specifications nor that they are recommended or approved by the ESONE Committee. Similarly, omission from this list does not indicate disapproval by the ESONE Committee.

Reader service

Readers are advised to use the Reader service enquiry card, inserted in this Bulletin, if you wish to obtain more information on CAMAC Products, and to be on the manufacturers mailing list.

Remarks on some columns in the Index of Products

Column

NC – N is new, C is corrected entry.

WIDTH – 1 to 25, indicates module width or—for crates—the number of stations available.
– 0 indicates unknown width or format.
– Blank, the width has no meaning.
– NA indicates other format, normally a 19 inch rack mounted chassis.

NPR – Number in brackets is issue number of the Bulletin in which the item was or is described in the New Products section.

DELIV – Date on which item became or will become available.

REF No – Reader service reference number.

CLASSIFICATION GROUPS

INDEX OF PRODUCTS

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	1 DATA MODULES — I/O TRANSFERS AND PROCESSING						
	11 Digital Serial Input Modules — Scalers, Time Interval and Bi-directional Counters, Serial Coded etc.						
	111 Simple Serial Binary Registers						
N	24 BIT SCALER (15MHZ)	CAM 2,01	METRIMPEX	1	//2		14,1001
	1X24 BIT BINARY BLIND SCALER (20MHZ NIM OR 10MHZ TTL I/P,EXT INHIBIT IN,OVF O/P)	J EB 10	SCHLUMBERGER	1	//1		14,1002
	MINISCALER (2X16BIT,30MHZ,SEPARATE GATES AND EXTERNAL RESET,NIM LEVELS)	1002	BORER	1	/69		14,1003
	MINISCALER (2X16BIT,30MHZ,SEPARATE GATES AND EXTERNAL RESET,NIM LEVELS)	002	NUCL. ENTERPRISES	1			14,1004
	MINISCALER(2X16BIT,30MHZ,SEPARATE GATES AND EXT RESET,NIM LEVELS)	C 104	RDT	1	//1		14,1005
	DUAL SCALER (2X16BIT, 50MHZ)	DS 050	STND ENGINEERING	1	//3		14,1006
	DUAL 150 MHZ 16 BIT SCALER (ONE 50 OHMS, ONE UNTERMINATED NIM INPUT PER SCALER)	2S 2024/16	SEN	1	//0		14,1007
	DUAL SCALER (2X16BIT, 100MHZ)	DS 100	STND ENGINEERING	1	//3		14,1008
	DUAL SCALER (2X16BIT, 150MHZ)	DS 150	STND ENGINEERING	1	//4		14,1009
	DUAL SCALER (2X16BIT, 200MHZ)	DS 200	STND ENGINEERING	1	//4		14,1010
	DUAL 24 BIT BINARY SCALER (15MHZ, NIM OR TTL INPUTS)	FHC 1313	FRIESEKE	1	//2		14,1011
N	QUAD SCALER (4X12 OR 2X24 BIT, 15MHZ)	CAM 2,02	METRIMPEX	1	//2		14,1012
	DOUBLE SCALER (24/16BIT,50MHZ,2 I/P & 3 GATE MODES,INHIBIT, P1=OVERFLOW) SELECTABLE,50MHZ,COMMON GATE,NIM LEVELS)	C=DS=24	WENZEL ELEKTRONIK	1	//2		14,1013
	FOUR=FOLD CAMAC SCALER (4X16BIT,40MHZ, ONE 50 OHMS,ONE HI=Z NIM I/P PER SCALER)	4 S 2004	SEN	1	//0		14,1022
	TIME DIGITIZER(4X16BIT,CLOCK RATE 70/85MHZ, WITH CENTER FINDING LOGIC)	TD 2031	SEN	1	//2		14,1023
	TIME DIGITIZER (4X16BIT,CLOCK RATE 70/85MHZ,NIM LEVELS)	TD 2041	SEN	1	//2	(4)	14,1024
	QUAD SCALER (4X16BIT, 50MHZ)	QS 050	STND ENGINEERING	1	//3		14,1025
	SERIAL REGISTER (4X16BIT,2X32BIT SELECT=ABLE,100MHZ,COMMON GATE,NIM LEVELS)	SR 1608	GEC=ELLIOTT	1	//1		14,1026
	FOUR=FOLD SCALER(4X16BIT,2X32BIT SELECT=ABLE,100MHZ,COMMON GATE,NIM LEVELS)	4 S 2003/100	SEN	1	//0		14,1027
	QUAD SCALER (4X16BIT, 150MHZ)	QS 150	STND ENGINEERING	1	//4		14,1028
	QUAD SCALER (4X16BIT, 200MHZ)	QS 200	STND ENGINEERING	1	//4		14,1029
	QUAD SCALER (4X24BIT, 50MHZ, DATAWAY AND/OR EXT FAST INHIBIT, NIM LEVELS)	S424S	EG&G/ORTEC	1		(7)	14,1030
N	SCALER=TIMER (4X24BIT, INT, 1MHZ CRYSTAL OSCILLATOR, RESOLUTION 10MHZ)	CAM 5,02	METRIMPEX	1	//3		14,1031
	QUAD COUNTING REGISTER(4X24BIT,NIM INPUT TTL INHIBIT IN,TTL CARRY AND OVF OUT)	709=2	NUCL. ENTERPRISES	1	//1		14,1032

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	SCALER (4X24BIT, 50MHZ)	9051	NUCL, ENTERPRISES	1	//3		14,1033
	QUAD SCALER (4X24BIT,150/125MHZ,DATAWAY AND/OR EXT FAST INHIBIT,NIM LEVELS)	S424B	EG&G/ORTEC	1	//1		14,1034
	QUAD SCALER (4X24BIT, 200MHZ, DATAWAY AND/OR EXT FAST INHIBIT, NIM LEVELS)	S424F	EG&G/ORTEC	1		(13)	14,1035
	QUAD SCALER (4X24BIT, 125MHZ,INTERRUPT STRUCTURE, INDIVIDUAL INHIBIT INPUTS)	S1	JUERGER	1	//2	(5)	14,1036
	QUAD SCALER (4X24BIT, 200MHZ,INTERRUPT STRUCTURE, INDIVIDUAL INHIBIT INPUTS)	S1=1	JUERGER	1	//3		14,1037
	QUAD 100MHZ SCALER (4X24BIT,DISCR LEVEL =0,5V,TIME=INTERVAL APPL,NIM INHIB I/P)	85A	JORWAY	1	//1	(2)	14,1038
	QUAD 100 MHZ SCALER(4X16/24BIT,=0,5V I/P THRESHOLD,COMMON EXT FAST INHIBIT,NIM)	2550B	LRS=LECROY	1	//0		14,1039
	QUAD SCALER (4X24BIT, 300MHZ, 7=SEGMENT DISPLAY/SCALER, OVF GIVES LAM)		SCHLUMBERGER	3		(12)	14,1040
	QUAD SCALER (4X24BIT OR 2X48BIT,100MHZ, OVF GIVES LAM, COMMON INHIBIT GATE)	QS 100	SIND ENGINEERING	1	//3	(12)	14,1041
	TIME DIGITIZER (6 CHANNELS,16 BITS, 100 MHZ CLOCK RATE)	TD	JUERGER	1	//4	(11)	14,1042
C	12=CHANNEL 100MHZ SCALER (16BIT,=0,5V I/P THR, FAST CLEAR, CASCADABLE, LAM)	2552	LRS=LECROY	1	05//5		14,1043
	12=CHANNEL 16 BIT SCALER (CERN SPS2135)	9054	NUCL, ENTERPRISES	1		(10)	14,1044
	HEX TTL/NIM 50 MHZ SCALER	3610	KINETIC SYSTEMS	1	//3		14,1045
	HEX COUNTING REGISTER (6X24BIT, 100MHZ NIM & TTL LEVELS, TTL CARRY OVF, BIN)	320	HYTEC	1	//4		14,1046
	HEX NIM 100 MHZ SCALER	3615	KINETIC SYSTEMS	1	//3	(8)	14,1047
	12=CHANNEL 100 MHZ SCALER(12X24BIT,=0,5V I/P THR, COMMON FAST CLEAR & INHIB, NIM)	2551	LRS=LECROY	1	//4	(12)	14,1048

112 Simple Serial Decade Registers

	1X6 BCD DECADE SCALER (30 MHZ, BUILT=IN DISPLAY)	J EA 20	SCHLUMBERGER	1	//3		14,1049
	DUAL 24 BIT BCD SCALER (15MHZ, NIM OR TTL INPUTS)	FHC 1311	FRIESEKE	1	//2		14,1050
	2X6 BCD DECADE SCALER = 100 MHZ WITH REMOTE DISPLAY	J EA 10	SCHLUMBERGER	1	//1		14,1051
	QUAD BCD SCALER (4X6 DECADES,30MHZ)	9021	NUCL, ENTERPRISES	1	//1		14,1052
	HEX COUNTING REGISTER (6X24BIT, 100MHZ NIM & TTL LEVELS, TTL CARRY OVF, BCD)	321	HYTEC	1	//4		14,1053

113 Preset Serial Binary Registers

	PRESET COUNTING REGISTER (16BIT,10MHZ, NIM/TTL I/P,TTL INHIB + O/P,DATAWAY SET)	7039=1	NUCL, ENTERPRISES	1	//0		14,1054
N	PRESET SCALER (24BIT)	CAM 2,04	METRIMPEX	1	//4		14,1055
	SCALER 50 MHZ (12/16/18/24BIT,PRESET WITH OVF LINE,CONSTANT DEADTIME)	C 72451=A3=A1	SIEMENS	1	//2		14,1056
	PRESET SCALER(24/16BIT,50MHZ,DATAW, SET, BUFFER,2 I/P & 3 GATE MODES,INHIB,OVFLO)	C=PS=24	WENZEL ELEKTRONIK	1	//2		14,1057
C	BIN,PRESET SCALER/BCD=DISPLAY(24BIT/8DEC 50MHZ,DATAWAY SET,2I/P&GATE MODES,INHIB)	C=SD=24	WENZEL ELEKTRONIK	1	//5	(14)	14,1058
	DUAL PRESET COUNTING REGISTER(16BIT BIN)	2204	BI HA SYSTEMS	1	//3		14,1059
	DUAL PRESET COUNTER/TIMER (2X16/24BIT, 40MHZ MIN, SELF RELOADABLE)	1006	BORER	1	//4		14,1060
	2X24 BIT PRESET SCALER (100MHZ COUNTING)	J EP 30	SCHLUMBERGER	1	//3		14,1061
	PRESET QUAD BINARY COUNTER (4X24BIT, 75 MHZ, NIM & TTL LEVELS, TTL CARRY OVF)	310	HYTEC	1	//3		14,1062
	(SAME BUT 50 MHZ)	350		1	//4		

114 Preset Serial Decade Registers

	REAL TIME CLOCK (3,8 USEC TO 18,2 HRS, PRESET=TIME AND PRESET=COUNT MODES)	RTC 2014	SEN	1	//1		14,1063
	24BIT BCD PRESET=SCALER (12MHZ, NIM OR TTL INPUTS,MANUAL OR DATAWAY PRESET)	FHC 1301	FRIESEKE	2	//1	(1)	14,1064
	24BIT BCD PRESET=SCALER (12MHZ, NIM OR TTL INPUTS,DATAWAY PRESET)	FHC 1302	FRIESEKE	1	//1		14,1065

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	6 BCD DECADE SCALER (MANUAL AND DATAWAY PRESET,1 MHZ, START/STOP OUTPUT)	J EP 20	SCHLUMBERGER	2	//1		14,1066
	PRESET SCALER (20MHZ,8DECADE BCD,7 SEGM LED INDICATES CONTENTS AND PRESET NO)	PSR 0801	GEC-ELLIOTT	1	//2	(7)	14,1067
	PRESET SCALER(10MHZ,8 DECADE BCD,DISPLAY OF 2 SIGNIF NUMBERS+EXP,MAN PRESET,NIM)	C 103	HDT	3	//1		14,1068
	DUAL PRESET COUNTING REGISTER(4 DECADES)	2204	HI MA SYSTEMS	1	//3		14,1069
	PRESET QUAD DECADE COUNTER (4X6 DECADES, 75 MHZ, NIM & TTL LEVELS, TTL CARRY OVF)	511	HYTEC	1	//3		14,1070
	(SAME BUT 50 MHZ)	551		1	//4		

117 Other Digital Serial Input Modules (Bi-Directional Sequential, Shift Types)

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
N	INCREMENTAL ENCODER INPUT (ACCEPTS QUADRATURE INPUTS, 24 BITS)	IE	JOERGER	1	09//5	(14)	14,1071
	UP/DOWN PRESETTABLE COUNTER(24BIT,10MHZ, GATE AND PULSE BURST OUTPUTS)	S2	JOERGER	1	//2	(5)	14,1072
	UP/DOWN PRESETTABLE COUNTER(6 BCD DIGITS 10MHZ, MANUAL AND DATAWAY PRESET)	S2-1	JOERGER	1	//3		14,1073
	QUAD PRESETTABLE UP-DOWN COUNTER	3640	KINETIC SYSTEMS	1	//3		14,1074
	DUAL INCREMENTAL POSITION ENCODER (2X20 BIT X-Y DIGITIZATION BY UP-DOWN COUNTER)	2IPE 2019	SEN	1	//1		14,1075
N	TOGGLING SCALER/TIMER (CONTINUOUS COUNTING WITH NO CHANGEOVER LOSS)	0311	SENSIUN	1	03//5		14,1076

12 Digital Parallel Input Modules — Storing and Non-storing Registers, Coinc. Latch, Lam, Status etc.

121 Non-Storing Registers (Gates)

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	PARALLEL INPUT GATE (CERN SPS2133,16BIT)	9049A	NUCL. ENTERPRISES	1		(10)	14,1077
	ISOLATED INPUT GATE(16BIT,VERSION AG302D FOR 12,24 OR 48V, AG302A FOR 115VAC)	AG 302*	STND ENGINEERING	1	//4		14,1078
	INPUT GATE (16BIT, CONTACT CLOSURE)	AG 302C	STND ENGINEERING	1	//4		14,1079
	INPUT GATE (16BIT)	PG 301	STND ENGINEERING	1	//3		14,1080
C	INPUT GATE (24BIT, SOURCE SELECTION BY 6BIT OUTPUT, DATAWAY GEN STROBE OUT)	207	JORWAY	1	//4	(8)	14,1081
	INPUT GATE 24-BIT	3420	KINETIC SYSTEMS	1	//1	(4)	14,1082
N	PARALLEL INPUT GATE (24BIT)	CAM 2,07	METHIMPEX	1	//4		14,1083
	PARALLEL INPUT GATE (22BIT STATIC DATA, 500 NSEC INTEGRATION,STROBE SETS L,TTL)	7060-1	NUCL. ENTERPRISES	1	//0		14,1084
	PARALLEL INPUT GATE (24 BIT)	9049B	NUCL. ENTERPRISES	1		(10)	14,1085
	INPUT GATE (24BIT)	PG 304	STND ENGINEERING	1	//3		14,1086
	24-BIT ISOLATED INPUT GATE	3471	KINETIC SYSTEMS	1	//3		14,1087
	STATIC DIGITAL INPUT (2X16BIT, TTL)	C 76451-A8-A4	SIEMENS	1	//3	(6)	14,1088
	DUAL INPUT GATE (16BIT)	PG 601	STND ENGINEERING	1	//3		14,1089
	DUAL PARALLEL STROBED INPUT GATE(2X24BIT HANDSHAKE MODE TRANSFER TO DATAWAY,TTL)	61	JORWAY	1	//0		14,1090
	DUAL PARALLEL INPUT GATE (2X24BIT,NON-INTERLOCK CONTROL TRANSF TO DATAWAY,TTL)	61-1	JORWAY	1	//0		14,1091
	INPUT GATE DUAL 24 BIT	3472	KINETIC SYSTEMS	1			14,1092
	INPUT GATE (2X24BIT STATIC DATA,INTEGR FOR 1USEC,TTL LEVELS, 2X37-WAY I/P CONN)	321	POLON	1	//4		14,1093
	INPUT GATE (2X24BIT STATIC DATA,INTEGR FOR 10USEC,TTL LEVELS,2X37-WAY I/P CONN)	321A		1	//4		
	(SAME, INTEGRATION FOR 5MSEC)	321B		1	//4		
	DUAL 24 BIT PARALLEL INPUT GATE (WITH LED DISPLAY OPTION)	PG-604	STND ENGINEERING	1	//2	(6)	14,1094
	PARALLEL INPUT GATE (3X16BIT INPUT FROM ISOLATING CONTACTS)	1061	BURER	1	//2	(4)	14,1095
	3X16-BIT INPUT GATE (INPUTS ISOLATED BY OPTO-COUPLERS)	1063	BURER	1	//3	(8)	14,1096
	DIGITAL INPUT REGISTER WITH OPTO COUPLER (4X8BIT PARALLEL INPUT GATES,WITH L)	DD 200-2003	DORNIER	1	//2		14,1097
	(WITH FRONT PANEL CONNECTOR)	DD 200-2203		1	//2		

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF, No.
	DIGITAL INPUT REGISTER (5X8BIT PARALL INPUT GATES,5TH BYTE SETS L,TTL,1=H)	DD 200-2001	DOMNIER	1	//1		14,1098
	(WITH FRONT PANEL CONNECTOR)	DD 200-2201		1	//2		
	(MODULE WITH ONLY LOGIC BOARD)	DD 200-2000		1	//3		
	DIGITAL INPUT REGISTER (5X8BIT PARALL INPUT GATES,5TH BYTE SETS L,HLL,1=H)	DD 200-2002	DOMNIER	1	//2		14,1099
	(WITH FRONT PANEL CONNECTOR)	DD 200-2202		1	//2		
	PARALLEL INPUT GATE(16X16BIT,TTL, 1=LOW)	IG 25601	GEC-ELLIOTT	2	//2		14,1100
	128 BIT RECEIVER (ADDRESSABLE AS 8 16BIT WORDS OR 128 1-BIT WORDS)	C 341	INFORMATEK	1	//3		14,1101

122 Storing Registers

	OPTICAL ISOLATED INPUT REGISTER	2601	BI HA SYSTEMS	1	//4		14,1102
	PARALLEL INPUT REGISTER (16BIT,CONTINUOUS OR STROBED MODES CONTROLLED BY REG)	7014-1	NUCL, ENTERPRISES	1	//0		14,1103
	DYN, DIG, INPUT (16BIT, TTL, LAM IF INPUT 0-1 OR 1-0 OR BOTH)	C 76451-A17-A4	SIEMENS	1	//3	(6)	14,1104
	INPUT REGISTER (16BIT)	PR 301	STND ENGINEERING	1	//3		14,1105
	DYNAMIC DIGITAL INPUT 16BIT FLOATING I/P	C 76451-A17-A3	SIEMENS	1	//3	(6)	14,1106
	ISOLATED INPUT REGISTER(16BIT,AR302D FOR 12,24 OR 48VDC, AR302A FOR 115VAC)	AR 302-	STND ENGINEERING	1	//4		14,1107
	INPUT REGISTER (16BIT,CONTACT CLOSURE)	AR 302C	STND ENGINEERING	1	//4		14,1108
	PARALLEL-INPUT-REGISTER (SINGLE 16/24BIT OPT,READY SIGNALS,I/O TTL,CONTROL BUS)	MS PI 2 1230/1	AEG-TELEFUNKEN	1	//0	(1)	14,1109
	INPUT REGISTER (24BIT, SPEC CONN, 8 BIT ALSO VIA LEMO,LAM ON NON-ZERO OR STROBE)	FHC 1308	FRIESEKE	1	//1		14,1110
N	CONTACT SENSE (24BIT ISOLATED INPUT REG, SENSES 12,24,48VDC OR 120VAC INPUTS)	CS	JOERGER	1	09//5		14,1111
N	CONTACT SENSE (24BIT ISOLATED INPUT REG, SENSES STATE OF SERIES SWITCHES)	CS-1		1	08/75		
	INPUT REGISTER 24-BIT	3470	KINETIC SYSTEMS	1	//1	(4)	14,1112
	INPUT REGISTER (24BIT)	PR 304	STND ENGINEERING	1	//3		14,1113
	INPUT REGISTER (24 INPUTS, + STROBE, OPTICALLY ISOLATED)	IR-2	JOERGER	1	//4	(11)	14,1114
	BALANCED INPUT REGISTER WITH ADDRESSING	3430	KINETIC SYSTEMS	1	//2	(8)	14,1115
	PARALLEL INPUT REGISTER (2X16BIT, TTL)	2312	BI HA SYSTEMS	1	//3		14,1116
	DUAL INPUT REGISTER(2X16BIT,LAM & STROBE I/P & DATA-READ-STROBE O/P PER CHANNEL)	PR 1610 SERIES	GEC-ELLIOTT	1	//3		14,1117
	CAMAC UNTERM, I/P'S VIA SCHMITT TRIGGERS I/P FILTER RESPONSE 1USEC TO 10MS	PR 1611		1			
	DUAL 16 BIT INPUT REGISTER (TTL LEVELS, CERN SPECS 072)	2IR 2002	SEN	1	//2		14,1118
	DUAL 16 BIT INPUT REGISTER(EXT STROBE OR DATAWAY COMMAND STORES DATA,TTL LEVELS)	2IR 2010	SEN	1	//0		14,1119
	DUAL INPUT REGISTER (16BIT)	PR 601	STND ENGINEERING	1	//3		14,1120
	DIGITAL INPUT (2X16BIT FLOATING INPUT)	C 76451-A8-A3	SIEMENS	1	//3	(6)	14,1121
	DUAL 24 BIT PARALLEL INPUT REGISTER(TTL)	2322	BI HA SYSTEMS	1	//3		14,1122
	DUAL 24 BIT INPUT REGISTER (TTL, HANDSHAKE)	RI-224	EG&G/ORTEC	1	//2		14,1123
	DUAL INPUT REGISTER(2X24BIT,LAM & STROBE I/P & DATA-READ-STROBE O/P PER CHANNEL)	PR 2400 SERIES	GEC-ELLIOTT	1	//3		14,1124
	CAMAC UNTERM, I/P'S VIA SCHMITT TRIGGERS I/P FILTER RESPONSE 1USEC TO 10MS	PR 2401		1	//3		
	(SAME BUT WITH TWISTED PAIR INPUTS)	PR 2402		1	//3		
	(SAME BUT WITH OPTICAL ISOLATION INPUT, LOGIC 1 = 5V OR 12MA)	PR 2403		1	//3		
	DUAL INPUT REGISTER (2X24BIT,I/P INTEGR TTL, PULL LAM, OUTPUT STROBES)	220	HYTEC	1	//3		14,1125
	INPUT REGISTER (2X24BIT, 3 MODES OF DATA ENTRY, LED DISPLAY)	IR	JOERGER	1	//2	(7)	14,1126
	DUAL PARALLEL INPUT REGISTER(2X24BIT,EXT LOAD REQUEST,4 OPER MODES,TTL LEVELS)	60A	JORWAY	1	//0		14,1127
	24-BIT DUAL PARALLEL INPUT REGISTER (A HAS LO-Z, B HAS UNTERMINATED INPUT)	9041A/9041B	NUCL, ENTERPRISES	1	//2	(7)	14,1128
	PARALLEL INPUT REGISTER (2X24 BITS)	J RE 10	SCHLUMBERGER	1	//3	(7)	14,1129
	DUAL 24 BIT PARALLEL INPUT REGISTER (WITH LED DISPLAY OPTION)	PR-604	STND ENGINEERING	1	//2		14,1130

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
C	DUAL INPUT REG,(2X24BIT,SEP,TIMING,LOGIC BITWISE POS/NEG,4TIMING& 3DATA IN MODES)	C-IC-48	WENZEL ELEKTRONIK	1	/75	(14)	14,1131
N	QUAD 24 BIT INPUT REGISTER (4x24, HAND-SHAKE DATA TRANSFER, 3 DATA ENTRY MODES)	QIR	JUERGER	1	09/75	(14)	14,1132
	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				14,1133
	DIGITAL INPUT REGISTER, EXTERNAL STROBE (4X8BIT INPUT LATCHES, 1X8BIT SET LAM)	DO 200-2004	DORNIER	1	/73		14,1134
	(SAME WITH FRONT PANEL CONNECTOR)	DO 200-2204		1	/73		

123 Terminated Signal Input Registers (Coinc. Latch, Pattern etc.)

	12 BIT PARALLEL INPUT REGISTER (NIM)	2351	BI RA SYSTEMS	1	/73		14,1135
	STROBED INPUT REGISTER (12BIT COINC AND LATCH,NIM LEVELS,PATTERN AND L-REQ APPL)	SIR 2026	SEN	1	/70		14,1136
	16BIT DISCRIMINATOR-COINCIDENCE REGISTER	2352	BI RA SYSTEMS	2	01/75		14,1137
	FAST COINCIDENCE LATCH(16BIT,DISCR I/P, MIN 2 NSEC STROBE-SIGNAL OVERLAP)	64	JORWAY	1	/71	(1)	14,1138
	16 FOLD DCR (16 DISCR, COMMON STROBE, -70MV THRESHOLD, FAST SUMMING OUTPUTS)	2340B	LRS-LECROY	2	/71	(6)	14,1139
	16-CH COINCIDENCE REGISTER (STROBE I/P, 2NS OVERLAP,FAST SUM O/P AND CLEAR,NIM)	2341S	LRS-LECROY	1	/71	(4)	14,1140
N	16 CHANNEL STROBED COINCIDENCE (16 COINC INPUTS, COINC & LAM OUTPUT, 10NS RESOL.)	CAM 8,05	METRIMPEX	2	/74		14,1141
	PATTERN UNIT (16 INDIV NIM INPUTS,COMMON NIM GATE)	021	NUCL. ENTERPRISES	2	/71	(5)	14,1142
	FAST INPUT REGISTER (ASSEMBLES 16BIT WORDS FROM IL2 INPUTS)	9053	NUCL. ENTERPRISES	1	/74		14,1143
	PATTERN UNIT(16BIT,I/P STROBED WITH COMMON GATE,10 NSEC OVERLAP,NIM LEVELS)	C 101	RDT	2	/71		14,1144
	16 BIT PATTERN UNIT (NIM I/P AND GATE)	J PU 10	SCHLUMBERGER	1	/72		14,1145
	PATTERN UNIT 16 BIT (16 INDIVIDUAL NIM INPUTS,COMMON NIM GATE, CERN SPECS 021)	16P 2007	SEN	2	/70		14,1146
	16 BIT PATTERN UNIT (CERN 071, 16 INDIV NIM INPUTS,COMMON NIM GATE,LED DISPLAY)	16P 2047	SEN	1	/72	(11)	14,1147
	COINCIDENCE REGISTER/LATCH (16 CHANNEL)	CR 116	STND ENGINEERING	1	/74		14,1148
	COINCIDENCE REGISTER/LATCH (16 CHANNEL)	CR 216	STND ENGINEERING	1	/74		14,1149
	COINCIDENCE REGISTER (16 CH,COMMON GATE, MIN OVERLAP 2NS,DOUBLE PULSE RESOL 10NS)	CR-6001	STND ENGINEERING	1	/74	(12)	14,1150
	COINCIDENCE LATCH (24 NIM INPUTS WITH COMMON STROBE, EXT RESET, 2NSEC OVERLAP)	C124	EG&G/ORTEC	2			14,1151
N	PARALLEL INPUT REGISTER (24BIT)	CAM 2,05	METRIMPEX	1	/74		14,1152
	COINCIDENCE REGISTER/LATCH (24 CHANNEL)	CR 224	STND ENGINEERING	1	/74		14,1153
	COINCIDENCE BUFFER (2X12BIT,ONE STROBE PER 12BITS,MIN 2NS OVERLAP,NIM INPUTS)	C212	EG&G/ORTEC	2	/71		14,1154

124 Manual Input Modules (Word Generators, Parameter Units)

	PARAMETER UNIT 12 BIT (PROVIDES 12 BIT COMMUNICATION,PUSH BUTTON L-REQUEST)	P 2005	SEN	1	/70		14,1155
	MANUAL INPUT REGISTER (INPUTS A HAND-SET 16-BIT WORD, MANUAL AND ELECTR LAM I/P)	1041	BORER	1	/73	(8)	14,1156
	24 BIT PARAMETER UNIT	2501	BI RA SYSTEMS	1	/73		14,1157
	WORD GENERATOR (24BIT WORD MANUALLY SET BY SWITCHES)	WG 2401	GEC-ELLIOTT	1	/71		14,1158
	DATA SWITCHES (16/24 BITS,READABLE + CONTENT ADDR)	C 322	INFORMATEK	1	/72		14,1159
N	MANUAL INPUT/OUTPUT (TEST UNIT PROVIDES MANUAL DATA INPUT & VISUAL DATA OUTPUT)	MI/O	JUERGER	1	08/75		14,1160
	MANUAL INPUT/OUTPUT REGISTER (24 BITS, SWITCH I/P + LAM, 24 LED O/P REGISTER)	201	JORWAY	1	/74	(11)	14,1161
C	24-BIT MANUAL INPUT	3460	KINETIC SYSTEMS	2	/73		14,1162
N	24-BIT MANUAL INPUT	3461		1	/75		
	WORD GENERATOR (24 BITS OF BINARY DATA, SWITCH SELECTED)	9020	NUCL. ENTERPRISES	1	/71	(2)	14,1163
	24 BIT WORD GENERATOR WITH LAM	WGR-241	STND ENGINEERING	1	/73		14,1164

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	MANUAL REGISTER (FOUR 16 BIT WORDS)	231	PULON	3	//4		14,1165
	PARAMETER UNIT (QUAD 4=DECADE BCD PARAMETERS MANUALLY SET)	022	NUCL, ENTERPRISES	4	//1	(2)	14,1166
	PARAMETER UNIT (QUAD 4 DECADE BCD PARAMETERS MANUALLY SET)	C 105	RDT	4	//1		14,1167

127 Other Parallel Input Modules (Incl. Lam and Status Registers, see 232 for Lam Grader)

	24=BIT INTERRUPT REGISTER (STATUS COMPARED,CHANGE GIVES LAM)	1051	BORER	1	//2	(3)	14,1168
	PRIORITY INPUT REGISTER(12BITS ORED TO LAM,FAST COINC LATCH APPL,MASK REGISTER)	63	JORWAY	2	//0		14,1169
	INPUT REGISTER (12 BIT, ORED TO LAM, COINCIDENCE LATCH APPL, NIM INPUTS)	65	JORWAY	1	//4		14,1170
N	INTERRUPT REQUEST REGISTER (16 INPUTS, ANY INPUT GIVES LAM)	CAM 2,09	METRIMPEX	1	//2		14,1171
N	INTERRUPT REQUEST REGISTER (8 CHANNELS)	9608	NUCL, ENTERPRISES	0		(14)	14,1172
	INTERRUPT REQUEST REGISTER	EC 218	NUCL, ENTERPRISES	1			14,1173
	LAM REQUEST REGISTER (16 BIT)	300	PULON	1	//4		14,1174
	INTERRUPT ALARM REGISTER (16 BITS, INDIVIDUALLY MASKABLE)	J IR 10	SCHLUMBERGER	1	//4	(11)	14,1175
	64 LINE SURVEYOR (SINGLE OR CONTINUOUS SURVEY CYCLES, 3 SURVEY MODES)	64LS 2052	SEN	1		(9)	14,1176
	ISOLATED INTERRUPT GATE(16BIT,*=D FOR 12,24 OR 48V,*=A FOR 115VAC VERSION)	AIG 302*	STND ENGINEERING	1	//4		14,1177
	INTERRUPT GATE (16BIT,CONTACT CLOSURE)	AIG 302C	STND ENGINEERING	1	//4		14,1178
	ISOLATED INTERRUPT REGISTER(16BIT,*=D FOR 12,24 OR 48VDC,*=A FOR 115VAC)	AIR 302*	STND ENGINEERING	1	//4		14,1179
	INTERRUPT REGISTER(16BIT,CONTACT CLOSURE)	AIR 302C	STND ENGINEERING	1	//4		14,1180
	INTERRUPT GATE (24BIT)	IG 304	STND ENGINEERING	1	//4		14,1181
	DUAL INTERRUPT GATE (24BIT)	IG 604	STND ENGINEERING	1	//4		14,1182
	INTERRUPT REGISTER (12BIT) INTERRUPT REGISTER (16BIT) INTERRUPT REGISTER (24BIT)	IR 012 IR 016 IR 024	STND ENGINEERING	1 1 1	//4 //4 //4		14,1183
	INTERRUPT REGISTER (24BIT)	IR 304	STND ENGINEERING	1	//4		14,1184
	STATUS INTERRUPT (24BIT,I/P&LATCH&LAM& MASK,GROUP&SEL=LAM=TEST,VAR,LOGIC&LEVEL)	C=SI=24	WENZEL ELEKTRONIK	1	//4	(12)	14,1185

13 Digital Output Modules — Serial: Clocks, Timers, Pulse Generators, Parallel: TTL Output, Drivers

131 Serial Output Modules (Clocks, Timers, Pulse GEN)

	PRESET SCALER (LEVEL OR PULSE TRAIN O/P, DURATION SET BY COMMAND,SINGLE & REPEAT)	PSR 0801	GEC=ELLIOTT	1	//3		14,1186
N	CLOCK PULSE GENERATOR (10 FIX & 1 PRO= GRAMMABLE O/P, INT, 1MHZ, EXT, MAX 5MHZ)	CAM 5,01	METRIMPEX	1	//3		14,1187
N	SCALER=TIMER (4X24BIT, INT, 1MHZ CRYSTAL OSCILLATOR, RESOLUTION 10MHZ)	CAM 5,02	METRIMPEX	2	//3		14,1188
	CRYSTAL CLOCK GENERATOR (7 TTL OUTPUTS FOR 1HZ TO 1MHZ FREQUENCY DECADES)	FMC 1303	FRIESEKE	1	//1	(1)	14,1189
	CRYSTAL CONTROLLED PULSE GENERATOR(7 DE= CADES=1HZ TO 1MHZ=500NS PULSES OUT,TTL)	PG 0001	GEC=ELLIOTT	1	//1		14,1190
	REAL TIME CLOCK (4SEC CLOCK/5MSEC STOP WATCH)	C 320	INFORMATEK	1	//2		14,1191
	CLOCK GENERATOR (INT 10MHZ, EXT 50MHZ, 8 DECADE STEPS,PLUS PROGRAMMABLE OUTPUT)	CG	JOERGER	1	//2	(7)	14,1192
	GATED CLOCK (10MHZ TO 1HZ, INT=EXT CLOCK, SYNCHRONOUS GATING)	217	JORWAY	1	//4	(11)	14,1193
	CLOCK PULSE GENERATOR (7 OUTPUTS=1HZ TO 1MHZ=IN DECADE STEPS,10MHZ EXT IN,TTL)	7019=1	NUCL, ENTERPRISES	1	//0		14,1194
	CLOCK GENERATOR(INTERN 1MHZ, EXT 10MHZ, 7 DECADES 1HZ=1MHZ TTL O/P,50SEC WIDTH)	730A	PULON	1	//4		14,1195
	CLOCK PULSE GENERATOR(7 DECADES=1HZ TO 1MHZ=500 NSEC PULSES OUT,TTL AND NIM)	C 109	RDT	1	//1		14,1196
	1 HZ - 1 MHZ QUARTZ CLOCK (7 O/P = 1HZ TO 1MHZ=200 TO 800 NSEC WIDTH,TTL LEVEL)	J HG 10	SCHLUMBERGER	1	//1		14,1197

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	QUARZ-CLOCK WITH 2 TIMER FUNCTIONS	C 76451-A14-A2	SIEMENS	1	//2		14,1198
	CAMAC-CLOCK-GENERATOR(7 DECADES-10MHZ TO 1HZ,50/500 NSEC O/P PULSES,2,8V/50 OHMS)	C-CG-10	WENZEL ELEKTRONIK	1	//1		14,1199
	CLOCK/TIMER (0,001S TO 10 HRS TIME INTERVAL,TIME-OF-DAY OUTPUT)	1411	HONER	1	//2	(3)	14,1200
	REAL TIME CLOCK, LIVE TIME INTEGRATOR, PRESET TIMER	RC014	EG&G/ORTEC	1	//3		14,1201
	REAL TIME CLOCK (COUNTS ,1 SEC TO 999 DAYS, DISPLAYS HRS/MIN/SEC, 50/60HZ GEN)	RTC	JOERGER	2	//3	(7)	14,1202
N	WATCHDOG TIMER (MONITORS SYSTEM ACTIVITY GENERATES AUDIO ALARM & CONTACT CLOSURE)	WT	JOERGER	1	08//5	(14)	14,1203
	REAL TIME CLOCK	9064	NUCL, ENTERPRISES	1		(10)	14,1204
	REAL TIME CLOCK (3,8 USEC TO 18,2 HRS, PRESET-TIME AND PRESET-COUNT MODES)	RTC 2014	SEN	1	//1		14,1205
	INTERVAL TIMER/WATCHDOG (100USEC-300SEC INTERVAL, 1 SEC--100 SEC TIMEOUT)	EC 384	SENSION	1	//4	(13)	14,1206
	REAL TIME CLOCK (PRESET COUNTER, PRESET TIMER 3,8USEC TO 18,2 HRS, ELAPSE TIME)	RTC 018	STND ENGINEERING	1	//4	(12)	14,1207
	DEAD TIME COUNTER	2203	BI HA SYSTEMS	1	//4		14,1208
	TIMER MODULE	3655	KINETIC SYSTEMS	1	//3		14,1209
	TIME BASE (10 TO 100MHZ IN INCREMENTS OF 10MHZ, USED WITH TD 2031/TD 2041)	TB 2032	SEN	1	//1		14,1210
	TIMER (MIN 1USEC,OVF FROM COUNTER-PP1)	C 76451-A12-A1	SIEMENS	2	//3	(6)	14,1211
	TEST PULSE GENERATOR (5 TO 50 NSEC NIM O/P PULSE DERIVED FROM S1,F(25) OR EXT)	TPG 0202	GEC-ELLIOTT	1	//1		14,1212
	TEST PULSE GENERATOR (NIM PULSE PAIR)	215	JORWAY	1	//5		14,1213
	8 CHANNEL DELAY GENERATOR (DELAY 0 TO 99 TIMES CLOCK, DELAYS CASCADABLE)	220	JORWAY	1	//4	(11)	14,1214
N	SERIAL OUTPUT REGISTER (12/16/24 BIT, SCALER OR SHIFT REG, INT, 100HZ & 1MHZ)	CAM 2,11	METRIMPEX	1	//3		14,1215
	DUAL PROGRAMMED PULSE GENERATOR(50HZ/ 2KHZ/5MHZ PULSE TRAIN,LENGTH BY COMMAND)	2PPG 2016	SEN	1	//1		14,1216

132 Parallel Output Registers (TTL, HTL, NIM etc.)

	OPTICAL ISOLATED OUTPUT REGISTER	3601	BI HA SYSTEMS	1	//4		14,1217
	12 BIT PARALLEL OUTPUT REGISTER (NIM)	3251	BI HA SYSTEMS	1	//3		14,1218
	15 BIT PARALLEL OUTPUT REGISTER (BIT ADDRESSABLE, NIM LEVELS OR PULSES)	C 343	INFORMATEK	1	//3		14,1219
	12 BIT OUTPUT REGISTER(DC OR PULSE O/P, UPDATING STROBE OUTPUT,NIM LEVELS)	41	JORWAY	1	//1	(2)	14,1220
	OUTPUT REGISTER (12BIT, NIM PULSES OR LEVELS OUT)	OR 2027	SEN	1	//0		14,1221
	OUTPUT REGISTER (12BIT)	PR 312	STND ENGINEERING	1	//3		14,1222
	DIFFERENTIAL OUTPUT REGISTER	3030	KINETIC SYSTEMS	1	//2	(8)	14,1223
	OUTPUT REGISTER (12 CHANNEL)	OR 612	STND ENGINEERING	1	//3		14,1224
	OUTPUT REGISTER (24BIT TTL VIA SPEC CONN 8BIT ALSO VIA FRONT PANEL LEMO)	FHC 1309	FRIESEKE	1	//2		14,1225
N	PARALLEL OUTPUT REGISTER (24BIT, OUTPUT WITH CAMAC STANDARD)	CAM 2,12-3	METRIMPEX	1	//3		14,1226
	OUTPUT REGISTER (24 BIT, 16 MA 5V OUT)	9600A	NUCL, ENTERPRISES	0		(13)	14,1227
	OUTPUT REGISTER (24BIT,OPTO-COUPLER,7MA)	9603	NUCL, ENTERPRISES	0		(13)	14,1228
	OUTPUT REGISTER (24BIT WORD, TTL O/P VIA 37-WAY CONN)	351	PULON	1	//3		14,1229
	OUTPUT REGISTER (24BIT)	PR 314	STND ENGINEERING	1	//3		14,1230
	PARALLEL OUTPUT REG, (24BIT,NEG/OPT POS TTL,ADJ, DURATION&LEVEL,4 TIMING MODES)	C-OC-24	WENZEL ELEKTRONIK	1	//3	(10)	14,1231
	DUAL 16BIT PARALLEL OUTPUT REGISTER(TTL)	3212	BI HA SYSTEMS	1	//3		14,1232
	DUAL 16 BIT OUTPUT REGISTER (SELECTABLE O/P STAGES ON PLUGABLE PC, FP CONNECTOR)	2OR 2051	SEN	1		(9)	14,1233
	DUAL 24 BIT PARALLEL OUTPUT REGISTER	3222	BI HA SYSIEMS	1	//3		14,1234
	OUTPUT REGISTER (2X24BIT DATA OUT,DATA-READY + BUSY FORM HANDSHAKE, TTL)	RO-224	EG&G/ORTEC	1	//2		14,1235

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	OUTPUT REGISTER (2X24BIT OR 6X8BIT, LED DISPLAY)	OR	JOERGER	1	//2	(7)	14,1236
	24-BIT DUAL OUTPUT REGISTER	9042	NUCL, ENTERPRISES	1	//2	(7)	14,1237
	DUAL OUTPUT REGISTER (2X24BIT, DATAWAY READ AND WRITE, HANDSHAKE CONTROL, LO=Z)	9043A	NUCL, ENTERPRISES	1		(7)	14,1238
	(SAME BUT HI=Z)	9043B		1		(7)	
	PARALLEL OUTPUT REGISTER (2X24 BITS)	J RS 10	SCHLUMBERGER	1	//3	(7)	14,1239
	DUAL 24 BIT PARALLEL OUTPUT REGISTER (WITH LED DISPLAY OPTION)	PR-612	STND ENGINEERING	1	//1	(6)	14,1240
	DIGITAL OUTPUT REGISTER (4X8BIT PARALL OUTPUT REGISTER,NO L,TTL,1=H)	DO 200-2501	DORNIER	1	//1		14,1241
	(WITH FRONT PANEL CONNECTOR)	DO 200-2701		1	//2		
	(MODULE WITH ONLY LOGIC BOARD)	DO 200-2500		1	//3		
	DIGITAL OUTPUT REGISTER (4X8BIT PARALLEL OUPTPUT REGISTER, HLL 12V)	DO 200-2505	DORNIER	1	//3		14,1242
	(SAME WITH FRONT PANEL CONNECTOR)	DO 200-2705		1	//3		
	(SAME, NO F.P. CONNECTOR, INVERTING)	DO 200-2506		1	//3		
	(SAME WITH FRONT PANEL CONNECTOR)	DO 200-2706		1	//3		
	DIGITAL OUTPUT REGISTER (4X8BIT PARALLEL OUPTPUT REGISTER, HLL 24V)	DO 200-2507	DORNIER	1	//3		14,1243
	(SAME WITH FRONT PANEL CONNECTOR)	DO 200-2707		1	//3		
	(SAME, NO F.P. CONNECTOR, INVERTING)	DO 200-2508		1	//3		
	(SAME WITH FRONT PANEL CONNECTOR)	DO 200-2708		1	//3		
	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				14,1244
N	QUAD 24 BIT OUTPUT REGISTER (4X24, HAND-SHAKE DATA TRANSFER, PROG. O/P POLARITY)	QDR	JOERGER	1	09/75	(14)	14,1245
	128 BIT OUTPUT REGISTER (ADDRESSABLE AS 8 16BIT OR 128 1-BIT WORDS)	C 342	INFORMATEK	1	//3		14,1246

133 Parallel Output Drivers (Open Coll., Relay etc.)

	TRIAC OUTPUT REGISTER (8 BITS, 2 AMPS, ZERO VOLTAGE SWITCHING)	LT	JOERGER	1	//4	(13)	14,1247
N	12 BIT OUTPUT REGISTER (RELAY CONTACTS, SELECTIVE SET/CLEAR LAM GENERATION)	240	JOHWAY	1	//5		14,1248
	8 CHANNEL TIMED TRIAC OUTPUT	3040	KINETIC SYSTEMS	2	//4	(13)	14,1249
	8 BIT TRIAC OUTPUT REGISTER	3080	KINETIC SYSTEMS	1	//3		14,1250
	12-BIT OUTPUT REGISTER (WITH OPTICAL ISOLATION,OPEN COLL O/P, MAX 30V/100MA)	3082	KINETIC SYSTEMS	1			14,1251
	12-BIT OUTPUT REGISTER WITH ISOLATED RELAY	3087	KINETIC SYSTEMS	1	//1	(4)	14,1252
	DRIVER (16BIT,OPEN COLLECTOR OUTPUT VIA MULTIWAY CONNECTOR,MAX 150MA/LINE)	9002	NUCL, ENTERPRISES	1	//1		14,1253
	OUTPUT REGISTER (16BIT, 48V/,05A MAX, 2X37-WAY O/P CONN)	360	PULON	1	//3		14,1254
	OUTPUT REGISTER (16BIT,250V/,1A MAX, 2X37-WAY O/P CONN)	360A		1	//3		
	(SAME, 25V/1A MAX)	360B		1	//3		
N	16-BIT OUTPUT REGISTER (ISOLATED RELAY CONTACTS & LATCHBACK INPUT)	3094	KINETIC SYSTEMS	1	//4		14,1255
	RELAY DRIVER (16 WAY RELAY OUTPUT)	J RD 10	SCHLUMBERGER	1	//3	(8)	14,1256
	PARALLEL OUTPUT REGISTER (16BIT REED RELAY,MAX SWITCHED PWR 10W,4 TIMING MODES)	C-OR-16	WENZEL ELEKTRONIK	1	//2	(10)	14,1257
N	PARALLEL OUTPUT REGISTER (24BIT, OUTPUT WITH OPEN COLLECTOR, EXT, 30V/100MA)	CAM 2,12-1	METRIMPEX	1	//3		14,1258
N	PARALLEL OUTPUT REGISTER (24BIT, OUTPUT WITH OPEN COLLECTOR, TTL)	CAM 2,12-2	METRIMPEX	1	//3		14,1259
	DRIVER (24BIT OUTPUT REGISTER,SET AND READ BY COMMAND,24BIT I/P DATA ACCEPTED)	9017	NUCL, ENTERPRISES	1	//1	(1)	14,1260
	OUTPUT REGISTER (24 BIT, 40 MA 30V OUT)	9600B	NUCL, ENTERPRISES	0		(13)	14,1261
	(SAME INVERTED OUTPUTS)	9600C		0		(13)	
	OUTPUT REGISTER (24 BIT, 1 AMP 60V OUT)	9601	NUCL, ENTERPRISES	0		(13)	14,1262
	(SAME WITH RELAY CONTACTS, MUX CONCEPT)	9602A		0		(13)	
	(SAME WITH RELAY CONTACTS,FREE CONTACTS)	9602B		0		(13)	
	OUTPUT REGISTER (2X16BIT,OPEN COLLECTOR)	1084	BUHER	1	//4		14,1263
	OUTPUT DRIVER(2X16BIT,40MA SINKING,1=LO, DATAWAY READ & WRITE,LAM I/P,STRUBE O/P)	OD 1613	GEC-ELLIOTT	1	//2		14,1264
	(SAME, 1=HI)	OD 1614		1	//2		
	OUTPUT DRIVER(2X16BIT,125MA SINKING,1=LO DATAWAY READ & WRITE,LAM I/P,STRUBE O/P)	OD 1617	GEC-ELLIOTT	1	//2		14,1265
	(SAME, 1=HI)	OD 1618		1	//2		

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	OUTPUT DRIVER(2X16BIT,TOTEMPOLE,30 LOADS DATAWAY READ & WRITE,LAM I/P,STROBE O/P)	OD 1620	GEC-ELLIOTT	1	//2		14,1266
	2X16 OR 4X8 BIT OUTPUT REGISTER	J RS 30	SCHLUMBERGER	1	//4	(11)	14,1267
	DUAL 16 BIT OUTPUT REGISTER (TTL LEVELS, OPEN COLL OUTPUTS VIA CABLE)	20R 2008	SEN	1	//0		14,1268
	DUAL OUTPUT DRIVER (200MA SINKING,24V)	2UR 2051MC	SEN	1		(9)	14,1269
	DUAL OUTPUT DRIVER (HI VOLTAGE DRIVER)	2UR 2051HV	SEN	1		(9)	14,1270
	DIGITAL OUTPUT (2X16BIT, MAX 30V)	C 76451-A9-A4	SIEMENS	1	//3	(6)	14,1271
	OUTPUT REGISTER (2X16BIT VIA ISOLATING CONTACTS)	1082	BORER	1	//2	(4)	14,1272
	DIGITAL OUTPUT (2X16BIT RELAYS)	C 76451-A9-A3	SIEMENS	1	//3	(6)	14,1273
	PARALLEL-OUTPUT-REGISTER (DUAL 24BIT, OR QUAD 12BIT,OPEN COLLECTOR OUTPUT)	MS PU 1 1230/1	AEG-TELEFUNKEN	1	//0	(1)	14,1274
	PARALLEL-OUTPUT REGISTER (24BIT, OPEN COLLECTOR OUTPUT, HANDSHAKE FACILITY)	MS PU 2 1230/1	AEG-TELEFUNKEN	1	//2	(4)	14,1275
	OUTPUT DRIVER(2X24BIT,40MA SINKING,1=LO, DATAWAY READ & WRITE,LAM I/P,STROBE O/P)	OD 2403	GEC-ELLIOTT	1	//2		14,1276
	(SAME, 1=HI)	OD 2404		1	//2		
	OUTPUT DRIVER(2X24BIT,125MA SINKING,1=LO DATAWAY READ & WRITE,LAM I/P,STROBE O/P)	OD 2407	GEC-ELLIOTT	1	//2		14,1277
	(SAME, 1=HI)	OD 2408		1	//2		
	OUTPUT DRIVER(2X24BIT,TOTEMPOLE,30 LOADS DATAWAY READ & WRITE,LAM I/P,STROBE O/P)	OD 2410	GEC-ELLIOTT	1	//2		14,1278
	DUAL OUTPUT REGISTER (2X24BIT, OPEN COLL O/P, FULL LAM, OUTPUT STROBES)	200-2	HYTEC	1	//3		14,1279
	OUTPUT REGISTER (2X24BIT OR 6X8BIT, 250MA SINKING, DIODE CLAMPED)	OR-1	JUERGER	1	//3		14,1280
	DUAL 24 BIT OUTPUT REGISTER(DC OR PULSE O/P,UPDATING O/P STROBE,TTL OPEN COLL)	40	JORWAY	1	//1	(2)	14,1281
	DUAL 24 BIT OUTPUT REGISTER (DC OR PULSE O/P UPDATING, 300MA SINK, DIODE CLAMPED)	40-2	JORWAY	1	//4		14,1282
	DUAL 24-BIT OUTPUT REGISTER (OPEN COLL DRIVERS, MAX 24V OR 250MA, REAR OUTPUTS)	3072	KINETIC SYSTEMS	1			14,1283
	DIGITAL OUTPUT REGISTER (4X8BIT PARALLEL OUTPUT REGISTER,NO L,OPEN COLL O/P,1=HI)	DO 200-2502	DORNIER	1	//2		14,1284
	(SAME WITH FRONT PANEL CONNECTOR, 1=HI)	DO 200-2702		1	//2		
	(SAME, NO F.P. CONNECTOR, 1=LO)	DO 200-2503		1	//2		
	(SAME WITH F.P. CONNECTOR, 1=LO)	DO 200-2703		1	//2		
	DIGITAL OUTPUT REGISTER WITH REED RELAYS (4X8BIT OUTPUT REG,OPEN CONTACT=0)	DO 200-2504	DORNIER	1	//1		14,1285
	(WITH FRONT PANEL CONNECTOR)	DO 200-2704		1	//1		
	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				14,1286

14 Digital I/O, Peripheral and Instrumentation Interfacing modules — Serial and Parallel I/O Regs, Printer-, Tape-, DVM-, Plotter- and Analyser Interfaces, Step-Motor Drivers, Supply CTR, Displays

141 Serial Input/Output Modules (General Purpose)

	SERIAL INPUT/OUTPUT REGISTER 16BIT CODED	9063	NUCL. ENTERPRISES	1	//4	(13)	14,1287

142 Parallel I/O Registers (General Purpose)

N	UNIVERSAL INPUT/OUTPUT REGISTER (2X16BIT INPUT, 1X16BIT OUTPUT, RELAYS OPTIONAL)	1031A	BORER	1	0//75		14,1288
N	INPUT RELAY ADAPTER (24BIT I/P RELAY COILS, O/P TO CAM 2,05/CAM 2,09)	CAM 8,02-1	METRIMPEX	2	//75		14,1289
N	OUTPUT RELAY ADAPTER (24BIT, I/P RELAY COILS TO CAM 2,12-1, RELAY CONTACTS O/P)	CAM 8,02-2	METRIMPEX	2	//75		14,1290
N	OPTOISOLATOR (24 INPUTS, OUTPUTS MAY BE CONNECTED TO CAM 2,05/CAM 2,09	CAM 8,09-1	METRIMPEX	2	//4		14,1291
C	UNIVERSAL INPUT/OUTPUT REGISTER	9066	NUCL. ENTERPRISES	1	01//5		14,1292
	16 BIT INPUT/OUTPUT REGISTER (O/P STAGES ON PLUGABLE PC, FP CONNECTOR)	IUR 2053	SEN	1	//4	(11)	14,1293
	INPUT/OUTPUT REGISTER (24 BITS IN, 12 BITS OUT, OPTICALLY COUPLED)	IUR-1	JUERGER	1	//4	(11)	14,1294
	INPUT/OUTPUT REGISTER (24BIT)	IU 302	STND ENGINEERING	1	02//5		14,1295
	INPUT/OUTPUT REGISTER (24BIT, INTEGRATED INPUT, OUTPUT STROBES, FULL LAM)	210	HYTEC	1	0///5		14,1296

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	INPUT/OUTPUT REGISTER (24 BIT, POS & NEG LOGIC O/P SINKING 450 MA)	9048	NUCL, ENTERPRISES	1			14,1297
	DUAL INPUT DUAL OUTPUT REGISTER (16BIT, TTL IN, OPEN COLL TTL OUT, MAX 40MA,30V)	C110	MDT	1	//2		14,1298
	INPUT/OUTPUT REGISTER(2X24BIT IN,2X12BIT OUT, 3 ENTRY MODES, LED DISPLAY)	IR-1	JOERGER	1	//2	(/)	14,1299
	BUFFER STORE/REGISTER (32X24BIT,WITH EXTERNAL ADDRESSING FACILITY)	104	MYTEC	1			14,1300
	(SAME, 32X24BIT, WITHOUT EXT ADDR)	100		1			
	(SAME, 32X16BIT, WITHOUT EXT ADDR)	101		1	//2		
	BUFFER STORE/REGISTER (32X16BIT, WITH EXTERNAL ADDRESSING FACILITY)	105	MYTEC	1			14,1301
	(SAME, 16X24BIT, WITHOUT EXT ADDR)	102		1	//2		
	(SAME, 16X16BIT, WITHOUT EXT ADDR)	103		1	//3		

143 Peripheral Interfacing Modules (For TTY, Tape etc.)

	DESK CALCULATOR CTRL (DIEHL INTERFACE TO FHC 1301/02/11 AND FHC 1309)	FHC 1312	FRIESEKE	1	//2		14,1302
	INTERFACE FOR ASR33 TTY,SERIAL DATA LINK	6711	BI RA SYSTEMS	1	//4		14,1303
	TELETYPE O/P CTRL (10 FHC 1301/02/11 AND FHC 1309 VIA SPEC CONN,TTY MOTOR ON/OFF)	FHC 1307	FRIESEKE	1	//1		14,1304
	TELETYPE INTERFACE	90	JORWAY	2	//1		14,1305
N	SERIAL DRIVER/RECEIVER (TTY, TTX & MODEM INTERFACE, V24 CCITT STANDARD)	CAM 3,04	METHIMPEX	1	//5		14,1306
	TELETYPEWRITER INTERFACE(I/O DATA TRANSF AND CONTROL,LAM USED AS TWO-WAY FLAG)	7061-1	NUCL, ENTERPRISES	1	//0	(1)	14,1307
	TELETYPE INTERFACE (FOR ASR 33, SER I/O)	500	POLON	1	//4		14,1308
	TERMINAL DRIVER	J TY 20	SCHLUMBERGER	1	//3	(11)	14,1309
	TELETYPE OR CRT INTERFACE	TCU 100	STND ENGINEERING	1	//4		14,1310
	VERSATEC LINE PRINTER INTERFACE	3320	KINETIC SYSTEMS	1	//2		14,1311
	INTERFACING OUTPUT UNIT(8BIT DATA, CONTR & STATUS REGS, FOR FACIT SP1 INTERFACE)	SP1/ACCEPTOR	ARSYCOM	1	//4	(12)	14,1312
	PAPER TAPE PUNCH INTERFACE, COUPLES TO FACIT 4070,DATA DYNAMICS,RACAL DIGISTORE	TP 0801	GEC-ELLIOTT	1	01//5	(1)	14,1313
	INTERFACING INPUT UNIT (8BIT DATA/STATUS & CONTR REGS, FOR FACIT SP1 INTERFACE)	SP1/SOURCE	ARSYCOM	1	//4	(12)	14,1314
	PAPER TAPE READER INTERFACE (COUPLES TO LINWOOD, TREND, & RACAL DIGISTORE)	TR 0801	GEC-ELLIOTT	1	01//5	(1)	14,1315
	MAGNETIC TAPE INTERFACE (TAPE DECKS OR CASSETTES)	CS 0042	NUCL, ENTERPRISES	1	//3	(8)	14,1316
	CASSETTE INTERFACE (READS & WRITES BY 8 OR 16BIT WORDS, 8BIT LAM REG) CONTROLS--	J CK 10	SCHLUMBERGER	1	//5	(12)	14,1317
	CASSETTE DRIVER FOR 1 CASSETTE	C CK 10			//5	(12)	
	CASSETTE DRIVER FOR 2 CASSETTES	C CK 11			//5	(12)	
	PORTABLE CASSETTE DRIVER(FOR 1 CASSETTE)	P CK 10	SCHLUMBERGER		//5		14,1318
	DISK DRIVE FOR CDS-110	9370	NUCL, ENTERPRISES	NA		(13)	14,1319
	INTERFACE FOR DISK DRIVE	9370		0		(13)	
	UNIVERSAL ASYNCHRONOUS TRANSMITTER/RECEIVER (129 CHAR,BUFFER)	C 317	INFORMATEK	1	//3		14,1320
	PERIPHERAL READER(8BIT PARALLEL DATA IN, NEG OR POS TTL,HANDSHAKE CONTROLS)	7064-1	NUCL, ENTERPRISES	1	//1	(1)	14,1321
	PERIPHERAL DRIVER (8BIT DATA OUT,NEG OR POS TTL,HANDSHAKE CONTROLS)	7065-1	NUCL, ENTERPRISES	1	//1	(1)	14,1322

144 Display Modules, Display and Plotter Interfacing

	24 BIT LED BCD DISPLAY (ONE FHC 1301/02/11 VIA SPEC CONNECTOR)	FHC 1305	FRIESEKE	1	//1	(1)	14,1323
	24 BIT NIXIE BCD DISPLAY (SELECTS ONE OF 10 FHC 1301/02/11 VIA SPEC CONNECTION)	FHC 1306	FRIESEKE	2	//1	(1)	14,1324
	24 BIT LED BINARY DISPLAY (ONE FHC 1313 OR FHC 1309 VIA SPECIAL CONNECTION)	FHC 1315	FRIESEKE	1	//2		14,1325
N	DISPLAY UNIT (8CMX10CM CRT, INPUTS- X,Y- +&-5V, Z- 5V)	CAM 3,01	METHIMPEX	12	//3		14,1326
N	DISPLAY DRIVER (FOR CAM 3,01)	CAM 3,02	METHIMPEX	3	//3		14,1327
N	24 BIT DECIMAL DISPLAY (6 SYMBOLS 0,1, ...,9,A,B, ...,F)	CAM 3,08	METHIMPEX	1	//4		14,1328

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	DECIMAL DISPLAY UNIT (ADDRESS AND 5 DATA DECADES + MULTIPLIER DISPLAYED)	9007	NUCL. ENTERPRISES	NA	/71		14,1329
	DISPLAY CONTROLLER (FOR 9007, INCLUDES BIN TO DECIMAL CONVERTER)	9006		2	/71		
	COLOUR DISPLAY INTERFACE	9062	NUCL. ENTERPRISES	NA	04/75	(12)	14,1330
	EXTERNAL DISPLAY FOR J EA 10 SCALER	C AE 10	SCHLUMBERGER	NA	/73		14,1331
	SCALER DISPLAY THROUGH COMPUTER (DISPLAY OF 24BIT WORD, 30MHZ)	J AF 15	SCHLUMBERGER	2	/71		14,1332
	MANUAL BINARY DISPLAY (CONTENT OF A REGISTER DISPLAYED, EXT MULTIWAY CONN)	J AF 20	SCHLUMBERGER	1	/71		14,1333
	GRAPHIC DISPLAY DRIVER FOR HP1311/TEK604	4301	BI RA SYSTEMS	1	/74		14,1334
	GRAPHIC DISPLAY DRIVER FOR STORAGE DISPLAY TEK 602	4301A	BI RA SYSTEMS	2	/74		14,1335
	INTERACTIVE GRAPHICS DISPLAY PROCESSOR 128 CHARACTERS, 9X7 DOT MATRIX, 4 SIZES, VECTORS, ARCS, CIRCLES IN THREE LINE TYPES LIGHT PEN & TRACKER BALL INPUTS, 32 CONTROL INSTRUCTIONS, BUILT IN 4K STORE,	DP 1603 DP 1603A DP 1603B	GEC-ELLIOTT	4 2 2	09/75		14,1336
	CRT DECIMAL DISPLAY SYSTEM (INCLUDING) DISPLAY DRIVER	72A 72A	JURRAY	NA 5	/71	(2)	14,1337
	DISPLAY SYSTEM COMPRISING		KINETIC SYSTEMS		/71	(4)	14,1338
	DISPLAY SYNCHRONIZING (COMPATIBLE WITH 60HZ 525 LINE MONITORS)	3200		1	/71		
	DISPLAY SYNCHRONIZING (COMPATIBLE WITH 50HZ 625 LINE MONITORS)	3200E		1	/74	(12)	
	DISPLAY TIMING	3205		1	/71		
	DISPLAY CONTROL	3210		1	/71		
	DISPLAY REFRESH (ALPHANUMERIC + GRAPHS)	3212		1	/71		
	DUAL LIGHT PEN INTERFACE	3225		1	/72		
N	PROGRAMMABLE DISPLAY SYSTEM	3232		4	10/75		
	COLOR MONITOR	RGB 5200 M			/71		
	STORAGE DISPLAY DRIVER	3260		1	/72		
	DISPLAY DRIVER (TWO 10BIT DAC, OUTPUT RANGE +5V TO -5V, TWO OPERATION MODES)	7011-2	NUCL. ENTERPRISES	2	/70	(1)	14,1339
	STORAGE OSCILLOSCOPE (DRIVER FOR TEKTRONIX 611 OR 601, USED WITH 7011)	9028	NUCL. ENTERPRISES	1	/71	(2)	14,1340
	SCOPE DISPLAY DRIVER MANUAL CONTROL OF J DD 10	J DD 10 MC 10	SCHLUMBERGER	2 NA	/73	(7)	14,1341
	SCOPE DISPLAY DRIVER X-Y-Z (SYSTEM) STORAGE DISPLAY DRIVER FOR TEKTRONIX 611 OR 601	FDD 2012 SDD 2015	SEN	1 1	/71 /71	(1) (1)	14,1342
	CHARACTER GENERATOR	CG 2018		1	/71	(1)	
	VECTOR GENERATOR	VG 2028		1	/71	(1)	
	LIGHT PEN FOR FDD 2012 OR CG 2018	LP 2035			/71		
N	LIGHT PEN (INCLUDES TRIGGER SWITCH)	EC397	SENSION				14,1343
N	LIGHT PEN PROCESSOR	EC396		1	/75		
N	PLOTTER DRIVER (2X10BIT, X,Y OUT +& - 2,5MV)	CAM 3,03	METRIMPEX	3	/73		14,1344
	PLOTTER DRIVER	J XY 10	SCHLUMBERGER	1	/73	(8)	14,1345
N	X-Y RECORDER DRIVER	XY 2074	SEN	1		(14)	14,1346

145 Instrumentation Interfacing Modules (DVM, Supply CTR, Stepping Motor Drivers, Pulse Analyser CTR)

DUAL 15 CHANNEL SERIAL OUTPUT MODULE (STEPPER MOTOR CONTROLLER, TTL)	3101	BI RA SYSTEMS	2	/73		14,1347
STEP MOTOR DRIVER (MAX 32768 STEPS, RATE, ROTATION AND START/STOP FULLY COMMANDED)	1161	BURER	1	/72	(3)	14,1348
STEPPING MOTOR CONTROLLER & DRIVER (ADJUSTABLE ACCEL/DECEL, TIME & MAX FREQ)	SMC	JOERGER	1	/74	(13)	14,1349
STEPPING MOTOR CONTROLLER, DUAL	3360	KINETIC SYSTEMS	1	/72	(4)	14,1350
STEPPING MOTOR CONTROLLER, ACCELERATING	3361	KINETIC SYSTEMS	1	/73		14,1351
STEPPING MOTOR DRIVER SUPPLY FOR J CP 20	J CP 20 C APP 10	SCHLUMBERGER	1	/74 /74	(9)	14,1352
CONTINUOUS STEPPER CONTROL (65536 STEPS, POSITION/DIRECT./SPEED/ACCELER. CONTROL)	C-ST-4	WENZEL ELEKTRONIK	2	/72		14,1353
INCREMENTAL STEPPER CONTROL(65536 STEPS, POSITION/DIRECT./SPEED/ACCELER. CONTROL)	C-ST-4-I	WENZEL ELEKTRONIK	2	/72		14,1354
VARIABLE PULSE DURATION TRIAC OUTPUT MODULE	3701	BI RA SYSTEMS	2	/74		14,1355
TRIAC OUTPUT REGISTER (8 BITS, 2 AMPS, ZERO VOLTAGE SWITCHING)	LT	JOERGER	1	/74	(13)	14,1356

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	POWER SUPPLY CONTROLLER 12-BIT	3158	KINETIC SYSTEMS	1	/73		14,1357
	CAMAC-TO-SCIPP PHA INTERFACE	2323	BI HA SYSTEMS	2	/73		14,1358
	INTERFACE CAMAC-TO-LABEN 8000SERIES MULTICHANNEL ANALYZERS	5380	LABEN	3		(12)	14,1359
	ADC-CAMAC INTERFACE (FOR PULSE ADC 8215, 8210,8211,8212,8112 & T-U-F CONV 8270)	5910	LABEN	1		(12)	14,1360
	MULTICHANNEL ANALYZER - CAMAC INTERFACE (FOR PACKARD 9000 AND 900 SERIES MCA)	9701	PACKARD	3		(4)	14,1361
	SYNCHRO TO DIGITAL CONVERTER (SINGLE AND MULTI-TURN CAPABILITIES)	SDC	JUERGER	2	/73	(13)	14,1362
	DUAL SYNCHRO-DIGITAL CONVERTER (14BIT)	CS 0047	NUCL, ENTERPRISES	2	/73		14,1363
	DUAL INCREMENTAL POSITION ENCODER (2X20 BIT X-Y DIGITIZATION BY UP-DOWN COUNTER)	2IPE 2019	SEN	1	/71		14,1364
	INTERFACE FOR MEASURING DEVICES (DUAL INPUT FOR 2 INSTRUMENTS)	DU 200-1412	DORNIER	1	/74	(10)	14,1365
	OUTPUT REGISTER (16 OR 24 BIT TTL DRIVER FOR FAST-ROUTING MULTIPLEXER SYSTEM)	CM 665	J AND P	1	/71		14,1366
	PULSE DURATION DEMODULATOR	3720	KINETIC SYSTEMS	1	/73		14,1367
	PLUMBICON READ OUT TERMINAL	J PG 10/PUDDING	SCHLUMBERGER	1	/71	(6)	14,1368
	PLUMBICON READ OUT (5 SCALERS RECORD DIGITIZED OUTPUTS FROM PLUMBICON CAMERA)	J PM 10/PLUM	SCHLUMBERGER	1	/71	(6)	14,1369
	SPARK CHAMBER READ OUT	J SC 10		2	/72		
N	INTERFACE FOR DIGITAL PROCESSING SCOPES WP1051, WP2051 & WP2052		TEKTRONIX	0			14,1370
	ADC/CAMAC INTERFACE (FOR ANY ADC,2X16BIT O/P BUFFER,STATUS,LAM HANDL,CLOCK TIME)	C-A1-2	WENZEL ELEKTRONIK	1	/73	(10)	14,1371
N	ISOLATED ON-OFF CONTROLLER FOR 16DEVICES 5 CONTROL-LINES/DEV,,1-SEC-FAILURE-TEST)	C-PC-16	WENZEL ELEKTRONIK	1	08/75	(14)	14,1372

147 Other Digital I/O Modules (Incl. Data Links)

	CAMAC DATA LINK MODULE (16 BIT PARALLEL,ASYNCHRONOUS DATA LINK)	6701	BI HA SYSTEMS	2	/73		14,1373
	BIT-SYNCHRONIZER - HARDWARE PROGRAMABLE 0 TO 10V INPUT, PCM-SIGNAL IN SERIES	DU 200-2251	DORNIER	3	/73		14,1374
	FORMAT-SYNCHRONIZER (IDENT & S/P OF DATA WORDS, SOFT- & HARDWARE PROGRAMMABLE)	DU 200-2260	DORNIER	4	/73		14,1375
	COMMUNICATION INTERFACE (V24/V23/V21 MODEM INTERFACE WITH AUTO-DIAL OPTION)	DU 200-2911	DORNIER	1	/73	(10)	14,1376
	START-STOP CONTROLLER(START,STOP,RESET, MANUAL OR DATAWAY CONTROL, 100HZ CLOCK)	FMC 1304	FRIESEKE	1	/71	(1)	14,1377
N N	COMMUNICATION INTERFACE COMMUNICATION INTERFACE W/ BUFFER	3340 3340B	KINETIC SYSTEMS	1 1	/75 /75		14,1378
N	SERIAL DRIVER/RECEIVER (TTY, TTX & MODEM INTERFACE, V24 CCITT STANDARD)	CAM 3,04	METRIMPEX	1	/75		14,1379
	SERIAL INTERFACE (V24 SPEC, QUAD VERSION VARIABLE TRANSMISSION RATES)	9045	NUCL, ENTERPRISES	1	/73	(13)	14,1380
N	SERIAL INTERFACE (VARIABLE TRANSMISSION RATE)	9046	NUCL, ENTERPRISES	1	09/75		14,1381
	START-STOP UNIT (START, STOP CLOCK AND GATE OUTPUTS)	J AM 10	SCHLUMBERGER	1	/71		14,1382
	FOUR FOLD BUSY DONE (START SIGNAL INITIATED BY COMMAND,DEVICE RETURNS LAM)	4BD 2021	SEN	1	/71		14,1383
N	DATA TRANSMISSSION MODULE (50BD TO 9,6KB SYNC/ASYNC, V24, USE WITH 0326)	0350	SENSIUN	1	/75		14,1384

15 Digital Handling and Processing Modules — and/or/nor Gates, Fan-Outs, Digital Level and Code Converters, Buffers, Delays, Arithm. Processors etc.

151 Fan-Outs, and/or/not-Gates

	FAN-OUT UNIT (2 ORED INPUTS PROVIDE 8 TRUE,2 COMPLEM OUTPUTS,NIM SIGNALS)	FO 0801	GEC-ELLIOTT	1	/71		14,1385
	NIM FANOUT (DUAL FOUR FOLD & COMPLEMENT, NIM DRIVER, -14MA INTO 50OHMS)	FON	JUERGER	1	/73		14,1386
C	TTL FANOUT (DUAL FOUR FOLD & COMPLEMENT, TTL DRIVER, 50MA CURRENT SINK)	FOT	JUERGER	1	/73	(14)	14,1387

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	NIM FANOUT (7=ORED INPUTS, 8 O/P+2 COMPL O/P GATED FROM DATAWAY)	216	JORWAY	1	//75		14,1388
	FAN OUT MODULE (IL2 I/P, 16 IL2 O/P)	9050	NUCL, ENTERPRISES	1	//73		14,1389
	SIX=FOLD CONTROLLED GATE (INDIV GATING, FAN=IN AND FAN=OUT CONTROLLED BY 3 REGS)	6CG 2017	SEN	1	//71	(4)	14,1390
	FAST LOGIC UNIT (4X4 NIM INPUTS)	FLU 2062	SEN	1		(12)	14,1391
	152 Digital Level Converters						
	6 CHANNEL TTL/NIM CONVERTER	5601	BI RA SYSTEMS	1	//73		14,1392
	6 CHANNEL NIM/TTL CONVERTER	5602	BI RA SYSTEMS	1	//73		14,1393
C	HEX CONVERTER (NIM TO TTL LEVELS PLUS TWO COMPLEMENT OUTPUTS)	CNT	JOERGER	1	//73	(14)	14,1394
C	HEX CONVERTER (TTL TO NIM LEVELS PLUS TWO COMPLEMENT OUTPUTS)	CTN	JOERGER	1	//73	(14)	14,1395
	HEX IL1 TO IL2 CONVERTER (6 TTL SIGNALS IN,6 NIM SIGNALS OUT)	7052=1	NUCL, ENTERPRISES	1	//70		14,1396
	153 Code Converters						
	DECIMAL INPUT 6 NUMBERS 3 DIGITS CODE CONVERTER	DD 200=2005	DORNIER	2	//74		14,1397
	(SAME BUT 3 NUMBERS)	DD 200=2006		2	//74		
	CAMAC BCD=TO=BINARY CONVERTER	LEM=52/5,7	EISENMANN	1			14,1398
	CAMAC BINARY=TO=BCD CONVERTER WITH DECIMAL DISPLAY	LEM=52/5,8	EISENMANN	1			14,1399
	GRAY CODE TO BCD CONVERTER (DUAL CHANNEL INPUT WITH MEMORY)	EIR	JOERGER	1	//74		14,1400
	BINARY CODE CONVERTER(BIN=BCD OR BCD=BIN CONVERSION, DATA FROM DATAWAY OR FRONT)	9044	NUCL, ENTERPRISES	1		(7)	14,1401
	BINARY TO DECIMAL CODE CONVERTER (24 BIT BINARY TO 8 DECADE)	610	POLON	1	//74		14,1402
	BCD TO BINARY CONVERTER (29BIT BCD TO 24BIT BINARY, CONV TIME 325 NSEC)	CD 001	STND ENGINEERING	1	//73	(12)	14,1403
	BINARY TO BCD CONVERTER (CONV TIME 325 NSEC,24BITS TO MAX 16777216=1 BCD CODED)	CD 002	STND ENGINEERING	1	//73	(12)	14,1404
	BINARY TO BCD=CONVERTER(24BIT TO 8 DECA= DE,DISPLAY,CONV 40SEC,TTL LEVEL OUT,1=M)	C=BBC=24	WENZEL ELEKTRONIK	2	//71		14,1405
	154 Buffer Memories, Storage Units						
	PROGRAM STORE/REGISTER (256X24BIT RAM + 64X24BIT ROM, EXT ADDR, USE WITH 7025=2)	110A	HYTEC	1			14,1406
	(SAME BUT WITHOUT EDIT ROM)	110		1			
	(SAME BUT NO BUFFER AND NO EXT ADDR)	112		1	//73		
	1024 WORD 24 BIT STATIC STORE (NORMAL & BYTE MODES, CLEAR, INCR, DECR, READ, & OVERWRITE ON ADDRESS REG ARE PERFORMED)	130	HYTEC	1	07//75		14,1407
	(SAME WITH MEMORY ACCESS ALSO FROM FRONT PANEL, MASTER/SLAVE OPERATION)	131		2	08//75		
	3=DECADE ADC & 16=WAY MUX (PRESET X1=X10 AMPL, 16X24 STORE, 100USEC/CH UPDATE)	500=1	HYTEC	1	//73		14,1408
	(SAME AS 500=1 BUT WITH 8=WAY MUX)	502		1	//74		
	(SAME BUT BINARY ADC)	501		1	//74		
	(SAME AS 501 BUT WITH 8=WAY MUX)	503		1	//74		
	(SAME, BUT AMPL GAIN CAN BE SET AND STORED INDIVIDUALLY/CHANNEL, BCD/BIN)	510		2	//74		
	256 WORD FIFO BUFFER (24 BITS PER WORD)	3841	KINETIC SYSTEMS	1	05//75	(13)	14,1409
	2048=WORD 16 BIT STORE	9061	NUCL, ENTERPRISES	2		(10)	14,1410
N	4096 WORD 16 BIT STORE	9061B	NUCL, ENTERPRISES	2	06//75		14,1411
	256 WORDS OF 24 BIT STORE MODULE	CS 0015	NUCL, ENTERPRISES	1	//72	(7)	14,1412
	PROGRAMMABLE READ ONLY MEMORY (32 WORDS, 18 BITS, LOADED BY SOLDER CONNECTIONS)	221	POLON	1	03//75		14,1413
	BUFFER MEMORY (256 16BIT WORDS, USE WITH J CAN 21/C/M)	J MT 20	SCHLUMBERGER	1	//72		14,1414
	CAMAC CORE MEMORY MODULE (2K X 16 BIT)	MM 216C	STND ENGINEERING	3	//74	(12)	14,1415
	(4K X 16 BIT)	MM 416C		3	//74	(12)	
	(8K X 16 BIT)	MM 816C		3	//74	(12)	
	(2K X 24 BIT)	MM 224C		3	//74	(12)	
	(4K X 24 BIT)	MM 424C		3	//74	(12)	
N	SPECTRUM MEMORY	F51=4653/CD	KEMMRMANN	1	//75		14,1416

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF, No.

155 Logic and Arithmetic Processing Modules

	FLOATING POINT ARITHMETIC INTERFACE (FOR USE WITH M 128 HARD, FLOAT, POINT)	C 327	INFORMATEK	1	//3		14,1417
N	MICROPROCESSOR MODULE (FOR FAST ASSY, OF SPECIAL INTERFACES ETC, 8080 BASED)	0326	SENSION	1	//5		14,1418
C	96 CHAN, DRIFT CHAMBER TDC (,5US/1US F,S,, 8 BIT, 40 DEEP BUFFER, DIFF I/P)	2770	LRS=LECROY	2	05/75	(13)	14,1419
	128 CHAN, MWPC ENCODER (RECEIVER, DELAY, LATCH, ENCODER, 80 HIT BUFFER, DIFF I/P)	2720		2	05/75	(13)	

16 Analogue Modules — ADC, DAC, Multiplexers, Amplifiers, Linear Gates, Discriminators etc.

161 Analogue Input Modules (DC and Pulse ADC, TDC)

	32 CHANNEL ANALOG DATA SYSTEM (EXPANDABLE WITH ADDITIONAL MUX MODULES)	5301	BI HA SYSTEMS	2	//4		14,1420
N	A/F CONVERTER	CAM 4,13	METRIMPEX	1	//3		14,1421
	ANALOG INPUT (DUAL SLOPE ADC, +/=16V RANGE,14BITS/16V+SIGN,0,2SEC CONVERSION)	DU 200=1021	DORNIER	1	//2		14,1422
	ANALOGUE TO DIGITAL INTEFACE (WITH PLUG= IN CONVERTER CARDS ADC/8Q, ADC/10Q AND ADC/12Q FOR 8, 10 AND 12 BIT CONVERSION)	ADC 1201	GEC=ELLIOTT	1	//1	(1)	14,1423
	16 CHANNEL, SCANNING A/D CONVERTER	3510	KINETIC SYSTEMS	1	//4		14,1424
N	INTEGRATING A/D CONVERTER (ISOLATED I/P INTEGR TIME 1S/,1S/,02S, RANGE ,03 = 5V)	CAM 4,06=2	METRIMPEX	3	/74		14,1425
	INTEGRATING ADC (12BIT, RANGES 0 TO +5V, 0 TO =5V, 40MSEC CONVERSION TIME)	700	POLON	1	//3		14,1426
	VOLTAGE = FREQUENCY CONVERTER (USED WITH MULTIPLEXERS J MX 10/20)	J CTF 10	SCHLUMBERGER	2	//3		14,1427
	UP=DOWN SCALER/FREQUENCY METER	J EF 10		1	//3		
	DUAL DIGITAL VOLTMETER (+AND= 0,1V, 10 BIT, DIFFERENTIAL INPUT)	2DVM 2013	SEN	1	//1		14,1428
	DIG, VOLTMETER (12BIT + SIGN, POT=FREE RANGES=-AC/DC ,02V = 20V,DC 5=100MA)	C 76451=A13=A1	SIEMENS	2	//3		14,1429
	DIGITAL VOLTMETER (SAME AS TYPE C 76451=A13=A1 WITH DISPLAY)	C 76451=A13=A2	SIEMENS	2	//3		14,1430
	ANALOG INPUTS (MULTIPLEXER=ADC, 8 DIFF I/P,+/=10V RANGE,7BITS/10V+SIGN)	DU 200=1013	DORNIER	2	//2		14,1431
	(SAME FOR +/=5V RANGE, 7BITS/5V+SIGN)	DU 200=1016		2	/72		
	(SAME FOR +10V RANGE, 8BITS/10V)	DU 200=1019		2	/72		
	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				14,1432
	ANALOG INPUT (ADC, +/=10V RANGE, 7BITS/10V+SIGN)	DU 200=1027	DORNIER	2	//2		14,1433
	(SAME FOR +/=5V RANGE, 7BITS/5V +SIGN)	DU 200=1028		2	/72		
	(SAME FOR +10V RANGE, 8BITS/10V)	DU 200=1029		2	/72		
	ANALOGUE TO DIGITAL CONVERTER(8BIT, I/P RANGE 0 TO +5V OR 0 TO =5V,25 USEC CONV)	7028=1	NUCL, ENTERPRISES	1	/70		14,1434
	HIGH SPEED DIGITIZER (6BIT, 100NSEC, RESOLUTION, WITH 256 WORD BUFFER)	SA/D 01	STND ENGINEERING	1	//4	(12)	14,1435
	DUAL 10 BIT ANALOG TO DIGITAL CONVERTER	3515	KINETIC SYSTEMS	1	//3		14,1436
	SINGLE 10BIT ANALOG TO DIGITAL CONVERTER	3515S	KINETIC SYSTEMS	1	//4		14,1437
	DUAL ADC (10BIT, 10USEC CONV TIME)	A/D 210	STND ENGINEERING	2	03/75		14,1438
	DUAL SLOPE ADC (+AND= 0,01/1/10V RANGES, 11BIT RESOLUTION,20MS CONV TIME)	1241	BORER	2	//2	(3)	14,1439
	SUCCESS, APPROX, ADC (WITH S+H, +/=5V OR 0 TO +/=10V, 10=BIT,20/11 USEC ACCESS)	1243/1243A	BORER	2	/72	(9)	14,1440
	SUCCESS, APPROX, ADC (WITH S+H, +/=5V OR 0 TO +/=10V, 12=BIT,23/13 USEC ACCESS)	1244/1244A	BORER	2	//3	(9)	14,1441
	ANALOG INPUTS (MULTIPLEXER=ADC, 8 DIFF I/P,+/=10V RANGE,11BITS/10V+SIGN)	DU 200=1003	DORNIER	2	//2		14,1442
	(SAME FOR +/=5V RANGE, 11BITS/5V+SIGN)	DU 200=1006		2	/72		
	(SAME FOR +10V RANGE, 12BITS/10V)	DU 200=1009		2	/72		
	ANALOG INPUT (ADC, +/=10V RANGE, 11BITS/10V+SIGN)	DU 200=1024	DORNIER	2	//2		14,1443
	(SAME FOR +/=5V RANGE,11BITS/ 5V+SIGN)	DU 200=1025		2	/72		
	(SAME FOR +10V RANGE,12BITS/10V)	DU 200=1026		2	/72		
	OCTAL ADC (8X11BIT + OVF, POS INPUT, 1 MV RESOL, COMMON STROBE, FAST CLEAR)	AD811	EG&G/ORTEC	1	03/75	(13)	14,1444

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	3-DECADE ADC & 16-WAY MUX (PRESET X1-X10 AMPL, 16X24 STORE, 100USEC/CH UPDATE)	500-1	HYTEC	1	/73		14,1445
	(SAME AS 500-1 BUT WITH 8-WAY MUX)	502		1	/74		
	(SAME BUT BINARY ADC)	501		1	/74		
	(SAME AS 501 BUT WITH 8-WAY MUX)	503		1	/74		
	(SAME, BUT AMPL GAIN CAN BE SET AND STORED INDIVIDUALLY/CHANNEL, BCD/BIN)	510		2	/74		
	16-CHANNEL A/D CONVERTER (DIFFERENTIAL INPUTS, 11 BITS + SIGN)	AM-1	JOERGER	2	/74	(11)	14,1446
N	16-CHANNEL A/D CONVERTER (ACCEPTS 4-20MA CURRENT INPUTS, 11 BITS)	AM/I	JOERGER	2	09/75		14,1447
C	A/D CONVERTER (12BIT,MAX 40 USEC CONVERSION, +AND-5V, +AND-10V, +10V RANGES)	30	JORWAY	2	/71	(2)	14,1448
	16 CHANNEL A/D CONVERTER (FET MUX DIFF INPUTS, 12BIT AUTO CYCLING, DUAL SLOPE)	34	JORWAY	2	/74		14,1449
	DUAL 12 BIT ANALOG TO DIGITAL CONVERTER	3520	KINETIC SYSTEMS	1	/73		14,1450
	SINGLE 12BIT ANALOG TO DIGITAL CONVERTER	3520S	KINETIC SYSTEMS	1	/74		14,1451
C	INSULATED ADC (12BITS, 100 USEC, 10MV, FULL SCALE, 300V COMMON MODE)	IADC 2069	SEN	2		(14)	14,1452
	DUAL ADC (12BIT, 25USEC CONV TIME)	A/D 212	STND ENGINEERING	2	03/75		14,1453
C	DIGITAL VOLTMETER (19,999MV TO 1999,9V)	9068	NUCL, ENTERPRISES	2		(13)	14,1454
	DUAL ADC (14BIT, 50USEC CONV TIME)	A/D 114	STND ENGINEERING	1	03/75		14,1455
N	SUCCES, APPROX, 16 BIT ADC (+&-10V, 5MS CONVERSION TIME, INPUT PROTECTION)	0324	SENSIUN	2	/75		14,1456
	OCTAL CHARGE DIGITIZER (8X8BIT CHARGE SENSITIVE ADC, READOUT IN 4X16BIT WORDS)	QD808	EG&G/ORTEC	1		(7)	14,1457
	QUAD FAST GATED INTEGRATOR (CHARGE DIGITIZER, 4X10 BIT)	QD410	EG&G/ORTEC	1	/74	(10)	14,1458
	OCTAL ADC (8 FAST I/P,8BIT/CH, COMMON GATE, NIM LEVELS, BILINEAR MODE)	2248	LRS-LECROY	1	/71		14,1459
	12-CHANNEL ADC (12 FAST I/P, 10BIT/CH, ,25PC SENSITIVITY, FAST CLEAR)	2249A	LRS-LECROY	1	/74	(9)	14,1460
C	12-CHAN, FAST CONV, ADC(4,9US/8,9BIT,32-DEEP BUFFERS, 1/8PS SENSITIVITY,0-256PS)	2250	LRS-LECROY	1	04/75	(13)	14,1461
	12-CHANNEL PEAK ADC (10BIT/CH, -2V FULL SCALE, FAST CLEAR, COMMON GATE)	2259	LRS-LECROY	1	02/75	(13)	14,1462
	OCTAL ADC (MIN 5 NSEC PULSES, POS OR NEG 8BIT/100 PC RESOLUTION, 250 USEC CONV)	9040	NUCL, ENTERPRISES	1	/72	(4)	14,1463
	ANALOGUE TO DIGITAL CONVERTER (80MHZ, 12 BITS)	9060	NUCL, ENTERPRISES	1	/74	(10)	14,1464
	16,000 CHANNEL PULSE ADC (200MHZ CLOCK)	J CAN 21 C/M	SCHLUMBERGER	6	/72	(6)	14,1465
	1024 CHANNEL PULSE ADC (100MHZ CLOCK)	J CAN 40	SCHLUMBERGER	2	/72	(6)	14,1466
	FAST ADC(10 & 12BIT VERSIONS,WITH SAMPLE AND HOLD, CONV TIME 2USEC/4,5USEC)	FADC 2067	SEN	2		(12)	14,1467
	FAST DUAL ADC (DATA AS FOR 2067)	2 FADC 2068		2		(12)	
	EVENT TIMER(4-CHANNEL TIME DIGITIZER, 8B 100MHZ INT, CLOCK, LAM WHEN DONE)	2205	BI RA SYSTEMS	1	/74		14,1468
	QUAD CAMAC SCALER (4X16BIT OR 2X32BIT, 100MHZ)	1004A	BORER	1	01/75		14,1469
	TIME DIGITIZER (4X16BIT,50MHZ CLOCK,WITH CENTRE FINDER, USABLE WITH PRE-AMP 511)	1005	BORER	1	/72		14,1470
	TIME DIGITIZER (4 NIM STOP CHANNELS, COMMON START, 200 PSECS RESOLUTION)	TD104	EG&G/ORTEC	1		(7)	14,1471
	OCTAL TDC (8X15BIT+OVF, COMMON START, 100PSEC RESOLUTION, FAST CLEAR)	TD811	EG&G/ORTEC	1	03/75	(13)	14,1472
	TIME DIGITIZER (6 CHANNELS,16 BITS, 100 MHZ CLOCK RATE)	TD	JOERGER	1	/74	(11)	14,1473
	QUAD TIME-TO-DIGITAL CONVERTER(9BIT/CH, 102/510NSEC RANGES,13USEC CONVERS,NIM)	2226A	LRS-LECROY	1	/70	(2)	14,1474
	OCTAL TIME-TO-DIGITAL CONVERTER(10BIT/CH 102/204/510 NSEC RANGES, FAST CLEAR)	2228	LRS-LECROY	1	/74	(9)	14,1475
C	96 CHAN, DRIFT CHAMBER TDC (,5US/1US F.S., 8 BIT, 40 DEEP BUFFER, DIFF I/P)	2770	LRS-LECROY	2	05/75	(13)	14,1476
	128 CHAN, MWPC ENCODER (RECEIVER, DELAY, LATCH, ENCODER, 80 HIT BUFFER, DIFF I/P)	2720		2	05/75	(13)	
N	A/D CONVERTER (11BIT + SIGN OR 12, CONV TIME 30USEC, RANGE +&-5V, INTERNAL S&H)	CAM 4,05	METRIMPEX	2	/72		14,1477

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	SIXTEEN FOLD TIME-TO-DIGITAL-CONVERTER (100MHZ EXT CLOCK, 4BIT SCALERS USED)	TDC-16	NUCLETRON	1	//4		14,1478
	TIME DIGITIZER(4X16BIT,CLOCK RATE 70/85MHZ, WITH CENTER FINDING LOGIC)	TD 2031	SEN	1	//2		14,1479
	TIME DIGITIZER (4X16BIT,CLOCK RATE 70/85MHZ,NIM LEVELS)	TD 2041	SEN	1	//2	(4)	14,1480
	SERIAL TIME DIGITIZER (8X8BIT 100MHZ, SER + SEQUENT COUNT MODE,SHIFT-REG GATE)	STD 2050	SEN	1	//2		14,1481
	OCTAL TIME TO DIGITAL CONVERTER	TD 008	STND ENGINEERING	1	04//5		14,1482

162 Analogue Output Modules (DAC)

	8 CHANNEL 8 BIT D/A CONVERTER (CURRENT OR VOLTAGE O/P,SLOW ANALOG METER DRIVER)	5405	BI HA SYSTEMS	1	//3		14,1483
	ANALOG OUTPUT (DAC, +10V O/P RANGE, 5MA, 8BIT RESOLUTION, SINGLE O/P)	DO 200-1511	DORNIER	1	//3		14,1484
	(SAME WITH 12BIT RESOLUTION, SINGLE O/P)	DO 200-1521		1	//3		
	(SAME WITH 8BIT RESOLUTION, DUAL O/P)	DO 200-1512		1	//3		
	(SAME WITH 12BIT RESOLUTION, DUAL O/P)	DO 200-1522		1	//3		
	(SAME WITH 8BIT RESOLUTION, QUAD O/P)	DO 200-1517		1	//3		
	(SAME WITH 12BIT RESOLUTION, QUAD O/P)	DO 200-1527		1	//3		
	ANALOG OUTPUT (DAC,+&-10V O/P RANGE,5MA, 8BIT RESOLUTION, SINGLE O/P)	DO 200-1513	DORNIER	1	//3		14,1485
	(SAME WITH 12BIT RESOLUTION, SINGLE O/P)	DO 200-1523		1	//3		
	(SAME WITH 8BIT RESOLUTION, DUAL O/P)	DO 200-1514		1	//3		
	(SAME WITH 12BIT RESOLUTION, DUAL O/P)	DO 200-1524		1	//3		
	(SAME WITH 8BIT RESOLUTION, QUAD O/P)	DO 200-1518		1	//3		
	(SAME WITH 12BIT RESOLUTION, QUAD O/P)	DO 200-1528		1	//3		
	ANALOG OUTPUT (DAC, +&-5V O/P RANGE,5MA, 8BIT RESOLUTION, SINGLE O/P)	DO 200-1515	DORNIER	1	//3		14,1486
	(SAME WITH 12BIT RESOLUTION, SINGLE O/P)	DO 200-1525		1	//3		
	(SAME WITH 8BIT RESOLUTION, DUAL O/P)	DO 200-1516		1	//3		
	(SAME WITH 12BIT RESOLUTION, DUAL O/P)	DO 200-1526		1	//3		
	(SAME WITH 8BIT RESOLUTION, QUAD O/P)	DO 200-1519		1	//3		
	(SAME WITH 12BIT RESOLUTION, QUAD O/P)	DO 200-1529		1	//3		
	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				14,1487
	OCTAL DAC (10BIT,0-5V,500HMS,10USECS)	DAC 1082	GEC-ELLIOTT	1	//3		14,1488
	(SAME BUT WITH 2'S COMPLEMENT 9BIT+SIGN, +AND- 5V, 500HMS)	DAC 1082(B)		1	//3		
	QUAD DAC (4 CHANNEL VERSION OF DAC 1082)	DAC 1042	GEC-ELLIOTT	1	//4		14,1489
	(SAME, 4 CHANNEL VERSION OF DAC 1082(B)	DAC 1042(B)		1	//4		
	DUAL 12 BIT DAC (+/- 10V OR +/- 5V O/P, FOR X-Y DISPLAY DRIVE)	550	HYTEC	1	10//5		14,1490
	DUAL D/A CONVERTER (10 BIT, 10USEC CONV TIME, +10V, +AND-10V, +AND-5V RANGES)	D/A-10	JUERGER	1	//3	(13)	14,1491
	DUAL D/A CONVERTER (12 BIT, 30USEC CONV TIME, +10V, +AND-10V, +AND-5V RANGES)	D/A-12	JUERGER	1	//3	(13)	14,1492
	OCTAL D/A CONVERTER (8BIT RESOLUTION, 0 TO 2MA OR 0 TO +10V OUT)	8 D/A	JUERGER	1	//3	(13)	14,1493
	D/A CONVERTER (12BIT,5 USEC CONVERSION, O/P RANGES +AND-2,5V/5V/10V AND +5V/10V)	31	JORWAY	1	//1	(2)	14,1494
	8 CHANNEL 10 BIT D-A CONVERTER	3110	KINETIC SYSTEMS	1	//2		14,1495
N	DIGITAL TO ANALOG CONVERTER (12BIT, CONV TIME 10USEC, O/P RANGE 0 TO 5V, MAX 5MA)	CAM 4,10	METRIMPEX	1	//2		14,1496
N	DIGITAL TO ANALOG CONVERTER (4X10BIT, TIME 10USEC, O/P RANGE +&-5V, MAX 5MA)	CAM 4,11	METRIMPEX	2	//4		14,1497
	DUAL DIGITAL-TO-ANALOG CONVERTER (10BIT, OUTPUT 0 TO +10V OR -5 TO +5V)	2DAC 2011	SEN	1	//1		14,1498
	DUAL DAC (12BIT, +AND-10V OR +AND-20MA)	C 76451-A15-A4	SIEMENS	1	//3		14,1499
	ISOLATED DUAL DAC (10BIT,30USEC,10V/5MA, OPTOCOUPLER,4 TIMING MODES,RANGE-MODIF)	C-DA-210	WENZEL ELEKTRONIK	1	//4		14,1500
	QUAD DAC (8BIT,10USEC,5V/50MA,4TIMING-M, +,- &RANGE MODIF,OPT,GROUND-REJ&,5USEC)	C-DA-408	WENZEL ELEKTRONIK	1	//4	(11)	14,1501
	QUAD DAC(10BIT,10USEC,5V/50MA,4TIMING-M, +,- &RANGE MODIF,OPT,GROUND-REJ&,5USEC)	C-DA-410	WENZEL ELEKTRONIK	1	//4	(11)	14,1502

164 Analogue Handling and Processing Modules I (MX)

	SEE ALSO DORNIER ADC TYPES		DORNIER				14,1503
N	MULTIPLEXER CONTROL UNIT (UP TO 7 CAM 4,08-21 /R CAM 4,08-22)	CAM 4,08-1	METRIMPEX	1	//4		14,1504
	12 INPUT ANALOGUE MULTIPLEXER (RANDOM OR SCAN ACCESS CONTROLLED BY SKIP REGISTER)	MX 2025	SEN	1	//2	(6)	14,1505

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	12-CHANNEL ANALOGUE MULTIPLEXER (FET, 5 USEC SWITCHING TIME, +/-10V)	MX 2070	SEN	1		(13)	14,1506
	WIDE-BAND ROUTER (12-CHANNEL 50 OHMS ANALOGUE MULTIPLEXER)	WBR 2073	SEN	1		(13)	14,1507
	15 CHANNEL MULTIPLEXER (ANALOGUE SIGNALS ROUTED TO ADC/DVM, DIRECT + SCAN MODES)	1701	BORER	1	//2	(3)	14,1508
	DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				14,1509
	RELAY MULTIPLEXER (16 CHANNELS, MAX 200V/ 500MA OR 10VA, DATAWAY SET+INCR ADDRESS)	DU 200-1036	DORNIER	1	//2		14,1510
	(WITH FRONT PANEL CONNECTOR)	DU 200-1236		1	//2		
	(SAME WITH LOW THERMO VOLTAGE CONTACTS)	DU 200-1035		2	//1		
	(WITH FRONT PANEL CONNECTOR)	DU 200-1235		2	//1		
	ANALOG MULTIPLEXER (15 CHANNELS, REED RELAYS, MAN AND DATAWAY SEL, EXPANDABLE)	AM	JUERGER	2	//2	(6)	14,1511
	16-CHANNEL A/D CONVERTER (DIFFERENTIAL INPUTS, 11 BITS + SIGN)	AM-1	JUERGER	2	//4	(11)	14,1512
N	16-CHANNEL A/D CONVERTER (ACCEPTS 4-20MA CURRENT INPUTS, 11 BITS)	AM/I	JUERGER	2	09/75		14,1513
C	15 CHANNEL RELAY MULTIPLEXER	3530	KINETIC SYSTEMS	1	//3		14,1514
N	15 CHANNEL RELAY MULTIPLEXER	3530L		2	//5		
	MASTER MULTIPLEXER (16 CH, 4 POLE REED)	601	NUCL. ENTERPRISES		//0		14,1515
	SLAVE MULTIPLEXER (16 CH, 4 POLE REED)	600			//0		
	16 CHANNEL RELAY MULTIPLEXER STANDARD LEVEL)	J MX 10	SCHLUMBERGER	1	//3		14,1516
	(SAME FOR LOW LEVEL)	J MX 20		1	//3		
	MULTIPLEXER MANUAL CONTROL	J AX 10		1	//3		
	MULTIPLEXER 16X4 CONTACTS		SIEMENS	1	//4		14,1517
	16-CHANNEL FAST MULTIPLEXER (FET SWITCHES FOR ADC 1243 AND 1244)	1704	BORER	1	//2	(4)	14,1518
	FET MULTIPLEXER (16 CHANNELS, MAX +OR-10V, DATAWAY SET + INCR ADDRESS)	DU 200-1031	DORNIER	1	//2		14,1519
	(SAME WITH FRONT PANEL CONNECTOR)	DU 200-1231		1	//2		
	FET MULTIPLEXER (16 DIFF I/P, MAX +OR-10V, DATAWAY SET+INCR ADDRESS)	DU 200-1034	DORNIER	1	//2		14,1520
	(WITH FRONT PANEL CONNECTOR)	DU 200-1234		1	//2		
	16 CHANNEL A/D CONVERTER (FET MUX DIFF INPUTS, 12BIT AUTO CYCLING, DUAL SLOPE)	34	JORWAY	2	//4		14,1521
N	16 CHANNEL FAST DIGITAL MULTIPLEXER (PULSE WIDTH MIN 7 NSEC)	CAM 6,03	METRIMPEX	2	//4		14,1522
N	16 CHANNEL MULTIPLEXER (SWITCHING OF 3 WIRES, MAX 500HZ, MAX 100V)	CAM 4,08-21	METRIMPEX	2	//4		14,1523
N	16 CHANNEL MULTIPLEXER (SWITCHING OF 4 WIRES, MAX 500HZ, MAX 100V)	CAM 4,08-22	METRIMPEX	2	//4		14,1524
	MULTIPLEXER-SOLID STATE (16 SINGLE-ENDED OR 8 DIFF CHAN, RANDOM OR SEQUENT ACCESS)	9026	NUCL. ENTERPRISES	1	//1		14,1525
	SOLID STATE MULTIPLEXER (16 CH, RANDOM, & SEQUENT ACCESS, MULTI-MUX SCAN MODE)	MX 016	SIND ENGINEERING	1	//4	(12)	14,1526
	32 CHANNEL ANALOG MULTIPLEXER (SERVE AS CHANNEL EXPANDER FOR 5301 DATA SYSTEM)	5101	BI NA SYSTEMS	1	//4		14,1527
N	32 CHANNEL ANALOG MULTIPLEXER (MAX 100KHZ, MAX +&-5V IN)	CAM 4,07	METRIMPEX	1	//3		14,1528
	RELAY MULTIPLEXER (32 CHANNELS)	750	PULON	2	03/75		14,1529
	MULTIPLEXER (32 CHANNEL, 2 CONTACTS)	C 76451-A4-A1	SIEMENS	2	//3		14,1530
	MULTIPLEXER (32 CHANNEL, 4 CONTACTS)	C 76451-A4-A2	SIEMENS	2	//3		14,1531
	MULTIPLEXER 32X2 CONTACTS	C 72468-A0628-A001	SIEMENS	1	//4		14,1532
	FET MULTIPLEXER (32 CHANNELS, MAX +OR-10V, DATAWAY SET+INCR ADDRESS)	DU 200-1032	DORNIER	1	//2		14,1533
	(WITH FRONT PANEL CONNECTOR)	DU 200-1232		1	//2		
	FET MULTIPLEXER (32 DIFF I/P, MAX +OR-10V, DATAWAY SET+INCR ADDRESS)	DU 200-1037	DORNIER	2	//2		14,1534
	(SAME WITH FRONT PANEL CONNECTORS)	DU 200-1237		2	//2		
	FET MULTIPLEXER (64 CHANNELS MAX +OR-10V, DATAWAY SET+INCR ADDRESS)	DU 200-1061	DORNIER	2	//3		14,1535
	(WITH FRONT PANEL CONNECTOR)	DU 200-1261		2	//3		

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	165 Analogue Handling and Processing Modules II (LIN. Gates, Ampl., Discriminators etc.)						
N	PREAMPLIFIER (GAIN RANGES=- X10, X30, X100, X300)	CAM 4,15	METRIMPEX	3	//2		14,1536
N	FILTER AMPLIFIER (GAIN RANGE=- OFF, X1, X10)	CAM 4,16	METRIMPEX	3	//2		14,1537
	ACTIVE FILTER AMPLIFIER(10 = 1000 GAIN, ,25=4USEC GAUSS, PULSE SHAPING,0=10V OUT	1101	POLON	3	//4		14,1538
	BASELINE RESTORER(,1% COUNT RATE STABIL UP TO 50KHZ,0=10 I/O SIGNALS,1V/V GAIN)	1102	POLON	2	//4		14,1539
	DELAY AMPLIFIER(,25 = 4,75USEC DELAY, 0 TO 10V IN/OUT SIGNALS, 1V/V GAIN)	1103	POLON	2	03//5		14,1540
	SUM=INVERT AMPLIFIER(,2% NON=LINEARITY, 1V/V GAIN, 0 TO 10V IN/OUT SIGNALS)	1104	POLON	1	//4		14,1541
	LINEAR GATE (,2% NON=LINEARITY, +/= 1V/V GAIN, 0 TO 10V IN/OUT SIGNALS)	1105	POLON	1	//3		14,1542
	PULSE STRETCHER(,05=,9USEC I/P WIDTH, 1USEC O/P WIDTH OF PULSES, ,9 V/V GAIN)	1106	POLON	1	//4		14,1543
	SINGLE CHANNEL ANALYSER (,2=10V LO/HI LEVEL, ,2=2V WINDOW, ,5=2,5USEC DELAY)	1201	POLON	3	//4		14,1544
	LINEAR RATEMETER (10 TO 100K CPS RANGE, 1S TO 30S TIME CONSTANTS)	1301	POLON	3	//4		14,1545
	LOGIC SHAPER AND DELAY (,2 TO 110USEC DELAY, ,2 TO 11USEC O/P PULSE WIDTH)	1401	POLON	2	//4		14,1546
	UNIVERSAL COINCIDENCE (,1 TO 2USEC RESOLVING TIME)	1402	POLON	2	//4		14,1547
N	FAST AMPLIFIER (200V/V GAIN, 10NS RISE TIME, 200NS TC DIFF, 200NS TC INTEGR)	1501	POLON	3	//5		14,1548
	FAN OUT (1 NIM IN, 2 NIM & 1 COMPL TTL OUT)	1504	POLON	1	//3		14,1549
	CAMAC CONTROLLED PULSE SHAPER (4 PM I/P, 4 NIM I/P & 6 NIM O/P)	CPS 2065	SEN	1		(12)	14,1550
	DUAL PULSE DELAY UNIT	PD 002	STND ENGINEERING	5	//3		14,1551
	SAMPLE=AND=HOLD AMPLIFIER (DUAL DIFF AMPL,+/=10V RANGE,20MA OUT,5USEC SETTL)	DO 200=1040	DORNIER	2	//2		14,1552
	(SINGLE AMPL VERSION, BOTH TYPES HAVE HOLD AND TRACK MODES)	DO 200=1041		2	//2		
	PROGRAMABLE AMPLIFIER/ATTENUATOR (GAIN 0DB TO 60DB IN 10 STEPS, ATTENUATION ,5)	DO 200=1052	DORNIER	2	//3		14,1553
	(SAME BUT DUAL CHANNEL VERSION)	DO 200=1053		1	//3		
	PROGRAMMABLE AMPLIFIER (GAIN 1, 10, 100, 1000)	DO 200=1054	DORNIER	1	05//5		14,1554
	(SAME BUT DUAL CHANNEL VERSION)	DO 200=1055		1	05//5		
	PROGRAMMABLE PRESISION ATTENUATOR (1/1 TO 1/2048, 20V MAX I/P RANGE)	PPA 2071	SEN	1		(13)	14,1555
	DIGITAL WINDOW DISCRIMINATOR (WITH 128X16BIT BUFFER, PARALLEL + SERIAL I/P)	DWD 2046	SEN	1	//2	(8)	14,1556
N	TIME TO PULSE HEIGHT CONVERTER (START= STOP I/P, MAX 256NSEC, RESOL 100PSEC)	CAM 4,17	METRIMPEX	2	//4		14,1557
	17 Other Digital and/or Analogue Modules — Mixed Analogue and Digital, Not Dataway Connected etc.						
N	PROM PROGRAMMER	3090	KINETIC SYSTEMS	2	11//5		14,1558
N	DUAL BRIDGE POWER SUPPLY (FLOATING OUTPUTS EACH MAX 24V/200MA)	CAM 4,08=3	METRIMPEX	2	//4		14,1559
N	OCTAL FLOATING POWERED BRIDGE (PT=THERMO=R APPL, USE WITH CAM 4,08=21)	CAM 4,08=41	METRIMPEX	2	//4		14,1560
N	OCTAL FLOATING POWERED BRIDGE (PT=THERMO=R APPL, USE WITH CAM 4,08=22)	CAM 4,08=42	METRIMPEX	2	//4		14,1561
N	COLD POINT POWER SUPPLY (FOR COLD POINT REFERENCE BRIDGES)	CAM 4,08=5	METRIMPEX	2	//4		14,1562
	DETECTOR BIAS SUPPLY (0 TO +/=2000V, 1MOHM AND 10MOHM OUTPUT RESISTANCE)	1901	POLON	4	//4		14,1563
	NUMERICAL CONTROL SYSTEM, COMPRISING --	C 500	RDT				14,1564
	DATA WRITER AND DISPLAY	C 504		NA			
	SERIAL CONTROLLER	C 502		0			
	DATA RECEIVER FOR MECHANICAL OPERATIONS (5 DECADE DATA,3 DECADE INSTRUCTION REG)	C 501		0		(7)	

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	CAMAC PROM PROGRAMMER		SESSION	2		(13)	14,1565
	CURRENT SOURCE (1MA TO 10MA AND FOR PT 100 ADAPTOR)	C 76451-A5-A1	SIEMENS	2	/73		14,1566

2 SYSTEM CONTROL EQUIPMENT — COMPUTER COUPLERS, CONTROLLERS AND RELATED EQUIPMENT

21 Interfaces/Drivers and Controllers — Parallel Mode for 4600 Branch and Other Multi-Crate Bus, Single-Crate Systems, Autonomous Systems

211 Interfaces/Drivers for Multicrate Systems I (4600 Branch Compatible)

	EXECUTIVE SUITE ASSEMBLY OF MODULAR CONTROLLERS IN CAMAC CRATE, COVERS SYSTEM COMPLEXITY FROM SINGLE SOURCE-SINGLE CRATE TO MULTI SOURCE-MULTI CRATE SYSTEMS,COMPRISING		GEC-ELLIOTT				14,2001
	EXECUTIVE CONTROLLER (TRANSFORMS STANDARD CRATE INTO SYSTEM CRATE)	MX-CTR-2		2	/72		
	BRANCH COUPLER (ONE PER BRANCH, MAX 7)	BR-CPR-2		2	/72		
	AND SYSTEM INTERFACE SOURCE UNITS, ALSO OPTIONALLY AUTONOMOUS CONTROLLER SOURCE UNITS (ALL INSERTED INTO SYSTEM CRATE)		GEC-ELLIOTT				14,2002
	PDP-11 SYSTEM INTERFACE, COMPRISING		GEC-ELLIOTT				14,2003
	PROGRAM TRANSFER INTERFACE	PTI-11 C/D		3	/72		
	UNIBUS TERMINATION UNIT	TRM-11-1		1	/74		
	INTER UNIT BUS (LINKS UNIBUS TO ALL SI SOURCE UNITS FORMING INTERFACE)	IUB-X			/74		
	INTERRUPT VECTOR GENERATOR (ADDS AUTONOMOUS ENTRY OF GL-DERIVED INTERRUPTS)	IVG-11		1	/72		
	AUTONOMOUS MEMORY ACCESS CONTROLLER (2 USEC/WORD TRANSFER TO PDP-11 STORE)	AMC-11		2	08/75		
	NOVA/SUPERNOVA SYSTEM INTERFACE, COMPR		GEC-ELLIOTT				14,2004
	PROGRAM TRANSFER INTERFACE	PTI-N C/D		3	/72		
	I/O BUS TERMINATION UNIT	TRM-N		1	/72		
	INTER UNIT BUS	IUB-X			/74		
	INTERRUPT VECTOR GENERATOR (256 BIT TRAP STORE, BRANCH OR GL PRIORITY MODES)	IVG-2402		1	/74		
	INTERDATA 70-SERIES SYSTEM INTERFACE COMPRISING		GEC-ELLIOTT				14,2005
	PROGRAM TRANSFER INTERFACE	PTI-70 C/D		3	/73		
	I/O BUS TERMINATION UNIT	TRM-70		1			
	INTER UNIT BUS	IUB-X			/74		
	INTERRUPT VECTOR GENERATOR (256 BIT TRAP STORE, BRANCH OR GL PRIORITY MODES)	IVG-2402		1	/74		
	HONEYWELL 316/516 SYSTEM INTERFACE,COMPR		GEC-ELLIOTT				14,2006
	PROGRAM TRANSFER INTERFACE	PTI-H16 C/D		3	/73		
	I/O BUS TERMINATION UNIT	TRM-H16		1			
	SYSTEM INTERFACE BUS	SI-BUS-XH16			/73		
	GEC 4080 SYSTEM INTERFACE, COMPRISING		GEC-ELLIOTT				14,2007
	DIRECT TRANSFERS INTERFACE	PTI-2050 C/D		3	/73		
	INTERRUPT VECTOR GENERATOR	IVG-2402		1	/74		
	BLOCK TRANSFER CHANNEL CONTROLLER	PTI-2050 D		3	/73		
	INTER UNIT BUS	IUB-X			/74		
	AUTONOMOUS MEMORY ACCESS CONTROLLER (2,5 US/WORD TRANSFER TO GEC-4080 STORE)	AMC-4080		2	08/75		
	GEC 2050 SYSTEM INTERFACE (SAME ITEMS AS FOR GEC 4080 INTERFACE)		GEC-ELLIOTT		/74		14,2008
	SYSTEM CRATE TEST UNIT (TWO-COMMAND TEST UNIT FOR CHECKING SYSTEM CRATE SYSTEMS)	SC-TST-1	GEC-ELLIOTT	3	/72		14,2009
	BRANCH HIGHWAY DRIVER	3991	KINETIC SYSTEMS	2	/75		14,2010
	MICROPROGRAMMED BRANCH DRIVER FOR PDP-11 (FROM 256 UP TO 4K WORDS MEMORY)	1201	BI NA SYSTEMS	NA	/72	(5)	14,2011
	UNIBUS CABLE ASSEMBLY	8101			/72		
	PDP-11 CAMAC CONTROLLER(SEQUENTIAL READ/WRITE,24 GRADED-L INTERRUPT DIRECTLY)	CA 11-A	D E C	NA	/71	(2)	14,2012
	PDP-15 CAMAC INTERFACE(18/24BIT,PROGR, SEQUENT ADDR AND BLOCK TRANSFER MODES)	CA 15 A	D E C	NA	/71	(1)	14,2013
	PDP-11 INTERFACE/BRANCH DRIVER (24 VECTOR ADDRESSES, PROGRAMMED AND MULTIPLE DMA-TRANSFER, ADDRESS SCAN AND -LIST MODE, REPEAT-, LAM- AND STUP MODE)	CA 11-C	D E C	NA	/72	(4)	14,2014
	PDP-11 BRANCH DRIVER (FOR 4600 COMPATIBLE,PROGRAMMED AND SEQUENT ADDR MODES)	BD-011	EG&G/ORTEC	NA	/71		14,2015
N	PDP-11 INTERFACE (BRANCH AND/OR SERIAL HIGHWAY, DMA, BD011 REG, ASSIGNMENTS)	211	JORWAY	NA	12/75		14,2016
	PDP-11 BRANCH DRIVER	KS 0011	KINETIC SYSTEMS	NA	/71	(4)	14,2017

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	INTERFACE AND DRIVER FOR PDP 11 OR PDP 8 MULTI-CRATE SYSTEM, COMPRISING		NUCL, ENTERPRISES				14,2018
	BRANCH INTERFACE	9031		2	//2	(7)	
	16-BIT CONTROLLER (WITH EITHER OF THE FOLLOWING INTERFACE CARDS)	9030		3	//2	(7)	
	PDP 11 INTERFACE CARD	9032			//2		
	INTERFACE CARD FOR DEC PDP 8 SERIES	9034			//3	(7)	
	INTERFACE CAMAC-PDP 11 (PROGRAMMED,BLOCK TRANSFER AND SEQUENTIAL ADDR MODES)	ICP 11/ICP 11 A	SCHLUMBERGER	NA	//1	(4)	14,2019
	NOVA BRANCH DRIVER	1251-1	BI RA SYSTEMS	NA	//3	(5)	14,2020
	NOVA BRANCH DRIVER WITH DATA CHANNEL	1251-2	BI RA SYSTEMS	NA	//4	(5)	14,2021
	NOVA BRANCH DRIVER	NBD 100	SIND ENGINEERING	2	//4		14,2022
	INTERFACE/SYSTEM CONTROLLER TO HP2100, 2114, 2115, 2116	2201	BURER	NA	//1	(4)	14,2023
	PRIME COMPUTER BRANCH DRIVER (WITH DTM, PRIME COMPUTER BRANCH CABLE TYPE 8103)	1260	BI RA SYSTEMS	NA	//4		14,2024
	INTERFACE FOR VARIAN 620I/L/F COMPUTER (PROGR,SEQUENT AND BLOCK TRANSFERS)	2204	BURER	NA	//2		14,2025
N	CTL MODULAR ONE AUTONOMOUS BRANCH HIGHWAY CONTROLLER	20368	C T L	NA	//5	(14)	14,2026
	SYSTEM CONTROLLER FOR SIEMENS 404/3 (TRANSFER OF 16 OR 24 BIT DATAWORDS PARALLEL BRANCH COMMAND CHAINING)	DU 200-2921	DURNIER	6	//3		14,2027
	(SAME BUT WITHOUT COMMAND CHAINING)	DU 200-2922		6	//3		
	SYSTEM CONTROLLER FOR SIEMENS 404/3 (TRANSFER OF 16 OR 24 BIT DATAWORDS PARALLEL BRANCH BUT NO COMMAND CHAINING)	DU 200-2923	DURNIER	6	//3		14,2028
	MICRODATA 800/CIP 2000 BRANCH DRIVER	91	JORWAY	NA	//3	(7)	14,2029
	BRANCH DRIVER (24BIT, PROGR, SEQUENT AND BLOCK TRANSFER MODES, MAX 7 CRATES)	5400	LABEN	4		(8)	14,2030
N	BRANCH DRIVER - INTERFACE FOR 1001 TPA-1	CAM 1,04	METRIMPEX	NA	//3		14,2031
N	AUTONOM ADAPTER (INTERFACES CAMAC TO AUTONOMOUS CHANNEL)	CAM 1,18		1	//4		
	INTERFACE-DRIVER FOR VARIAN 73/620I/620L MULTI-CRATE SYSTEM, COMPRISING		NUCL, ENTERPRISES			(8)	14,2032
	BRANCH INTERFACE	9031		2	//2	(7)	
	16-BIT CONTROLLER	9030		3	//2	(7)	
	AND						
	INTERFACE CARD FOR VARIAN 73/620I/620L SERIES COMPUTERS	CS 0044				(8)	
	SYSTEM CONTROLLER FOR SIEMENS 320/330 (AUTO-GL, 24 VECTOR ADDR, PROGRAMMED & DMA TRANSF, ADDR-SCAN,INCREM,RANDOM LIST REPEAT,LAM & STOP MODES)	C 72451 A1602	SIEMENS	8	//4		14,2033

212 Interfaces/Drivers for Multicrate Systems II (for other Parallel Mode Control/Data Highway)

	DEDICATED CRATE CONTROLLER FOR NOVA	NC023	EG&G/ORTEC	2	//3		14,2034
	TERMINATOR FOR NOVA I/O BUS	NT022		1	//3		
	BIDIRECTIONAL DATA BREAK MODULE FOR PDP8 COMPUTERS (FOR USE WITH 7048-2)	1000	HYTEC	2	//4		14,2035
	PROGRAMMED DATAWAY CONTROLLER (PART OF 7000-SER SYSTEM WITH EXT CONTR HIGHWAY)	7025-2	NUCL, ENTERPRISES	2	//0		14,2036
	COMMAND GENERATOR	7062-1		2	//1		
	TRANSFER REGISTER	7063-1		1	//0		
	PROGRAM CONTROL UNIT	0362-2		NA	//0		
	WIRED STORE	7044-1		1	//0		
	CONTROLLER/INTERFACE FOR T1600 COMPUTER (MAX 8 CRATES, PROG/ADDR,SCAN/STOP MODE)	JCT 16-10		2			
	DMA MODULE	JDM 16,10		2			
	CRATE CONTROLLER FOR NOVA COMPUTER	CC 2023A/B	SEN	2	//0		14,2037
	CRATE CONTROLLER BUS TERMINATOR FOR CC 2023A/B (ONE PER SYSTEM)	BT 2022		1	//1		

213 Interfaces/Drivers for Single-Crate Systems (4100 Dataway Compatible)

	SINGLE CRATE SYSTEM CONTROLLERS(SEE EXECUTIVE SUITE, CLASS ,211)		GEC-ELLIOTT				14,2038
	PDP-11-SERIES CRATE CONTROLLER	1304	BI RA SYSTEMS	2	//3		14,2039
	CRATE CONTROLLER/PDP11 UNIBUS INTERFACE	1533A	BURER	2	//2	(4)	14,2040
	NPR CONTROLLER FOR DMA TO PDP11 E,G, VIA 1533A CRATE CONTROLLER/INTERFACE	1542	BURER	NA	//3	(8)	14,2041
	SINGLE CRATE CONTROLLER/PDP-11 INTERFACE (MULTIPLE BUS ADDRESS VERSION)	CA-11-E	D E C	2	//4	(9)	14,2042

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
C	SINGLE CRATE CONTROLLER/PDP-11 INTERFACE (PROGRAMMED TRANSFERS, WITH NAF REG & CONNECTOR TO DMA OPTION CA-11-FN)	CA-11-FP	D E C	2	06/75	(14)	14,2043
C	PDP-11 DMA INTERFACE FOR CA-11-FP (8 DMA CHANNELS, MI OR LIST MODE, 16BIT WC, CA, OFFSET FOR EACH CHANNEL, LIMIT REGISTER)	CA-11-FN		2	06/75 06/75	(14)	
N	POWER SUPPLY FOR CA-11-F CONTROLLER (GENERATES AC LO & DC LO)	CA-11-PS		NA	06/75	(14)	
	DEDICATED CRATE CONTROLLER FOR PDP-11 (MULTIPLE TRANSFER OR AUTO ADDRESS SCAN)	DC011	EG&G/ORTEC	2		(7)	14,2044
	SINGLE CRATE CONTROLLER FOR PDP-8/E ADDR.-SCAN MODE, DMA I/O, MAX 22 LAMS)	LEM-52/32,1	EISENMANN	3		(13)	14,2045
C	UNIBUS CRATE CONTROLLER PDP-11	3911A	KINETIC SYSTEMS	2	/72		14,2046
	INTERFACE AND DRIVER FOR PDP 11 OR PDP 8 SINGLE CRATE SYSTEM, COMPRISING		NUCL. ENTERPRISES				14,2047
	16-BIT CONTROLLER (WITH EITHER OF THE FOLLOWING INTERFACE CARDS)	9030		3	/72	(7)	
	PDP 11 INTERFACE CARD	9032			/72		
	INTERFACE CARD FOR DEC PDP 8 SERIES	9034			/73	(7)	
	AUTONOMOUS CONTROLLER FOR PDP 11	9033	NUCL. ENTERPRISES	2	/73	(8)	14,2048
	CAMAC CRATE-PDP 11 INTERFACE	J CC 11	SCHLUMBERGER	2		(7)	14,2049
	UNIBUS TERMINATOR	J UT 11		1	/74		
	UNIBUS EXTENDER	C BEX 11			/74		
	CRATE-SYSTEM CONTROLLER FOR PDP-11 (24 BIT READ & WRITE CAPABILITIES)	C-CSC-11	WENZEL ELEKTRONIK	2	/72		14,2050
	NOVA-SERIES CRATE CONTROLLER	1303	BI RA SYSTEMS	2	/73		14,2051
	SINGLE CRATE CONTROLLER TO HP COMPUTERS WITH EXT SYNCHRONISATION FACILITIES	1531A	BORER	2	02/75		14,2052
	INTERFACE FOR HP 2114-2115 COMPUTERS, COMPRISING--		NUCL. ENTERPRISES				14,2053
	16-BIT CONTROLLER	9030		3	/72	(7)	
	AND						
	INTERFACE CARD FOR HP 2114-2115	CS 0058			/74		
N	CTL MODULAR ONE PROGRAMMED DATAWAY CONTROLLER	1,75	C T L	3	/75	(14)	14,2054
	VARIAN-CAMAC INTERFACE CRATE CONTROLLER (16BIT SEQUENT-BLOCK TRANSF, 1 CC/CRATE)	C 300	INFORMATEK	2	/72		14,2055
N	CRATE CONTROLLER-INTERFACE FOR 1001TPA-1	CAM 1,02	METHIMPEX	3	/73		14,2056
	INTERFACE-DRIVER FOR VARIAN 73/620I/620L SINGLE CRATE SYSTEM,COMPRISING		NUCL. ENTERPRISES			(8)	14,2057
	16-BIT CONTROLLER	9030		3	/72	(7)	
	AND						
	INTERFACE CARD FOR VARIAN 73/620I/620L SERIES COMPUTERS	CS 0044				(8)	
	INTERFACE FOR HONEYWELL 316-516 COMPUTERS, COMPRISING--		NUCL. ENTERPRISES				14,2058
	16-BIT CONTROLLER	9030		3	/72	(7)	
	AND						
C	INTERFACE CARD FOR HONEYWELL 316-516	9038			/74		
	INTERFACE FOR K202 COMPUTER (24BIT,AUTO-NOMOUS BLOCK TRANSFERS TO/FROM MEMORY, L-NUMBER INTERRUPT ENCODER)	100	POLON	3	/73		14,2059
	SINGLE CRATE CONTROLLER FOR MICRAL N/G/S	JC MIC 10	R 2 E	2	02/75	(13)	14,2060
	CRATE INTERFACE FOR MULTI 20 OR MULTI 8	J CM 8/20	SCHLUMBERGER	3	/74		14,2061
	CRATE CONTROLLER 320	C 72451-A1446-A6	SIEMENS	3	/72		14,2062
	CRATE CONTROLLER 404	C 76451-A1446-A7	SIEMENS	2	/73		14,2063

	DATA PROCESSOR (AUTONOMOUS PROGRAMABLE SINGLE DATAWAY CONTROLLER 16 REGISTERS	DU 200-2951	DORNIER	3	/73		14,2064
	DATA PROCESSOR (AUTONOMOUS PROGRAMABLE SINGLE DATAWAY CONTROLLER 16 REGISTERS, REGISTERS AND MEMORY EXPANDABLE)	DU 200-2951		3	/73		
N	MICROCOMPUTER	3880	KINETIC SYSTEMS	2	11/75		14,2065
N	CRATE CONTROLLER FOR 3880	3908		2	11/75		
	CADET (SINGEL-CRATE CONTROLLER FOR READ-ONLY SYSTEM, INCL MODULE TEST & DISPLAY)	CT 2058	SEN	4		(12)	14,2066
	PRINT BUFFER (ALLOWS A PARALLEL PRINTER TO BE USED WITH THE CT 2058)	PR 2059		0		(12)	
	PROGRAMMABLE CRATE CONTROLLER	S 800	SENSION	22		(13)	14,2067
	PROGRAMMABLE CRATE CONTROLLER	S 804	SENSION	22		(13)	14,2068

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	CAMAC MICROPROCESSOR CRATE CONTROLLER	MIK XA	STND ENGINEERING	0	/74		14,2069
	217 Other Parallel Mode Interfaces/Drivers/Controllers						
	SYSTEM CRATE CONTROLLER	3960	KINETIC SYSTEMS	2	/73		14,2070
	MODCOMP I,MODCOMP II & MODCOMP III SYSTEM DRIVER(USE WITH 3960)	3970		2	/73		
	CONTROL DATA 6000 SERIES SYSTEM DRIVER (USE WITH 3960)	3973		3	/75		
	MANUAL SYSTEM DRIVER(USE WITH 3960)	3980	KINETIC SYSTEMS	2	/73		14,2071
	22 Interfaces/Controllers/Drivers for Serial Highway						
	SERIAL CRATE CONTROLLER TYPE L=1 (CONFORMING TO ESONE/SH/01 AND ERRATA)	SCC 2401	GEC-ELLIOTT	2	06/75		14,2072
	SERIAL EXTENSION UNIT, 8 BIT BYTE SERIAL LINK, BRANCH COMPATIBLE, CONSISTING OF SERIAL CRATE CONTROLLER *L=1* (CONFORMS TO ESONE/SH/01 & TID=26488 + ERRATA)	74	JUERGER	2	/73 /74	(8) (11)	14,2073
	MANUAL SERIAL DRIVER (BIT/BYTE MODE, MULTIPLE MESSAGES, ERROR GENERATION)	78	JORWAY	4	/74		14,2074
N	PDP=11 INTERFACE (BRANCH AND/OR SERIAL HIGHWAY, DMA, BD011 REG, ASSIGNMENTS)	211	JORWAY	NA	12/75		14,2075
N	MASTER LOOP CONTROL UNIT	3930	KINETIC SYSTEMS	2	/75		14,2076
C	SERIAL HIGHWAY LOOP CONTROL UNIT	3931	KINETIC SYSTEMS	2	/75	(13)	14,2077
	TRANSF, ISOLATED SERIAL D=PORT ADAPTER	3932	KINETIC SYSTEMS	1	/75	(13)	14,2078
N	CRATE CONTROLLER EXPANDER	3940	KINETIC SYSTEMS	1	/75		14,2079
N	SERIAL CRATE CONTROLLER TYPE L=1	3950	KINETIC SYSTEMS	3	/75		14,2080
	TYPE L=1 CRATE CONTROLLER FOR THE "STANDARD" SERIAL HIGHWAY	3952	KINETIC SYSTEMS	2	/75	(13)	14,2081
	DRIVER FOR SERIAL HIGHWAY	3992	KINETIC SYSTEMS	3	/74	(11)	14,2082
	DRIVER FOR SERIAL HIGHWAY (WITH 256 WORD FIFO BUFFER)	3994	KINETIC SYSTEMS	4	/75	(13)	14,2083
N	SERIAL HIGHWAY CONTROLLER	9080	NUCL, ENTERPRISES		09/75		14,2084
	SERIAL CRATE CONTROLLER SPECIFICATION L1	CH 6001	HOVSING	2	11/75	(13)	14,2085
	23 Units Related to 4600 Branch or Other Parallel Mode Control/Data Highway — Crate Controllers, Terminations, Lam Graders, Branch/Bus Extenders						
	DISPLAY DRIVER(CONTROLS 72A DISPLAY, ALSO CRATE CTR AND BRANCH DRIVER)	72A	JORWAY	5	/71		14,2086
	231 Crate Controllers (Type A-1, Other CC Types)						
	TYPE A=1 CRATE CONTROLLER	1301	BI RA SYSTEMS	2	/73		14,2087
	CRATE CONTROLLER /ESONE TYPE A1/ (CONFORMS TO EUR4600 SPECS)	1502	BORER	2	/72		14,2088
	CRATE CONTROLLER TYPE CCA=1 ACCORDING TO EUR4600 SPECS WITH CERN OPTIONS	DU 200=2905	DORNIER	2	/74		14,2089
	CAMAC CRATE CONTROLLER TYPE A=1 (CONFORMS TO EUR4600 SPECIFICATIONS)	CC101	EG&G/ORTEC	2	/72		14,2090
	ESONE TYPE $A_{,}1$ CRATE CONTROLLER(CONFORMS TO EUR4600 SPECS, INCL CERN HOLD OPTION)	CC 2405	GEC-ELLIOTT	2	/73		14,2091
	CRATE CONTROLLER TYPE A=1 (CONFORMS TO EUR4600 SPECS)	CCA=1	JUERGER	2	/72	(5)	14,2092
	BRANCH CRATE CONTROLLER/TYPE A=1 (CONFORMS TO EUR 4600 SPECS, 1972)	70A	JORWAY	2	/73	(7)	14,2093
	TYPE A=1 CRATE CONTROLLER	3900	KINETIC SYSTEMS	2	/73		14,2094
N	TYPE A=1 CRATE CONTROLLER (CONFORMS TO EUR4600 SPECS)	CAM 1,01	METRIMPEX	2	/73		14,2095
	CRATE A=1 CONTROLLER (CONFORMS TO EUR 4600 SPECS)	9016	NUCL, ENTERPRISES	2		(4)	14,2096
	CRATE CONTROLLER TYPE A (CONFORMS TO EUR4600 SPECS)	C 106	RDT	2	/71		14,2097
	CRATE CONTROLLER TYPE A=1 (CONFORMS TO EUR4600 SPECS)	J CRC 51	SCHLUMBERGER	2	/72	(1)	14,2098
	A=1 CRATE CONTROLLER (CONFORMS TO EUR4600 SPECS, INCL CERN SPEC HOLD LINE)	ACC 2034	SEN	2	/72		14,2099

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	CRATE CONTROLLER A1 (EUR 4600 SPECS AND CERN NOTE 38-00)	C 72451-A1446-A2	SIEMENS	2	//0	(1)	14,2100
	TYPE A-1 (ESONE) CRATE CONTROLLER	CC-A1	STND ENGINEERING	2	//2	(6)	14,2101
	TYPE A1 CONTROLLER WITH TERMINATOR (MEETS 4600 SPECS OF JAN 1972)	CCT-A1	STND ENGINEERING	2	//3		14,2102

232 Lam Graders

	LAM GRADER (24 BIT MASK REGISTER, PLUG-IN PATCH BOARD, CERN 064)	LG 2401	GEC-ELLIOTT	1	//2		14,2103
	LAM GRADER (INTERNALLY PATCHABLE, SWITCH SELECTABLE MULTI-CRATE BG-RESPONSE)	LG	JOERGER	1	//3	(8)	14,2104
C	LAM GRADER-SORTER	75	JORWAY	1	//3	(7)	14,2105
N	LAM GRADER (24 BIT)	CAM 1,10	METRIMPEX	1	//4		14,2106
	LAM GRADER (DESIGNED TO EUR 4600 SPECS)	064	NUCL. ENTERPRISES	1	//2	(4)	14,2107
	PRIORITY GRADER	9037	NUCL. ENTERPRISES	1		(10)	14,2108
	LAM GRADER (CERN SPECS 064)	C 107	RUT	1	//1		14,2109
	LAM GRADER (CERN SPECS 064)	LG 2001	SEN	1	//2	(6)	14,2110
	LAM GRADER (24BIT MASK REG, WITH CABLE, PATCHABLE C-ADDR-REG FOR MULTI-CRATE BG)	C 76451-A18-A1	SIEMENS	0	//4		14,2111
N	LAM GRADER(24I/P-&24MASKED-&SUM-LAM-LEDS 24G,X24M,LAM-SUM-TOG,LAM1-7-PATCHPANEL)	C-LG-24	WENZEL ELEKTRONIK	1	08//5	(14)	14,2112

233 Terminations (Simple, with Indicators)

	BRANCH HIGHWAY TERMINATOR	6601	BI HA SYSTEMS	1	//3		14,2113
	BRANCH TERMINATION UNIT (WITH BUILT-IN CABLE)	1592	BORER	1	//3		14,2114
	BRANCH TERMINATION UNIT (NON INDICATING)	BT 6503	GEC-ELLIOTT	2	//2		14,2115
	BRANCH TERMINATION UNIT	BT 6601	GEC-ELLIOTT	2	//1		14,2116
	BRANCH TERMINATOR	BT	JOERGER	2	//2		14,2117
	BRANCH TERMINATION WITH INTEGRAL CABLE	50C	JORWAY	2	//2		14,2118
	BRANCH TERMINATOR IN A CONNECTOR	BT-01	KINETIC SYSTEMS	NA	//3		14,2119
N	BRANCH TERMINATOR	CAM 1,11-1	METRIMPEX	2	//2		14,2120
	BRANCH TERMINATOR	J BT 20	SCHLUMBERGER	2	//1		14,2121
	BRANCH TERMINATOR (NON-INDICATING, 40 CM FLYING CABLE WITH BRANCH CONNECTOR) (DITTO, XXX= CABLE LENGTH IN CM)	BT 231 BT 231XXX	SEMRA-BENNEY	1 1	//4 //4		14,2122
	CRATE CONTROLLER BUS TERMINATOR FOR A-1 CRATE CONTROLLER	BT 2042	SEN	1	//2		14,2123
	BRANCH HIGHWAY TERMINATOR	BHT 2055	SEN	1	//4	(11)	14,2124
	BRANCH HIGHWAY TERMINATOR	BHT-001	STND ENGINEERING	1	//3		14,2125
	BRANCH HIGHWAY TERMINATOR, WITH DISPLAY	BHT-002/D	STND ENGINEERING	2	//3		14,2126
	BRANCH TERMINATOR (FULL BRANCH MONITOR WITH INTERNAL STORAGE AND LED DISPLAY)	BT 6502	GEC-ELLIOTT	2	//2		14,2127
	VISUAL BRANCH TERMINATOR (STORES AND DISPLAYS ON LEDS BRANCH SIGNALS)	VBT	JOERGER	2	//2	(6)	14,2128
	BRANCH TERMINATION WITH BRANCH DISPLAY	51	JORWAY	2	//2		14,2129
N	BRANCH TERMINATOR (WITH INDICATORS)	CAM 1,11-2	METRIMPEX	2	//2		14,2130
	BRANCH TERMINATION UNIT (WITH INDICATOR AND POWER SUPPLY)	C 72451-A10-A1	SIEMENS	NA	//3	(3)	14,2131

234 Branch Extenders, Bus Extenders

	DIFFERENTIAL BRANCH EXTENDER (FOR EXTENDING BRANCHES UP TO 3 KM)	DBE 6501	GEC-ELLIOTT	2	//1		14,2132
	BRANCH HIGHWAY TRANSCEIVER FOR LONG DISTANCE TRANSMISSION	J BHT 10	SCHLUMBERGER	2		(4)	14,2133
	SERIAL DRIVER (TERMINATES BRANCH HIGHWAY AND RETRANSMITS COMMAND SERIALLY) SERIAL RECEIVER (RECEIVES SERIAL DATA, DRIVES TYPE A-1 SYSTEM, OPTICAL ISOL)	SD SR	JOERGER	2 2			14,2134

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	UNIBUS EXTENDER, TRANSMITTER RECEIVER (FOR DISTANCES UP TO 200 METRE OR MORE)	1594 1595	BURER	2 2	//2 //2		14,2135

3 TEST EQUIPMENT

31 System Related test Gear

SYSTEM CHECK OUT UNIT, STORES DATA & COMMAND IN READABLE MEGS, PROGRAMMABLE L	DTM 4	GEC-ELLIOTT	1	//4		14,3001
SYSTEM TEST UNIT (FOR EXECUTIVE SUIT SYSTEM CONFIGURATION, SEE MX-CTR-2)	SC-TST-1	GEC-ELLIOTT	3	//2		14,3002

311 Computer Simulators

PDP-11 SIMULATOR	6101	BI HA SYSTEMS	NA	//2	(5)	14,3003
TEST MODULE (USED IN SYSTEM TEST OF READ/WRITE CAPABILITY)	TM024	EG&G/ORTEC	2	//1		14,3004
TEST CONTROLLER WITH PROGRAM PLUGBOARD	SPS 2048	NUCL, ENTERPRISES	2	01//5	(12)	14,3005
CAMAC SYSTEM SIMULATOR/TESTER	CSS/T	STND ENGINEERING	6	//3		14,3006

32 Branch Related Testers/Controllers and Displays

321 Branch Testers/Controllers (Manual, Programmed)

MANUAL BRANCH TESTER (TYPE A SYSTEM TEST SET WITH MX-CTR-2 & BR-CPR-2)	SC-TST-1	GEC-ELLIOTT	7			14,3007
N MANUAL CONTROLLER (SWITCHES FOR N,A,F,C, I,Z, OP-MODES- REPEAT,SINGLE & STEPPING)	110	POLON	4	//5		14,3008
BRANCH HIGHWAY TEST POINT MODULE(24 DIRECT,22 INDIRECT ACCESS POINTS FOR TEST)	CD 18104	HUGHES	NA	//1	(3)	14,3009
BRANCH HIGHWAY REMOVE INHIBIT MODULE (REMOVES INHIBIT FROM BCR/BA/BF/BN/BTA)	CD 18105	HUGHES	NA	//1	(3)	14,3010
MANUAL BRANCH DRIVER (FOR TESTING TYPE A SYSTEMS)	MBD	JUERGEN	5	//2	(6)	14,3011
MANUAL BRANCH CONTROL SET (COMPRISING TYPES C COB 10 AND T CMB 10)	C CMB 10	SCHLUMBERGER	NA	//1	(1)	14,3012

33 Dataway Related Testers and Displays

331 Dataway Controllers/Testers Manual, Programmed)

N MC WORD GENERATOR FOR USE WITH TYPE 110 (25 BITS WORD TO W BUS LINES)	232	POLON	1	//5		14,3013
N WORD DISPLAY FOR USE WITH TYPE 110	260		1	//5		
N TEST CONTROLLER24	744006/D	WEHRMANN	1	//5		14,3014
N TEST CONTROLLER25	744006/E	WEHRMANN	1	//5		14,3015
MANUAL CRATE CONTROLLER	GFK-LEM	EISENMANN	8	//1		14,3016
MANUAL CRATE CONTROLLER	MCC	JUERGER	5	//2		14,3017
N MANUAL DATAWAY TEST CONTROLLER	CAM 7,01	METHIMPEX	3	//3		14,3018
MANUAL DATAWAY CONTROLLER/DISPLAY SYSTEM INTERFACE TO DATAWAY CONTROL AND DISPLAY CRATE	D AI 10 J DA 10 C AI 10	SCHLUMBERGER	 1 NA	//1		14,3019
MANUAL CRATE CONTROLLER	J CMC 10	SCHLUMBERGER	8	//1	(1)	14,3020
TEST MODULE FOR CRATE CONTROLLER AND DATAWAY	DTM 2040	SEN	1	//2		14,3021
MANUAL 24 BIT CRATE CONTROLLER	MCC-240	STND ENGINEERING	2	//2	(5)	14,3022
DYNAMIC TEST CONTROLLER (GENERATES ALL POSSIBLE CAMAC COMMANDS IN SINGLE CRATE)	TC 2403	GEC-ELLIOTT	3	//1		14,3023
DYNAMIC TEST CONTROLLER (2 SIMULT TRANSF SINGLE,STEP-BY-STEP AND CONTINUOUS MODE)	C 108	KDT	8	//1	(4)	14,3024
DATAWAY SERVICE MODULE	J DS 10	SCHLUMBERGER	1	//4	(12)	14,3025
N MANUAL INPUT/OUTPUT (TEST UNIT PROVIDES MANUAL DATA INPUT & VISUAL DATA OUTPUT)	MI/O	JUERGER	1	08//5		14,3026
CONTROLEUR SURTIE DATAWAY (DATAWAY TEST MODULE)	41403	TRANSHACK	1	//0		14,3027

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	332 Dataway Displays						
N	DATAWAY DISPLAY	734653/A	WEHRMANN	2	//5		14,3028
	CAMAC TEST MODULE/DATAWAY DISPLAY	6102	BI RA SYSTEMS	2	//3		14,3029
	CAMAC DATAWAY DISPLAY (DATAWAY SIGNAL PATTERN STORED/DISPLAYED,2 TEST MODES)	1801	BURER	1	//1	(1)	14,3030
	CAMAC DATAWAY TEST AND DISPLAY MODULE	LEM-52/16,2	EISENMANN	1			14,3031
	DATAWAY MEMORY (DISPLAY + READABLE REGISTER)	C 340	INFORMATEK	1	//2		14,3032
	DATAWAY DISPLAY (STORES AND DISPLAYS DATAWAY SIGNALS, FARBQXCIZS1S2BP1P2)	DD	JUERGER	1	//2	(6)	14,3033
	DATAWAY DISPLAY (SEPARATE R & W DISPLAY, TRACKS OR STORES, MANUAL CLEAR)	202	JORWAY	1	//4	(11)	14,3034
	DATAWAY DISPLAY	3290	KINETIC SYSTEMS	1	//2		14,3035
	DATAWAY DISPLAY (WITH MEMORY, FOLLOW, ON-LINE & TRIGGER MODES)	9554	NUCL. ENTERPRISES	1		(13)	14,3036
	DATAWAY DISPLAY	C 76451-A16-A1	SIEMENS	1	//3	(6)	14,3037
	DATAWAY DISPLAY MODULE	DD-002	STND ENGINEERING	1	//2	(5)	14,3038
	DATAWAY DISPLAY (DISPLAYS AND STORES DATAWAY SIGNAL PATTERN)	C-D1-24	WENZEL ELEKTRONIK	1	//2		14,3039
	34 Module Related Test Gear (Module Extenders)						
	CAMAC MANUAL MODULE TESTER	6103	BI RA SYSTEMS	NA	//4		14,3040
	341 Module Extenders						
	CAMAC EXTENDER MODULE	8201	BI RA SYSTEMS	1	//3		14,3041
	EXTENSION FRAME (MODULE EXTENDER)	EF 1-1	GEC-ELLIOTT	1	//1		14,3042
	MODULE EXTENDER (+AND-6V,+AND-24V FUSED, RETRACTABLE LOCKING DEVICE)	ME	JUERGER	1	//2		14,3043
	EXTENDER MODULE (FUSED +&-6V AND +&-24V, SUPPORT ARM)	11A	JORWAY	1	//4		14,3044
C	EXTENDER MODULE (W/36 POS PC EDGE CONN)	1100	KINETIC SYSTEMS	1	//1	(4)	14,3045
N	EXTENDER CARD	1150F	KINETIC SYSTEMS	1			14,3046
N	DATAWAY EXTENDER MODULE	9073	NUCL. ENTERPRISES	1	01//5		14,3047
	BUFFERED EXTENDER (25NSEC PROPAGATION DELAY, 60 CM FLEXIBLE CABLE)	060	PULON	1	03//5		14,3048
	EXTENDER MODULE	061	PULON	1	//3		14,3049
	EXTENDER	CEX	RDT	1	//2		14,3050
	MODULE EXTENDER	ME 2030	SEN	1	//0		14,3051
	DATAWAY EXTENDER MODULE	EB 01	STND ENGINEERING	1	//2		14,3052
	EXTENDER (XXX=LENGTH OF CABLE IN MM BEYOND RACK, SINGLE WIDTH)	577/XXX	TEKDATA	1	//2	(5)	14,3053
	(DITO, DOUBLE WIDTH, FIXED SIDES)	5813/XXX		2	//3		
	(DITO, DOUBLE WIDTH, HINGED SIDES)	5824/XXX		2	//5		
	PROLUNGATEUR POUR TIROIRS CAMAC CABLE (WIRED EXTENDER)	41401	TRANSRACK	1	//0		14,3054
	PROLUNGATEUR POUR TIROIRS CAMAC NON CABLE (UNWIRED EXTENDER)	41402	TRANSRACK	1	//0		14,3055
	37 Other Test Gear for CAMAC Equipment						
	TRANSIENT GENERATOR(MODULE NOISE SUSCEPTIBILITY TESTED BY TRANSIENTS ON DC LINES	TG	JUERGER	1	//3		14,3056

4 CRATES, SUPPLIES, COMPONENTS, ACCESSORIES

41 Crates and Related Components/Accessories — Crates with/without Dataway and Supply, Blank Crates, Crate Ventilation Gear

411 Crates with Dataway and Supply

	CRATE (270VA,COOLED,MODULAR POWERED BY MAX 8X1922 OR 1X1923/1925 + MAX 4X1922)	1902A	BORER	25	/69		14,4001
	VOLTAGE REGULATOR (FOR +OR=24V/6A, +/=12V/7A,+/=6V/8A/16A/24A)	1922			/69		
	VOLTAGE REGULATOR (+&=6V 25A MAX, OR 40A MAX WITH EXTERNAL +6V SUPPLY)	1923			/74		
	VOLTAGE REGULATOR (+AND=6V, 25A MAX, 270W RATING, USABLE WITH 4X1922)	1925			/75		
	CAMAC MINICRATE (19 INCH RACK MOUNTING) (+6V/15A,=6V/5A, +24V/2A,=24V/2A,200W)	307,100CC	EDS SYSTEMTECHNIK	17	/73	(10)	14,4002
	POWERED CRATE	MC200	EG&G/ORTEC	25	/74		14,4003
	POWERED CRATE (INCL, CRATE AND POWER SUPPLY COOLING TO SUPPL CP 1 SPEC)	PS 004/PA1/VC 0040	GEC=ELLIOTT	25	05/75		14,4004
	POWERED CRATE (+&=6V/40A, +&=24V/8A, 200V/,1A, 117V AC, MAX 300W)	CPC/14	GRENSON		/73		14,4005
N	POWERED CRATE (+&=6V/20A, +&=24V/5A, 200V/0,03A, 117VAC/0,5A, MAX 200W)	CPC/15			10/75		
C	POWERED CRATE	1500/25	KINETIC SYSTEMS	NA	/73		14,4006
N	POWERED CRATE (42A CAPABILITY ON +6V)	1500/42	KINETIC SYSTEMS	NA			14,4007
N	POWERED CRATE (MAX 400W, +&=24V/3A, +&=12V/3A,+&=6V/24A,=6V/6A,+200V/,1A,AC)	CAM 9,01	METRIMPEX	24	/72		14,4008
	POWER CRATE (9070 CRATE WITH 9022 POWER SUPPLY)	9071	NUCL, ENTERPRISES	24	/74	(12)	14,4009
	POWERED CRATE (+AND=6V/25A, +AND=24V/6A, (INCL POWER DESIGN TYPE AEC432 SUPPLY)	NSI=875CC100AEC432	NUCL, SPECIALTIES	25	/72		14,4010
C	POWERED CRATE (6U,VENTILATED,NO FAN,130W +6V/15A,=6V/4A,+AND=24V/2A,+200V/50MA)	2000	PULON	25	/71		14,4011
	POWERED CRATE	CCMN=CSAN	RDT	25	/71		14,4012
	POWERED CRATE(SEE P7 ALJ 13)	C7 ALJ 13 DW	SAPHYMO=STEL	25		(1)	14,4013
	POWER SUPPLY (CAMAC CRATE)	CM5125/53/DW/BLOCS	SAPHYMO=STEL	25	/72		14,4014
	POWERED VENTILATED CRATE (+6V/24A, =6V/16A, +AND=24V/3A, MAX 400W)	C JAL=41	SCHLUMBERGER	25	/73	(8)	14,4015
	POWER CRATE (200W MAX,+6V/25A,=6V/10A, +AND=12V/3A,+AND=24V/3A,200V/0,05A)	PC 2006/B	SEN	25	/70		14,4016
	POWER CRATE (200W MAX,+6V/25A,=6V/10A, +AND=24V/3A,200V/0,05A)	PC 2006/C		25	/71		
	COMPLETE POWER CRATE	CPC 2057	SEN	25	/74	(11)	14,4017
N	POWERED CRATE (500W, +6V/65A OR 25A, =6V/25A OR 65A, MAX TOT CURRENT IS 80A)	HPC 2075	SEN	25		(14)	14,4018
N	POWERED CRATE (200W, +&=6V/10A, +&=12V/2A, +&=24V/3A)	SPC 2077	SEN	25		(14)	14,4019
	POWERED CRATE (7U,VENT,+AND=6V/20A,+AND=12V/6,5A,+AND=24V/6,5A,200V/0,1A,200W)	C 76455=A2	SIEMENS	25	/71	(3)	14,4020
	POWERED CRATE (SAME BUT WITH 117V AC)	C 76455=A1		25	/71		
	POWERED CAMAC CRATE	PCS/12	STND ENGINEERING	25	/72		14,4021
	POWERED CAMAC CRATE	PCS/42	STND ENGINEERING	25	/72		14,4022
	POWERED CRATE (SEE CRATE C=CF AND SUPPLY P=156 FOR RATINGS)	C=CF + P=156	WENZEL ELEKTRONIK	25	05/75		14,4023
	POWERED CRATE (SEE C=CF & SUPPLY P=264)	C=CF + P=264		25	03/75		
C	POWERED CRATE (SEE C=CF & SUPPLY P=300F)	C=CF + P=300F		25	04/75	(14)	

412 Crates with Dataway, without Supply

	VENTILATED CRATE (HEAVY DUTY 25 STATION FASTON CONNECTORS, 6U HIGH)	VC 0022	GEC=ELLIOTT	25	/74		14,4024
	(SAME BUT WITH ALL PATCH LINES BUSSED AS PER COGELAB REQUIREMENTS)	VC 0030		25	/74		
	5U CRATE 25 STATION HEAVY DUTY, FITS TO PS 0004 USING ADAPTOR PA 1,	VC 0040	GEC=ELLIOTT	25	05/75		14,4025
	CONVERTS FASTON CONNECTORS TO RECOMMENDED FIXED POWER CONNECTOR ON CHOSEN CRATE	/AMP	GEC=ELLIOTT		/73		14,4026
	CAMAC CRATE VERDRAHTET (EMPTY CRATE WITH WIRED DATAWAY)	2,084,000,6	KNUERR	25	/73	(2)	14,4027

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	CRATE	9070	NUCL. ENTERPRISES	24	//4		14,4028
	CAMAC COMPATIBLE CRATE (WIRED)	NSI-875 DB-MV	NUCL. SPECIALTIES	25	//1		14,4029
	CAMAC CRATE (WIRED)	NSI-875 CC 100	NUCL. SPECIALTIES	25	//2		14,4030
N	UNPOWERED CRATE WITH DATAWAY (5U, VENTILATED, NO FAN, 25 STATIONS)	002	POLON	25	//5		14,4031
	UNPOWERED CRATE WITH DATAWAY (6U, EMPTY, VENTILATED, NO FAN)	012	POLON	25	//1		14,4032
	UNPOWERED CRATE WITH DATAWAY (360 MM) (525 MM)	CM 5125/53/DW CM 5125/53/DW	SAPHYMO-STEL	25 25			14,4033
	UNPOWERED CRATE WITH DATAWAY AND CONNECTORS	UPC 2029	SEN	25	//0		14,4034
	CRATE (WIRED CRATE)	WCS	STND ENGINEERING	25	//2	(5)	14,4035
C	WIRED CRATE (HEAVY DUTY, 3 FAN & MONIT, UNIT, 6U, USE WITH P-156, P-264, P-300F)	C-CF	WENZEL ELEKTRONIK	25	03/75	(14)	14,4036
	CRATE (WITH DATAWAY AND VENTILATION)	C 76455-A3	SIEMENS	25	//2		14,4037

413 Crates without Dataway, with Supply

	CAMAC CRATE (+6V/25A,-6V/12,5A,+&-24V/6A,+&-12V/4A)	DD 200-3001	DORNIER	NA	//4		14,4038
	(SAME WITHOUT +&-12V SUPPLY)	DD 200-3002		NA	//4		

417 Blank Crates and Other Components and Accessories

N	RACK BLOWER (1 U HIGH, MAY BE USED WITH AIR SCOUP NSI-12109-AS FOR HI EFFIC,)	NSI-05235-RB	NUCL. SPECIALTIES	NA	07//5		14,4039
	CRATE (5U,EMPTY, 25 STATIONS)	MCF/5CAM/S/25	IMHOF-BEDCO	25	//1		14,4040
	(SAME BUT WITH 24 STATIONS)	MCF/5CAM/S/24		24	//2		
	CRATE (6U,EMPTY,WITH VENTILATION BAFFLE, 25 STATIONS, HARWELL TYPE 7000)	MCF/6CAM/SV/25		25	//1		
	(SAME BUT WITH 24 STATIONS)	MCF/6CAM/SV/24		24	//2		
	CRATE (6U,EMPTY,WITH VENTILATION BAFFLE, REMOVABLE PANEL, 25 STNS, HARWELL 7000)	MCF/6CAM/SVR/25		25	//1		
	(SAME BUT WITH 24 STATIONS)	MCF/6CAM/SVR/24		24	//2		
	CAMAC CRATE (EMPTY)	2,080,000,6	KNUERR	25	//0	(2)	14,4041
	CAMAC CRATE (EMPTY,INCL HARDWARE SUPPLY CHASSIS AND VENTILATION PANEL)	2,080,000,6		25		(2)	
	CAMAC COMPATIBLE CRATE	NSI 875 DB/MV	NUCL. SPECIALTIES	25	//0		14,4042
	CAMAC CRATE (UNWIRED)	NSI 875 CC 100	NUCL. SPECIALTIES	25	//2	(5)	14,4043
	CHASSIS CAMAC (6 UNITES AVEC PENTE DE VENTILATION, 525 MM PROFONDEUR)	9905-1-05	OSL	25	//1		14,4044
	(360 MM PROFONDEUR)	9905-2-05		25	//1		
	CAMAC CRATE WITH VENTILATION BAFFLE (6U, 525MM DEPTH)	9905MVDJ/98/525	OSL	25			14,4045
	(SAME BUT WITH 460MM DEPTH)	99055MVJAVD/98/460		25			
	(SAME BUT WITH 360MM DEPTH)	99055MVJAVD/98/360		25			
	CRATE (6U, EMPTY, VENTILATED, NO FAN)	010	POLON	25	//1		14,4046
	VENTILATED CRATE NO POWER NO DATAWAY (TWO FANS)	CCMN	ROT	25	//1		14,4047
	(SAME WITH 3 FANS)	CCMNA		25	//2		
	UNPOWERED CRATE	UC 2057	SEN	25	//4	(11)	14,4048
	CAMAC CRATE (EMPTY CRATE)	C	STND ENGINEERING	25	//2		14,4049
	CHASSIS CAMAC NORMALISE 5U (EMPTY CRATE,360 MM DEEP)	40206	TRANSRACK	25	//4		14,4050
	(*=7 FOR 460MM & *=8 FOR 525MM DEEP)	4020*		25			
	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U TOTAL,360MM DEEP,VENTILATION HARDWARE)	40203	TRANSRACK	25	//4		14,4051
	(*=4 FOR 460MM & *=5 FOR 525MM DEEP)	4020*		25			
	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U TOTAL,360MM DEEP,WITH TWO FANS)	40200	TRANSRACK	25	//4		14,4052
	(*=1 FOR 460MM & *=2 FOR 525MM DEEP)	4020*		25			
	CAMAC CRATE (EMPTY) HEAVY DUTY		OSL/WILLSHER&QUICK		//3		14,4053
	6U WITH VENTILATION BAFFLE	9905-5MV		25	//3		
	5U NON VENTILATED	9905-5H		25	//3		
	DEPTH OPTIONS 360MM, 460MM, 525MM						
	CAMAC CRATE WITH VENTILATION BAFFLE (6U, 525MM DEPTH)	99055MVJAVD/98/525	OSL/WILLSHER&QUICK	25	//3		14,4054
	(SAME BUT WITH 460 MM DEPTH)	99055MVJAVD/98/460		25	//3		
	(SAME BUT WITH 360 MM DEPTH)	99055MVJAVD/98/360		25	//3		
	VENTILATION UNIT	CAM/FV	IMHOF-BEDCO		//3		14,4055

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	LUFTEREINHEIT (VENTILATION UNIT,COMPLETE WITH 3 FANS AND FILTER)	2,081,000,6	KNÜRR		//0		14,4056
	(VENTILATION UNIT,NO FAN,NO FILTER)	2,085,000,6					
	AIR SCOOP (STOPS CHIMNEY EFFECT BETWEEN UN-VENTILATED CRATES IN RACK, 1U HIGH)	NSI-12109-AS	NUCL. SPECIALTIES	NA	//1		14,4057
	VENTILATION MODULE	VM 2057	SEN		//4	(11)	14,4058
	1U VENTILATION GRILL	1 UG	OSL/WILLSHER&QUICK		//2		14,4059
	CARD EXTENDER (FOR SUPPLY OF 2057)	CE 2061	SEN				14,4060

42 Supplies and Related Components/Accessories — Single- and Multi-Crate Supplies, Blank Supply Chassis, Control Panels, Supply Ventilation

421 Multi-Crate Supplies

	POWER SUPPLY FLEXIBLE SYSTEM (TO SPECS CERN-ISR-CO/72-43), COMPRISING	CPU/10	GRENSUN		//1		14,4061
	BASIC CRATE(FOR SUPPLY MODULES,INCLUDES REFERENCE,CONTROL AND 200V/0,1A)	CFC					
	SUPPLY MODULE(* IN TYPE = P FOR POS AND N FOR NEG OUTPUT VOLTAGE 6V/ 6A)	CF*/6					
	(12V/ 3A)	CF*/12					
C	(24V/ 3A)	CF*/24					
	POWER SUPPLY SYSTEM (CRATE) (MODULE OPTIONS AS FOLLOWS)	C48MT204/C68MT306	SAPHYMO-STEL		//2		14,4062
	POWER SUPPLY MODULE 6 V/10 A (6V/20A & 6V/40A OPTIONS ALSO AVAILABLE)	BP /5 6,10					
	12 V/ 2 A (ALSO 12V/4A, 7A, 15A & 25A OPTIONS)	BSN					
	24 V/ 1,2A (ALSO 24V/2,5A, 3,5A, 9A & 15A OPTIONS)	BSN					

422 Single-Crate Supplies

	POWER SUPPLY AND COOLING UNIT (+6V/42A, -6V/25A,+&-24V/6A, 375W, 2U FAN UNIT)	PS 0004	GEC-ELLIOTT		05/75		14,4063
	CAMAC POWER UNIT (+6V/15A,-6V/3A,+24V/2A -24V/2A,200V/0,05A,117VAC)	CPU/4	GRENSUN				14,4064
	CAMAC POWER SUPPLY - RACK MOUNTING (+6V/20A,-6V/5A,+AND-24V/5A,200V/0,05A)	CPU/2	GRENSUN		//1		14,4065
	CAMAC POWER SUPPLY - RACK MOUNTING (+6V/20A,-6V/5A, +&-12V/2A, +&-24V/3A)	CPU/5	GRENSUN		//1		14,4066
	POWER SUPPLY (RACK MOUNTING,+6V/25A, -6V/15A,+AND-24V/5A,200V/0,1A)	CPU/6	GRENSUN		//1		14,4067
	POWER SUPPLY (RACK MOUNTING,+6V/25A, -6V/15A,+AND-24V/5A,+AND-12V)	CPU/7	GRENSUN		//1		14,4068
	POWER SUPPLY (+6V/20A,-6V/5A, +AND-24V/5A,200V/0,05A)	9001	NUCL. ENTERPRISES		//1		14,4069
	POWER UNIT (+6V/15A,-6V/3A, +AND-24V/2A,200V/0,05A)	9022	NUCL. ENTERPRISES		//1	(2)	14,4070
	POWER SUPPLY (BACK MOUNTING,+6V/15A, -6V/4A,+AND-24V/2A,+200V/50MA,130W)	C2C-10	PULON		//3		14,4071
	POWER UNIT (+6V/20A, -6V/15A,+24V/2A, -24V/2A,200V/0,1A)	SP 426	POWER ELECTRONICS		//4		14,4072
	POWER UNIT (+6V/25A, -6V/25A, +24V/5A, -24V/5A, 200V/100MA)	SP 558	POWER ELECTRONICS		//5		14,4073
	POWER SUPPLY (+6V/25A,-6V/5A, +AND-12V/2A,+AND-24V/3A,200V/0,1A)	C 303	RDT		//1		14,4074
	POWER SUPPLY UNIT -MAINTENANCE ONLY- (+6V/10A,-6V/2A,+AND-24V/1,5A)	P4 ALJ 13	SAPHYMO-STEL		//1		14,4075
	(+6V/5A,-6V/1,5A,+AND-12V/1,5A, +AND-24V/1,5A) -MAINTENANCE ONLY-	P6 ALJ 13					
	(+6V/25A,-6V/10A,+AND-12V/3A, +AND-24V/3A,+200V/0,1A,MAX 200W)	P7 ALJ 13	SAPHYMO-STEL				14,4076
	POWER SUPPLY (+6V/32A,-6V/32A,+24V/6A, -24V/6A,+200V/,1A,300W, POWER FAIL LAM)	PS 2057	SEN		//4	(11)	14,4077
	SUPPLY (+AND-6V/26A,+AND-12V/6,5A,+AND-24V/6,5A,200V/0,1A,117V AC, 200W MAX)	C 76455-A4	SIEMENS		//2		14,4078
	SUPPLY (SAME BUT WITHOUT 117V AC)	C 76455-A5			//2		
	POWER SUPPLY (+AND-6V/6A SHARED AND +AND-24V/2A SHARED, METERING OF V AND I)	825	STND ENGINEERING		//2		14,4079
	POWER SUPPLY AND BLOWER UNIT	1410	STND ENGINEERING		//2	(5)	14,4080
	CAMAC POWER SUPPLY	1510/12	STND ENGINEERING	NA	//2		14,4081

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	CAMAC POWER SUPPLY	1510/42	STND ENGINEERING	NA	//2		14,4082
C	PLUG-IN POWER SUPPLY 156W (+-6V/8A, +-12V/2A,+-24V/1A,117VAC)	P-156-1	WENZEL ELEKTRONIK		05//5		14,4083
C	PLUG-IN POWER SUPPLY 264W (+-6V/10A, +-12V/2A,+-24V/2A,117VAC,OPT,+200V/40MA)	P-264			03//5		
	PLUG-IN POWER SUPPLY 300W&FAN(+-6V/32A, +-12V/3A,+-24V/6A,+200V/100MA,117VAC)	P-300F			04//5		

427 Blank Supply Chassis, Other Components/Accessories

POWER SUPPLY CRATE (STANDARD)	MCF/4/PPC	IMHOF-BEDCO	NA	//1		14,4084
POWER SUPPLY CRATE (WIRED)	MCF/PPC/WV		NA	//1		
NETZTEILCHASSIS (EMPTY SUPPLY CHASSIS)	2,082,000,6	KNOERR		//0		14,4085
POWER SUPPLY CRATE(FOR SEPARATE SUPPLY)	CSAN	RDT		//1		14,4086
MAINS SWITCH ASSEMBLY	MS 3	GEC-ELLIOTT	NA	//1		14,4087
POWER INDICATOR	0704	NUCL. ENTERPRISES	NA	//0		14,4088

43 Recommended or Standard Components/Accessories — Branch Cables, Connectors etc., Dataway Connectors, Boards etc., Blank Modules, Other Stnd Components

431 Branch Related (Cables, Connectors etc.)

BRANCH HIGHWAY CABLE	8102	BI NA SYSTEMS	//3		14,4089
BRANCH HIGHWAY CABLE	BH001	EG&G/ORTEC	//1		14,4090
BRANCH HIGHWAY CABLE (WITH CONNECTORS, 27 CM LONG)	BHC 027	GEC-ELLIOTT	//2		14,4091
SAME,***=067,107 & 207 FOR CORRESP LENGTH IN CM,OTHER LENGHTS TO SPEC ORDER	BHC ***		//2		
BRANCH HIGHWAY CABLE ASSEMBLY (WITH CONNECTORS,27 CM LONG)	CC 66 PUL PB-27	HUGHES	//1		14,4092
(XX CM LONG,PVC JACKET)	CC 66 PUL PB-XX				
BRANCH HIGHWAY CABLE (COMPLETE PTFE CABLE ASSEMBLY,27CM LONG)	CD 18067-27	HUGHES	//0		14,4093
(***= 107, 207 = OR CUSTOMER SPECIFIED = FOR CORRESPONDING LENGTH IN CM)	CD 18067/***		//1		
BRANCH HIGHWAY CABLE		JOERGER			14,4094
BRANCH CABLE WITH CONNECTOR (1,5 FT TO 75 FT LONG)		JORWAY	//1		14,4095
BRANCH HIGHWAY CABLE (66 TWISTED PAIRS)	CL 90	SCHLUMBERGER	//1		14,4096
BRANCH HIGHWAY CABLE ASSEMBLY (COMPLETE WITH CONNECTORS, LENGTH 27 CM)	BHC 27	SEMRA-BENNEY	//2		14,4097
(SAME, XXX=LENGTH IN CM, 040,100 ETC)	BHC XXX		//2		
BRANCH HIGHWAY CABLES(COMPLETE WITH CONNECTOR,XXX = LENGTH IN METERS)	2000/132/XXX	TEKDATA	//1	(4)	14,4098
BRANCH HIGHWAY CONNECTOR (FREE MEMBER, PIN MOULDING WITH METAL PIN PROTECTOR)	MSS0132P08BN527-M	HUGHES	//3		14,4099
BRANCH HIGHWAY CONNECTOR (FIXED MEMBER,SOCKET MOULDING)	MSS0132S00BN000	HUGHES	//0		14,4100
(FREE MEMBER,PIN MOULDING, PXX YYY SELECTS JACKSCREW)	MSS0132PXXBNYYY				
HOOD (FOR FREE MEMBER)	MAC 0132 H005				
EXTENDED BRANCH CABLE (LOW COST TELE-PHONE CABLE FOR LONG BRANCH RUNS)	EBC XXXX	GEC-ELLIOTT	//2		14,4101
BRANCH HIGHWAY CABLE ONLY (PLAIN PVC JACKET)	66 PUL PB	HUGHES	//1		14,4102
BRANCH HIGHWAY CABLE (132-WAY)	LIY-Y72X2X0,088	LEONISCHE	//2		14,4103
BRANCH HIGHWAY CABLE (TRUE 132-WAY WITH METALISED POLYESTER SCREEN, PVC JACKET)	LI2Y(ST)Y66X2X0,18	LEONISCHE			14,4104
C CABLE FOR BRANCH HIGHWAY (PVC JACKET)	132 PE 189	PRECICABLE	//1		14,4105
C (BRAIDED RILSAN JACKET)	132 PE 210				
C (MEPLAT 20MMX10,8MM,GAINE PVC NOIR)	132 PE 291		//2		
CABLE EXTENSION MODULE (JOINS TWO BRANCH HIGHWAY CABLES)	CD 18106	HUGHES	//2		14,4106
BRANCH HIGHWAY TO PDP-11 (COMPLETE WITH CONNECTORS, XXX= LENGTH IN METERS)	5805/P/132/XXX	TEKDATA	//3	(8)	14,4107
BRANCH HIGHWAY JUNCTION BOX	5849	TEKDATA	//5		14,4108

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.

432 Dataway Related (Connectors, Boards, Assemblies)

	ADDRESS & FUNCTION DECODING PC	AFD 2066	SEN				14,4109
	DATAWAY MOTHERBOARD (MULTILAYER PNR)	DM=1	STND ENGINEERING		//2		14,4110
	DATAWAY MOTHERBOARD (WITH CONNECTORS)	1186	WEHRMANN		//4	(10)	14,4111
	DATAWAY SOCKET (MOTHERBOARD COMPLETE WITH 25 CONNECTORS)	CIM	RDT		//0		14,4112
	DATAWAY MINI WRAPPING (MOTHERBOARD WITH 25 DATAWAY CONNECTORS)	J/DW	SAPHYMO=STIEL		//1		14,4113
	DATAWAY MOTHERBOARD ASSEMBLY	DM 2	STND ENGINEERING		//2		14,4114
	DATAWAY CONNECTOR, EDGE TYPE II	1=163633=0	AMP AG		//0		14,4115
	(WIRE WRAP)						
	(TERMI=POINT/WIRE WRAP)	1=163634=0			//0		
	(MOTHERBOARD SOLDER)	1=163635=0			//0		
	(WIRE SOLDER)	1=163636=0			//0		
C	DATAWAY CONNECTOR WITH CARD GUIDES (HAND SOLDER, DIP SOLDER & MINI=WRAP)	PCBD43N/7=1E00	BURNDY	NA	//4		14,4116
	DATAWAY CONNECTOR (MINIWRAP)	EAA 043 D301	HUGHES		//1	(2)	14,4117
	CAMAC DATAWAY CONNECTOR (* INSERT A FOR SOLDER TAG, B SOLDER PIN, C MINI WRAP)	G03D 086P 26 * BL	ITT CANNON		//3	(6)	14,4118
	CAMAC=LEISTE(DATAWAY CONNECTOR,WIREWRAP)	4,000,060,0	KNUERR		//0		14,4119
	DATAWAY FEMALE CONNECTOR, MINI=WRAP	2422 061 04334	PHILIPS		//1	(5)	14,4120
	*=1 FOR WIRE SOLDER, 5 FOR BOARD SOLDER	2422 061 043*4				(5)	
	DATAWAY MALE CONNECTOR (MATING THE CRATE MOUNTED 86=WAY CONNECTOR SOCKET)	2422 060 14314	PHILIPS		//2	(5)	14,4121
	CONNECTEUR 254 DOUBLE FACE	254 DF 43 BWV	SOCAPEX		//0		14,4122
	(DATAWAY CONNECTOR,WIRE WRAP)						
	(MOTHERBOARD SOLDER)	254 DF 43 AYV			//0		
	(WIRE SOLDER)	254 DF 43 AZV			//0		
	DATAWAY CONNECTOR (MINI=WRAP)	8606.86 21 15 000	SOURIAU		//1		14,4123
	(WIRE=SOLDER)	8606 86 21 10 000					
	(FLOW SOLDER)	8606 86 21 14 000					
	DATAWAY CONNECTOR (*=2 FLOW SOLDER,*=3 SOLDER LUGS,*=4 MINIWRAP,AU PLATING)	C 288* CSP 221	UECL		//1		14,4124
	(FLOW SOLDER,NI + AU PLATING)	C 2885 CSP 221					
	(13 MINIWRAP CONTACTS,OTHER ARE FLOW SOLDER,NI + AU PLATING)	C 2886 CSP 221					
	(*=7 MINIWRAP,*=8 SOLDER LUGS, NI + AU PLATING)	C 288* CSP 221					
	MOUNTING BRACKETS FOR ABOVE	C 8523					
	DATAWAY CONNECTOR HOUD (43=WAY DOUBLE SIDED, 2,54 MM PITCH CONTACTS)	S 4051	TEKDATA	1	//5		14,4125

433 Module Related (Blank Modules, Patchboars etc.)

	CAMAC CARRYING CASE (TAKES 8 MODULES)	C/NCC8=4	HENESA		//3		14,4126
	CAMAC CARRYING CASE (TAKES 12 MODULES	C/NCC12=6	HENESA		//3		14,4127
	BLANK MODULE KIT (SINGLE WIDTH)	BM 1	GEC=ELLIOTT	1	//3		14,4128
	(SAME,*=2,3 & 4 FOR CORRESP WIDTH)	BM *					
	SINGLE CARD MOUNTING KIT	CAM/M1/A	IMHOF=BEDCO	1	//2		14,4129
	(EMPTY MODULE,SHORT SCREEN PLATE)						
	(SAME,*=2,3 & 4 FOR CORRESP WIDTH)	CAM/M*/A			//3		
	SINGLE CARD MOUNTING KIT (EMPTY MODULE,	CAM/M1/B		1	//2		
	(EMPTY MODULE,LONGT SCREEN PLATE)						
	(SAME,*=2,3 & 4 FOR CORRESP WIDTH)	CAM/M*/B			//3		
	CAMAC HARDWARE	CM=001	KINETIC SYSTEMS	1	//1	(4)	14,4130
	CAMAC=KASSETTE (EMPTY MODULE,WIDTH 1/25)	2,090,001,8	KNUERR	1	//0	(2)	14,4131
	(*=2,3,4,5,6 FOR CORRESPONDING WIDTHS)	2,090,00*,8			//0		
	CAMAC COMPATIBLE MODULE (EMPTY, WIDTH=1, ALSO IN 2 & 3 UNIT WIDTHS)	NSI 875 DM	NUCL, SPECIALTIES	1	//0		14,4132
	CAMAC MODULE (EMPTY MODULE HARDWARE)	NSI 875 CM=100=1	NUCL, SPECIALTIES	1	//2	(5)	14,4133
	(SAME, *= 2, 3, & 4 FOR CORRESP WIDTH)	NSI 875 CM=100=*			//2	(5)	
	CAMAC MODULE,SHIELDED (EMPTY, 1 WIDTH)	NSI=875=DM/SPH=1	NUCL, SPECIALTIES	1	//1		14,4134
	(SAME, *=2, 3, AND 4 FOR CORRESP WIDTH)	NSI=875=DM/SPH=*			//1		
	CAMAC MODULE (EMPTY,*=1/25)	021	POLON	1	//1		14,4135
	(*=2,3,4,6 & 8 FOR CORRESP WIDTH)	02*			//1		
	(*=0&2 FOR WIDTH 10 & 12 RESPECTIVELY)	03*			//1		
	EMPTY MODULE 1 UNIT	CCA 1	RDT	1	//0		14,4136
	(SAME,*=2,3 & 4 FOR CORRESP WIDTH)	CCA *					

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	EMPTY MODULE SCREENED (1 WIDE, ADD TYPE SUFFIX A FOR SHORT, B FOR LONG SCREENS) (DITO, *=2,3,4 OR 6 FOR CORRESP WIDTH)	CM1 CM*	SEMRA-BENNEY	1	/73		14,4137
	MODULE HARDWARE (EMPTY MODULE, W=1/25, ALSO AVAILABLE W=2/25,3/25 & UP TO 8/25)		STND ENGINEERING	1	/72		14,4138
	TIROIRE MODULAIRE POUR CARTE BASCULANTE (EMTY MODULE FOR HINGED CARD) TIROIRE MODULAIRE POUR 2 CARTES BASCUL, (EMTY MODULE FOR 2 HINGED CARDS)	41405 41406	TRANSRACK	2 3	/72 /72		14,4139
	TIROIR MODULAIRE (EMPTY MODULE,W=1/25) (*=2,3,4 & 5 FOR CORRESPONDING WIDTH)) (**=06,08,10 AND 12 FOR CORRESP WIDTH)	TM 50125 TM 50*25 TM 5**25	TRANSRACK	1	/70		14,4140
	CAMAC MODULE (EMPTY,1/25 CARD MODULE) (*=2,3 & 4 FOR CORRESPONDING WIDTH)	CAMCAS 1 CAMCAS *	WILLSHER & QUICK	1	/71	(2) (2)	14,4141
	CAMAC MODULE (EMPTY,1/25 CARD MODULE) (*=2,3 & 4 FOR CORRESPONDING WIDTH)	CAMCAS 1-G CAMCAS *-G	WILLSHER & QUICK	1	/72 /72		14,4142
	CAMAC MODULE(EMPTY,1/25 SCREENED MODULE) (*=2,3 & 4 FOR CORRESPONDING WIDTH)	CAMMOD 1-G CAMMOD *-G	WILLSHER & QUICK	1	/72 /72		14,4143
	CAMAC MODULE(EMPTY,2/25 SCREENED MODULE) (*=3 & 4 FOR CORRESPONDING WIDTH)	CAMMOD 2 CAMMOD *	WILLSHER & QUICK	2	/71	(2) (2)	14,4144
	EMTY MODULE WITH HINGED CARDS (2/25) (3/25)	9905-CB2 9905-CB3	OSL/WILLSHER&QUICK	2 3	/73 /73		14,4145
	EMPTY MODULE (1/25) (**= T2, T3, T4, T5, T6, T8, T10, AND T12 FOR CORRESPONDING WIDTH)	9905-5T1 9905-5**	OSL/WILLSHER&QUICK	1	/73 /73		14,4146
	TIROIR MODULAIRE POUR COMMANDE	9905-TC-1	OSL	1	/71		14,4147
	TIROIR MODULAIRE DE COMMANDE (SUPPLY CONTROL MODULE)	41703	TRANSRACK	1	/70		14,4148
	BLANK CAMAC MODULE PC BOARD (GOLD PLATED & ETCHED FINGERS BOTH SIDES)	NSI-04071-PC	NUCL, SPECIALTIES		/71		14,4149
	GENERAL-PURPOSE IC PATCH BOARD	18605	VERO ELECTRONICS		/74		14,4150
	MK-1 KLUGE MODULE (131 MIXED 14, 16, 24 PIN SOCKETS)	8301	BI HA SYSTEMS	2	/73		14,4151
	MK-5 KLUGE MODULE (HAS 70 14 PIN, 13 AND 2 24 PIN WIRE WRAP SOCKETS)	8305		2	/73		
	MK-6 KLUGE MODULE (HAS 34 14 PIN, 16 16 PIN & 3 24 PIN WIRE WRAP SOCKETS)	8306		1	/73		
	CAMAC-UNIVERSAL-BOARD(PRINTED CARD MODULE WITH 28 14-PIN + 28 16-PIN SOCKETS)	DD 200-2900	DUNNIER	2	/71		14,4152
	CAMAC PROTOTYPE ASSEMBLY BOARDS (MX B1 HAS 68 SITES, MX B2 HAS 80 SITES) (MX B3 HAS 68 SITES,MX B4 HAS 80 SITES, MX B3/MX B4 INCLUDE 5V CIRCUIT)	MX B1/MX B2 MX B3/MX B4	GEC-ELLIOTT	NA NA	/71 /71		14,4153
	PRINTED CIRCUIT TEST BOARD	10	JORWAY	1	/71		14,4154
	KLUGE BOARD FOR WIRE WRAP	15	JORWAY	3	/74		14,4155
	KLUGE CARD (FOR CREATING YOUR OWN CAMAC MODULES)	2000-36	KINETIC SYSTEMS	1	/71	(4)	14,4156
C	KLUGE WITH 52 POSITION 2D CONNECTOR	2000-52		1	/73		
N	KLUGE WITH 25 POSITION D CONNECTOR	2000-25		1			
	EXPERIMENTIERPLATTE (PRINTED CIRCUIT BOARD)	4,000,087,0	KNUERR	NA	/70		14,4157
	EXPERIMENTIERPLATTE ($P_1C_1B_1$)	4,000,088,0		NA	/73		
	DECODED MATRIX BOARD (FOR PROTOTYPE WIRING OF 64 14-PIN SITES, A&F DECODED)	D 21 621	NUCL, ENTERPRISES	0	/74		14,4158
	MODULE PRINTED CIRCUIT BOARDS(TAKE 24,16 OR 14 PIN, ON THE WHOLE 1092 PINS)	CBP 1	RDT	NA	/72		14,4159
	(SAME, WITH MINI-WRAP TO 0V AND +6V)	CBP 2		NA	/72		
	BLANK MODULE(COMPLETE WITH PRINTED BOARD FOR 69 INTEGRATED CIRCUITS,1 U WIDTH)	BM 2020/1U	SEN	1	/70		14,4160
	(SAME,2U WIDTH)	BM 2020/2U		2	/70		
	EXPERIMENT PLATE	C 72468-A453-A1	SIEMENS	1	/72		14,4161

437 Other Recommended or Standard Components/Access.

N	RIBBON CABLE FOR LAM GRADER (XXX DENOTES LENGTH IN METERS)	S 4003/XXX	TEKDATA			(14)	14,4162
	NIM/CAMAC ADAPTOR	NCA-1	GEC-ELLIOTT		/74		14,4163
	NIM ADAPTOR	9072	NUCL, ENTERPRISES		/74		14,4164
	NIM-CAMAC ADAPTOR	CAN	RDT	NA	/71		14,4165
	NIM/CAMAC ADAPTOR	ANC 10	SCHLUMBERGER		/72		14,4166

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	CAMAC NIM ADAPTOR	CNA 2033	SEN	2	//1		14,4167
	LAM GRADER CABLE (20CM, WITH CONNECTORS) (40CM, WITH CONNECTORS)	LGC 20 LGC 40	GEC-ELLIOTT		//2 //2		14,4168
	LAM GRADER CABLE		JUERGER				14,4169
	52 WAY CANNON 20B52S HARNESSES LAM GRADER CABLE, XXX= LENGTH IN METERS)	5809/S/52/XXX	TEKDATA		//3		14,4170
	LAM GRADER CONNECTOR (52-PIN FIXED MEMBER, TAKES PIN TYPE 031-9540-000)	2 DB 52 P	ITT CANNON		//0		14,4171
	COAXIAL CONNECTOR (PANEL MOUNTING, CABLE CONNECTOR HAS TYPE F 00,250 & FS 00,250) T- & L-ADAPTERS, FREE DOUBLE SOCKET, AND ARE ALSO AVAILABLE	RA 00,250	LEMO		//0	(4)	14,4172

INDEX OF MANUFACTURERS

AEG-Telefunken
Elisabethenstrasse 3, Postfach 830
D-7900 Ulm, Germany

AMP AG
Haldenstrasse 11
CH-6000 Luzern, Switzerland

Applied Computer Systems Ltd.
2 Charlton Street,
Manchester M1 3JL, England

Arsycom B.V.
Kabelweg 43-47,
Amsterdam 1016, Netherland

BF Vertrieb GmbH
(Sales of F & H Products in Germany)
Bergwaldstrasse 30, Postfach 76
D-7500 Karlsruhe 41, Germany

BI RA Systems, Inc.
3520 D Pan American Freeway, N.E.
Albuquerque, New Mexico 87107,
USA

Borer Electronics AG
Postfach
CH-4500 Solothurn 2, Switzerland

N Borer Electronics
Box 17-126
West Hartford, CT 06117, USA

Burndy Electra AG
Hertistrasse 23,
CH-8304 Wallisellen, Switzerland

Cannon Electric GmbH
Bureau Schweiz
Friedenstrasse 15,
CH-8304 Wallisellen, Switzerland

Christian Rovsing A/S
Marielundvej 46B
DK-2730 Herlev, Denmark

N Computer Technology Limited
Eaton Road. Hemel Hempstead
Hertfordshire HP2 7EQ, England

Digital Equipment Corporation (DEC)
146 Main Street, Maynard
Massachusetts 01754, USA

Digital Equipment GmbH
Wallensteinplatz 2,
D-8000 München 40, Germany

Dornier System
Vertrieb Elektronik, Abt. VCE
Postfach 648
D-799 Friedrichshafen, Germany

EDS Systemtechnik GmbH
Trierer Strasse 281
D-5100 Aachen, Germany

EG & G/ORTEC, Inc.
High Energy Physics Department
500 Midland Road, Oak Ridge,
Tennessee 37830, USA

J. Eisenmann, Elektronik für
Prozessautomatisierung
Vogesenstrasse 6
D-7513 Stutensee-Buechig, Germany

Emihus — See Hughes

Frieseke & Hoepfner GmbH
Export Dept. & Production
Tennenloher Strasse
D-8520 Erlangen-Brück, Germany

Frieseke & Hoepfner
See also BF Vertrieb
(Sales of F & H Products in Germany)

GEC-Elliott Process Automation Ltd.
Camac Group, New Parks
Leicester LE3 1UF, England

Grenson Electronics Limited
Long March Industrial Estate
High March Road, Daventry
Northants NN11 4HQ, England

Hans Knuerr KG
Ampfingstrasse 27
D-8000 München 8, Germany

High Energy & Nuclear Equipment SA
2, Chemin de Tavernay,
CH-1218 Grand-Saconnex,
Switzerland

Hughes Microcomponents Limited
Clive House
12-18 Queens Road, Weybridge,
Surrey, England

Hytec Electronics
Court Road, Maidenhead
Berkshire SL6 8LQ, England

IDAS (Informations-, Daten -und
Automationssysteme) GmbH
Kornmarkt 9
D-6250 Limburg/Lahn, Germany

Imhof-Bedco Standard Products Ltd
Colne Way Trading Estate, By-Pass,
Watford, Herts, England

Informatek
Z.A. de Courtabœuf, B.P. 81
F-91401-Orsay, France

ITT Cannon — See Cannon

J and P Engineering (Reading) Ltd.
Portman House
Cardiff Road, Reading
Berkshire RG1-8JF, England

C Joerger Enterprises, Inc
32 New York Avenue
Westbury, N.Y. 11590, USA

Jorway Corporation
27 Bond Street, Westbury,
New York 11590, USA

Kinetic Systems Corporation
Maryknoll Drive,
Lockport, Ill. 60441, USA

C Kinetic Systems International S.A.
6, Chemin de Tavernay,
CH-1218 Grand Saconnex (Geneva)
Switzerland

Knuerr — See Hans Knuerr

Laben (Division of Montedel)
Via Edoardo Bassini, 15
I-20133 Milano, Italy

Le Croy Research Systems Corp.
126 North Route 303, West Nyack,
New York 10994, USA

Le Croy Research Systems SA
81, Avenue Casai
CH-1216 Cointrin, Geneva
Switzerland

Lemo SA
CH-1110 Morges, Switzerland

Leonische Drahtwerke AG
Abholfach
D-8500 Nürnberg 1, Germany

LRS-LeCroy — See LeCroy

N Metrimpex
P.O. Box 202
H-1391 Budapest 62, Hungary

Nuclear Enterprises Limited
Bath Road, Beenham
Reading RG7 5PR, England

Nuclear Enterprises Inc.
935 Terminal Way
San Carlos, California 94070, USA

Nuclear Specialties Inc.
6341 Scarlett Court, Dublin,
California 94566, USA

Nucletron SA
11, Chemin G. de Prangins
CH-1004 Lausanne, Switzerland

Numelec S.A.
Division Electronique Nucléaire
2, Petite Place,
F-78000 Versailles, France

ORTEC Incorporated
Software Dev, Digital Data Systems
100, Midland Road, Oak Ridge,
Tennessee 37830, USA

ORTEC GmbH
Frankfurterring 81
D-8000 München 40, Germany

O.S.L.
18bis, Avenue du Général de Gaulle
F-06340 La Trinité, France

OSL/Willsher and Quick — See OSL
respectively Willsher and Quick

Packard Instrument Company, Inc.
Subsidiary of AMBAC Industries, Inc.
2200 Warrenville Rd.,
Downers Grove, Illinois 60515, USA

Polon
Nuclear Equipment Establishment
00-086 Warsaw, Bielanska 1, Poland

Power Electronics (London) Limited
Kingston Road Commerce Estate
Leatherhead, Surrey, England

C Precicable
151, Rue Michel-Carré
F-95101 Argenteuil, France

RDT, Ing. Rosselli Del Turco
Rossello S.R.L.
Via di Tor Cervara, 261
Casella postale 7207
Roma Nomentano
I-00155 Rome, Italy

Réalisations Études Électroniques
(R 2 E)

Zone d'Activités de Courtabœuf
F-91, 403 Orsay, France

Rovsing — See Christian Rovsing

Saphymo-Stel
51, rue de l'Amiral-Mouchez
F-75013 Paris, France

Schlumberger Instruments &
Systèmes
Dépt. Instrumentation Nucléaire
B.P. 47 (57, rue de Paris)
F-92222 Bagneux, France

Semra-Benney (Electronics) Limited
Industrial Estate,
Chandler's Ford, Eastleigh,
Hampshire SO5 3DP, England

SEN Electronique
31, Avenue Ernest-Pictet, C.P. 57
CH-1211 Genève 13, Switzerland

C Sension Limited
Manor Lane, Holmes Chapel, Crewe
Cheshire CW4 8AB, England

Siemens AG
Bereich Mess- und Prozesstechnik
Postfach 21 1080
D-7500 Karlsruhe 21, Germany

SOCAPEX (Thomson-CSF)
9, Rue Edouard Nieuport
F-92153 Suresnes, France

Software Partners
Grossgerauer Weg 2
D-61 Darmstadt, Germany

Souriau et Cie
13, Rue Gallieni, B.P. 410
F-92 Boulogne-Billancourt,
Hauts-de-Seine, France

Standard Engineering Corporation
44800 Industrial Drive,
Fremont, California 94538, USA

Tekdata Limited
Westport Lake, Canal Lane,
Tunstall, Stoke-on-Trent,
Staffs ST6 4PA, England

N Tektronix, Inc.
P.O. Box 500, Beaverton,
Oregon 97005, USA

Telefunken — See AEG-Telefunken

Transrack
B.P. 12
22, Avenue Raspail
F-94100 Saint-Maur, France

Ultra Electronics (Components) Ltd
Fassetts Road, Loudwater,
Bucks. HP10 9UT, England

Vero Electronics Ltd.
Industrial Estate, Chandler's Ford,
Eastleigh, Hants SO5 3ZR, England

Karl Wehrmann, Industrievertr.
Spaldingstrasse 74
D-2000 Hamburg 1, Germany

Wenzel Elektronik
Wardeinstrasse 3
D-8000 München 82, Germany

Willsher and Quick Ltd.
Walrow, Highbridge
Somerset, England

CAMAC SOFTWARE PRODUCTS GUIDE

INTRODUCTION

The Software Products Section of the CAMAC Products Guide lists a number of software packages, programs and routines which have been developed by software firms, manufacturers of CAMAC equipment, and at research laboratories.

Work is going on to implement IML — the intermediate level CAMAC language. One contribution to IML implementation is listed below, but at least five other laboratories are at present engaged in implementing IML on several computers.

The products listed below are either in current use or will be so in the nearest few months. Some of the software listed is commercially available, information about other is presumably available from respective authors. The correctness of each entry has been carefully checked against data provided.

Inclusion in the list does not necessarily indicate endorsement, recommendation or approval by the ESONE Committee, nor does omission indicate disapproval.

The classification used tentatively and reproduced below, is the same as was proposed in the March 1974 issue (No. 9) of this Bulletin.

SOFTWARE CLASSIFICATION GROUPS

.50 Fundamental Concepts, General Subjects

READER SERVICE REF NO 14,5001
CLASS CODE = ,50
TITLE= = = = IMPLEMENTING CAMAC BY COMPILERS
AUTHOR(S)= = W, KNEIS, GFK, ZYKLOTRON-LB,, KARLSRUHE, GERMANY
PUBL, REF, = PROC CAMAC SYMPOS, LUXMBG, DEC 1973

DESCRIPTION= =
DEMANDS ON REAL-TIME SYSTEMS SUCH AS MINIMUM EXECUTION TIME MINIMUM CORE REQUIREMENTS, ETC,, RECOMMEND THE USE OF COMPILERS IN PROGRAMMING, THE POSSIBILITY TO IMPLEMENT A CAMAC LANGUAGE BY A COMPILER IS FIRST OF ALL A FUNCTION OF THE LEVEL AND CONCEPT OF THE LANGUAGE, META-LANGUAGES, THE SYNTAX OF A PROGRAMMING LANGUAGE, ARE USED TO FORMULATE A COMPILER FOR A SPECIFIC LANGUAGE, THE METHOD DESCRIBED HAS BEEN USED TO WRITE A COMPILER FOR IML, THE INTERMEDIATE LEVEL CAMAC LANGUAGE, IMPLEMENTED IN AN ASSEMBLER ENVIRONMENT,

READER SERVICE REF NO 14,5002
CLASS CODE = ,50
TITLE= = = = PROCEDURE CALLS = A PRAGMATIC APPROACH
AUTHOR(S)= = J, MICHELSON, H, HALLING, KFA, JUELICH,
PUBL, REF, = PROC CAMAC SYMPOS, LUXMBG, DEC 1973
ESONE REGSTR DATE 31 MAY 1974

DESCRIPTION= =
DISCUSSION OF PROCEDURE CALLS AS THE BASIS FOR CAMAC SOFTWARE WITHIN HIGH-LEVEL LANGUAGES, COMPARISON WITH SYNTAX MODIFICATIONS TO LANGUAGES, DISCUSSION OF IMPLEMENTATION RESTRICTIONS DUE TO LANGUAGE REQUIREMENTS FOR EXISTING HIGH-LEVEL LANGUAGES, E,G, CLOSED SYSTEM-SUBROUTINES WHICH EXECUTE ONE DEFINED OPERATION (INVOLVING ONE OR MORE CAMAC CYCLES AS A GROUP), COMPARISON OF US-NIM CAMAC FORTRAN SUBROUTINES AND PROCEDURE-CALL SYNTAX OF ESONE SWG IML LANGUAGE, APPLICATION OF PROCEDURE-CALLS TO APPLICATION-ORIENTED SOFTWARE,

READER SERVICE REF NO 14,5003
CLASS CODE = ,501(PL-11)
TITLE= = = = CAMAC FACILITIES IN THE PROGRAMMING LANGUAGE OF PL-11
AUTHOR(S)= = ROBERT D RUSSELL, CERN, GENEVA
PUBL, REF, = PROC CAMAC SYMPOS, LUXMBG, DEC 1973
YELLOW REPORT, CERN 74-24, DEC 1974
NAME/ACRONYM = EXTENDED PL-11
OPERATIVE DATE= 1971/72
COMPUTER = PDP-11, WORD LENGTH 16 BITS
INTERFACE(S) = CA-11 (EG&G/ORTEC)
SOFTWARE TYPE = LANGUAGE, PL-11(EXTENDED)
INCORP TECHNIQUE IN-LINE CODING OF CAMAC STATEMENTS
FACILITIES = SYMBOLIC DEVICE NAME USED
DEMAND HANDLING IS INCLUDED

DESCRIPTION= =
PL-11 IS AN INTERMEDIATE-LEVEL, MACHINE-ORIENTED PROGRAMMING LANGUAGE EXTENDED TO INCLUDE CAMAC FEATURES, SYNTACTIC FORM OF CAMAC STATEMENTS ARE ANALOGOUS TO STANDARD PL-11 STATEMENTS, SYMBOLIC NAMES FOR VARIABLES AND FUNCTIONS ARE DECLARED AT ONCE, AND OPERATIONS ARE EXECUTED BY STATEMENTS REFERRING TO THESE NAMES, USE OF SYMBOLIC NAMES MAKES PROGRAMS READABLE, AND SIMPLIFIES MODIFICATIONS OF CAMAC CONFIGURATIONS,
EXAMPLE OF STANDARD STATEMENT= =
WHILE PRINTSTATUS = BUSY DO
EXAMPLE OF CAMAC STATEMENT= =
WHILE CRTSTATUS = BUSY DO

READER SERVICE REF NO 14,5004
CLASS CODE = ,501 (CATY)
AUTHOR(S)= = F R GOLDING, DARESBURY LABORATORIES
NAME/ACRONYM = CATY
COMPUTER = ANY
SOFTWARE TYPE = LANGUAGE (BASED ON BASIC)

DESCRIPTION= =
CATY IS A MACHINE INDEPENDENT HIGH-LEVEL LANGUAGE BASED UPON A SUBSET OF BASIC WITH EXTENSIONS FOR ADDRESSING CAMAC, PROGRAMS WRITTEN IN CATY ARE COMPILED AND NOT INTERPRETED, THUS, THE SPEED OF OPERATION WHEN CAMAC IS TESTED UNDER CATY IS COMPARABLE WITH THE SPEED OF OPERATION IN APPLICATIONS, CATY HAS BEEN IMPLEMENTED ON SEVERAL COMPUTERS (SEE ,543),

READER SERVICE REF NO 14,5005
CLASS CODE = ,501 (CATY)
TITLE= = = = SPECIFICATION OF THE LANGUAGE CATY C1030
AUTHOR(S)= = R F CRANFIELD, GEC ELLIOTT (SEE ALSO PREVIOUS ENTRY)
NAME/ACRONYM = CATY
OBTAINABLE FROM= GEC ELLIOTT (SEE LIST OF MANUFACTURERS)
AVAILABLE ON/AS= DESCRIPTION
SOFTWARE TYPE= LANGUAGE (BASED ON BASIC)

DESCRIPTION= =
THE MAIN SPECIFICATION DESCRIBES THE FACILITIES AVAILABLE IN THE MACHINE INDEPENDENT HIGH LEVEL LANGUAGE CATY, APPENDICES TO THE SPECIFICATION DESCRIBE THE ADDITIONAL FEATURES ASSOCIATED WITH IMPLEMENTATIONS, ALL USING GEC ELLIOTT SYSTEM CRATE INTERFACES ON THE PDP-11, NOVA, GEC-4080, AND GEC-2050 COMPUTERS,

READER SERVICE REF NO 14,5006
CLASS CODE = ,501 (IML)
TITLE= = = = THE DEFINITION OF IML
A LANGUAGE FOR USE IN CAMAC SYSTEMS
PREPARED BY = ESONE COMMITTEE, SOFTWARE W,G, AND AEC NIM COMMITTEE, SOFTWARE W,G,
PUBL, REF, = REPORT ESONE/IML/01, OCT 1974, AND REPORT TID-26615, JAN 1975
NAME/ACRONYM = IML
MAINTENANCE BY= ESONE COMMITTEE IN COLLABORATION WITH NIM COMMITTEE
OBTAINABLE FROM ESONE SECRETARIAT AND U,S, GOVERNMENT PRINTING OFFICE RESPECTIVELY
ESONE REGSTR DATE AUG/SEPT 1974
COMPUTER = ANY
SOFTWARE TYPE = LANGUAGE

DESCRIPTION= =
IML IS A LANGUAGE USED TO EXPRESS THE OPERATIONS DESCRIBED IN THE CAMAC HARDWARE SPECIFICATIONS, AND THEIR INTERACTION WITH A COMPUTER SYSTEM, IML STATEMENTS LINK CAMAC STRUCTURES AND MODES OF OPERATION TO DATA STRUCTURES AND REAL-TIME FEATURES IN THE COMPUTER SYSTEM,
THIS DEFINITION IS A GUIDE FOR THOSE IMPLEMENTING LANGUAGES AND OPERATING SYSTEMS WHO WISH TO MAKE CAMAC INPUT/OUTPUT AVAILABLE TO USERS, FEATURES ARE INCLUDED WHICH SUPPORT THE CAMAC BRANCH HIGHWAY AND THE CAMAC SERIAL HIGHWAY,
THE LANGUAGE IS DEFINED SEMANTICALLY - THE SYNTAX USED TO EXPRESS IML DEPENDS ON THE ENVIRONMENT, THE MACRO SYNTAX IML-M1 IS DEFINED IN AN APPENDIX,

READER SERVICE REF NO 14,5007
CLASS CODE = ,501 (CASIC)
TITLE= = = = A CAMAC EXTENDED BASIC LANGUAGE
AUTHOR(S)= = J M SERVENT (SCHLUMBERGER)
NAME/ACRONYM = CASIC
OBTAINABLE FROM= SCHLUMBERGER (SEE LIST OF MANUFACTURERS)
AVAILABLE ON/AS= DESCRIPTION
SOFTWARE TYPE= LANGUAGE (EXTENDED BASIC)

DESCRIPTION= =
CASIC IS BASED ON BASIC AND PROVIDES ALL STANDARD STATEMENTS OF BASIC PLUS A SET OF CAMAC RELATED STATEMENTS,
CASIC = LIKE BASIC = IS CONVERSATIONAL, THE MOST RECENT VERSION CONFORMS TO THE IML LANGUAGE (SEE ,501(IML)) DEFINED BY THE ESONE COMMITTEE,
CASIC IS IMPLEMENTED ON PDP-11 (SEE ,544),

.51 User-Oriented Programs I (full system support)

READER SERVICE	REF NO 14,5008
CLASS CODE =	,51
TITLE= = = =	CAMAC OPERATING SYSTEM FOR CONTROL APPLICATIONS
AUTHOR(S)= =	DR B, MERTENS, IKP, KFA, JUELICH
PUBL, REF, =	CAMAC BULLETIN NO 9, MARCH 1974
NAME/ACRONYM =	COS
AVAILABLE ON/AS	PAPER TAPE, ASCII CODE
OPERATIVE DATE=	1972
COMPUTER =	PDP=15, CORE REQUIREMENTS= 16K
INTERFACE(S) =	TYPE 2200 (BOREK)
SOFTWARE TYPE =	SYSTEM PROGRAM
LANGUAGE =	FORTRAN & MACRO=ASSEMBLER
CAMAC FACILITIES	SYMBOLIC DEVICE NAMES USED, SINGLE & MULTIPLE ACTION PER INSTRUCTION, REAL/TIME DEMEND HANDLING INCORPORATED

DESCRIPTION= =
THE SYSTEM SUFTWARE PACKAGE PERMITS READ AND WRITE OF UP TO 100 MODULES, REAL=TIME TASKS MAY BE DEFINED ON=LINE, ABOUT 60 ELEMENTARY COMMANDS ARE PRE=DEFINED, SUCH AS==
=NAME MODULE/C=1, N=2, A=3/DEFINE SYMBOLIC NAME
=READ MODULE/F=0
=WRITE MODULE 321/F=16
=DISAB MODULE/F=24
=DEFINE TASK/OPEN A TASK=DEFINITION
=END/CLOSE TASK=FILE
=AFTER 15 SECS TASK/EXECUTE USER=DEFINED TASK
=15 SECS FROM NOW
=SULL MODULE 3456/VALUE TO BE WRITTEN NEXT TO MODULE

READER SERVICE	REF NO 14,5009
CLASS CODE =	,51
TITLE= = = =	BACKGROUND=FOREGROUND SYSTEM FOR PULSE=HEIGHT ANALYSIS OF TWO= DIMENSIONAL MULTIWIRE PROPORTIONAL CHAMBER DATA
AUTHOR(S)= =	DR A HEUSLER, IPK, KFA, JUELICH
NAME/ACRONYM =	BFG
AVAILABLE ON/AS	PAPER TAPE, ASCII CODE
OPERATIVE DATE=	1974?
COMPUTER =	PDP=15, CORE REQUIREMENTS = 24K
INTERFACE(S) =	TYPE 2200 (BOREK)
MIN SYSTEM CONFIG	MAGTAPE, DECTAPE, DISK, & MEMORY SCANNING DISPLAY (IN=HOUSE)
SOFTWARE TYPE =	SYSTEM PROGRAM
LANGUAGE =	FORTRAN & MACRO=ASSEMBLER

DESCRIPTION= =
THE SYSTEM SUFTWARE PERMITS START AND STOP OF BLOCK TRANSFER FROM THE A/D CONVERTERS TO THE PDP=15 MEMORY (LIST MODE OUTPUT ONTO MAGTAPE ON=LINE SORTING IF DESIRED).
THE BOREK INTERFACE HAS BEEN MODIFIED TO ALLOW BLOCK LENGTHS UP TO 4K 18 BIT WORDS.

READER SERVICE	REF NO 14,5010
CLASS CODE =	,51
TITLE= = = =	TRIUMF CONTROL SYSTEM SOFTWARE
AUTHOR(S)= =	D, P, GURD, W, K, DAWSON, TRIUMF, UNIVERSITY OF ALBERTA, CANADA
PUBL, REF, =	CAMAC BULLETIN NO 5, NOVEMBER 1972
OPERATIVE DATE=	1973
COMPUTER =	4 SUPERNOVAS
INTERFACE(S) =	IN=HOUSE TYPE
SOFTWARE TYPE =	FULL SYSTEM SUPPORT FOR CONTROL OF TRIUMF CYCLOTRON

DESCRIPTION= =
THE SYSTEM SUFTWARE PACKAGE MONITORS OVER 1000 ANALOGUE PARAMETERS AND 1000 DIGITAL STATUS POINTS, SEARCHES OUT=OF= LIMIT READINGS, DISPLAYS MEASUREMENTS ON REQUEST, SETS OVER 300 ANALOGUE POINTS FROM A CENTRAL CONSOLE AND PERFORMS A NUMBER OF OTHER ROUTINES.
A REAL=TIME EXECUTIVE PROGRAM = NATS (FOR NOVA ASYNCHRONOUS TASKING SUPERVISOR) = SCHEDULES AND SUPERVISES CAMAC TASKS, SUPPORTED BY A SUBPROGRAM LIBRARY, AS THEY ARE REQUESTED, JOBS TO BE PERFORMED ARE STRUCTURED INTO SEQUENCES OF CAMAC OPERATIONS SPECIFIC TO A PIECE OF HARDWARE (= CAMAC MODULE), THERE IS THUS A DIRECT MODULAR HARDWARE=SOFTWARE CORRESPOND= ENCE. CONTROL IS BASICALLY CLOCK=INITIATED SOFTWARE SCAN OF CYCLOTRON MONITORING, BUT INTERRUPTS ARE INCLUDED, MAINLY INITIATED BY CONSOLE.

READER SERVICE	REF NO 14,5011
CLASS CODE =	,51
TITLE= = = =	BASIC SINGLE PARAMETER MCA SYSTEM (MISP)
NAME/ACRONYM =	MISP
OBTAINABLE FROM=	NUCLEAR ENTERPRISES (SEE INDEX OF MFRS)
SOFTWARE TYPE=	SYSTEM SOFTWARE
COMPUTER = =	PDP=11, 8K MEMORY & REAL TIME CLOCK
INTERFACE(S) =	9030 (NUCL, ENTERPR) (PROGRAMMED TRANSFERS & INTERRUPT ONLY)
HARDWARE CONFIG	ADC (LABEN OR 9060),9021 LIVE TIME RTC, TTY/READER (7064),TEK603/604 OR LANSCOPE

DESCRIPTION= =
THE PROGRAM OCCUPIES 2K OF MEMORY AND USES A DATA AREA OF 4K FOR UP TO 4096 CHANNELS ACQUISITION.
THE PACKAGE CONSISTS OF A DISPLAY DRIVER, A USER ORIENTED TELETYPE HANDLER, ACQUISITION CONTROL, AND A DATA MANIPULA= TION ROUTINE.
THE DISPLAY DRIVER IS RUN AS A BACKGROUND TASK WHICH IS INTERRUPTED BY THE ADC, CLOCKS AND TELETYPE.
THIS PACKAGE CAN BE OBTAINED WITH MULTISCALER OPTION, THE HARDWARE IS EXTENDED WITH A 9003 OR 003 SCALER, DATA AREA IS DIVIDED INTO 4 AREAS, EACH ONE THOUSAND CHANNELS.

READER SERVICE	REF NO 14,5012
CLASS CODE =	,51
TITLE= = = =	DUAL MCA SYSTEM (DAMCAS)
NAME/ACRONYM =	DAMCAS
OBTAINABLE FROM=	NUCLEAR ENTERPRISES (SEE INDEX OF MFRS)
SOFTWARE TYPE=	SYSTEM SOFTWARE
COMPUTER = =	PDP=11, 16K MEMORY & REAL TIME CLOCK
INTERFACE(S) =	9030 & 9033 (NUCL ENTERPR) (PROGRAMMED & AUTONOMOUS TRANSFERS)
HARDWARE CONFIG	ADC (LABEN OR 9060),9021 LIVE TIME RTC, TTY/READER (7064), PUNCH (7065), MAGTAPE (CS 0042),TEK603/604 OR LANSCOPE

DESCRIPTION= =
THE PROGRAM OCCUPIES 6K LEAVING 10K OF MEMORY FOR DATA ACQUI= SITION (4K OF 16 BITS & 4K OF 24 BITS).
THE SOFTWARE PACKAGE CONSISTS OF A DISPLAY DRIVER, A TELETYPE HANDLER FOR OPERATOR CONTROL OF DATA ACQUISITION, DATA MANI= PULATION ROUTINE, AND A ROUTINE FOR AUTONOMOUS CONTROL OF DATA ACQUISITION AND MAG TAPE TRANSFERS.

READER SERVICE	REF NO 14,5013
CLASS CODE =	,51
TITLE= = = =	MULTI PARAMETER DATA ACQUISITION SYSTEM
NAME/ACRONYM =	MUDAS 1
OBTAINABLE FROM=	NUCLEAR ENTERPRISES (SEE INDEX OF MFRS)
SOFTWARE TYPE=	SYSTEM SOFTWARE
COMPUTER = =	PDP=11, 8K MEMORY & REAL TIME CLOCK
INTERFACE(S) =	9030 (NUCL, ENTERPR) (PROGRAMMED TRANSFERS & INTERRUPT ONLY)
HARDWARE CONFIG	ADC'S (LABEN OR 9060) & CUINC SELECTOR (CS 0049), 9021 LIVE TIMER RTC, TTY & MAG TAPE, TEK 603/604.

DESCRIPTION= =
THE SYSTEM IS CAPABLE OF ACCEPTING FIVE PARAMETER EVENTS AND STORING THEM ON MAG TAPE, SIMULTANEOUSLY PERFORMING MULTI= CHANNEL ANALYSIS ON ONE SELECTED PARAMETER.
WINDOWS MAY BE SET ON EACH PARAMETER FOR BOTH MODES, TOGETHER WITH A COUNT DIVISION FACTOR SET OVER THE REGION OF INTEREST. DATA DUMPED IN LIST MODE MAY BE READ BACK FOR ANALYSIS.

READER SERVICE REF NO 14,5014
CLASS CODE = ,51
AUTHOR(S)= = D GURD, TRIUMF,UNIV, ALBERTA,CANADA
NAME/ACRONYM = CAMAC
OPERATIVE DATE= 1973
SOFTWARE TYPE = SYSTEM SOFTWARE

DESCRIPTION= =
THE SYSTEM SOFTWARE= CAMAC = CONSISTS OF SEVERAL SUBROUTINE CALLS, THESE ARE= =
PRIMITIVE SUBROUTINES PERFORMING THE ACTUAL I/O OPERATIONS,
MODULE SUBROUTINES, THE MUX/ADC SUBROUTINES, CAMAC LAMS OR INTERRUPTS, SERIAL TASKS, AND AN INTERPRETER (FOR DATA),

.52 User-Oriented Programs II (specific run-time programs)

READER SERVICE REF NO 14,5015
CLASS CODE = ,52
TITLE= = = = OPERATING SYSTEM SOFTWARE PACKAGES
NAME/ACRONYM = SEE DESCRIPTION
MAINTENANCE BY= DEC
OBTAINABLE FROM DEC (SEE INDEX OF MANUFACTURERS)
OPERATIVE DATE= 1975
COMPUTER = PDP=11
INTERFACE(S) = SEE DESCRIPTION
SOFTWARE TYPE = CAMAC SERVICE ROUTINES, USER=, INTERFACE= & DESCRIPTOR PROGRAMS

DESCRIPTION= =
THE SOFTWARE PACKAGES ARE COMPLETE OPERATING SYSTEMS, CONTROLLERS AND OPERATING SYSTEMS ARE RELATED AS FOLLOWS=-
CA=11=C USES RSX=11=D OPERATING SYSTEM
CA=11=E USES RSX=11=M OR RT=11
CA=11=F USES RSX=11=M OR RT=11

READER SERVICE REF NO 14,5016
CLASS CODE = ,52
TITLE= = = = CASPAC = A SOFTWARE PACKAGE FOR COMMUNI= CATION WITH CAMAC=PROCESS=PERIPHERALS
NAME/ACRONYM = CASPAC
OBTAINABLE FROM= IDAS (SEE INDEX OF MANUFACTURERS)
SOFTWARE TYPE= SYSTEM OF RE=ENTRANT ASSEMBLER ROUTINES
COMPUTER = = PDP=11 (DEC), MIN 740 WORDS OF MEMORY
INTERFACE(S) = I CP=11 (SCHLUMBERGER)

DESCRIPTION= =
THE SYSTEM OF ASSEMBLER ROUTINES ALLOW COMMUNICATION WITH CAMAC=PROCESS=PERIPHERALS USING SINGLE=WORD TRANSFER MODE AS WELL AS BLOCK TRANSFER MODE ON FORTRAN AND ASSEMBLER LEVEL, INTERRUPT ACTIONS CAN BE OBTAINED IN THE FORM OF AN ARBITRARY SEQUENCE OF CAMAC TRANSFERS ON FORTRAN LEVEL,
NO SOFTWARE OPERATING SYSTEM IS NEEDED, AND CASPAC CAN THEREFORE BE USED AUTONOMOUSLY AS WELL AS IN CONNECTION WITH A REAL TIME OR BATCH OPERATING SYSTEM,

.53 User-Oriented Programs III (subprograms, etc.)

READER SERVICE REF NO 14,5017
CLASS CODE = ,53 (BASIC)
TITLE= = = = CAMAC AND INTERACTING PROGRAMMING
AUTHOR(S)= = DR E M RIMMER, CERN, GENEVA
PUBL, REF, = PROC CAMAC SYMPOS, LUXMBG, DEC 1973 & BASIC CALLABLE ROUTINES, NP GROUP NOTE, NP=DMG, CERN
NAME/ACRONYM = HPCMA, HPCMB, HPCMC
MAINTENANCE BY= DR E M RIMMER
OBTAINABLE FROM NP DIV, CERN, CH=1211 GENEVA
AVAILABLE ON/AS PAPER TAPE, ASCII CODE
OPERATIVE DATE= 1971/72
COMPUTER = H=P 2100=SERIES, 8K 16 BIT WORDS
INTERFACE(S) = 2201(BORER), 7218 & HPCC=066(CERN)
MIN SYSTEM CONFIG TTY OR TEK 4010 TERMINAL & CC=A1
SOFTWARE TYPE = SET OF SUBROUTINES
LANGUAGE = HP ASSEMBLY
HOST LANGUAGE = BASIC (NP EXTENSION OF)
CAMAC FACILITIES IN=LINE CODED CALLS IN BASIC, SUBROUTINES IN ASSEMBLY, ABS ADDR
FACILITIES = SINGLE & MULTIPLE ACTION PER INSTRUCTION, NO DEMAND HANDLING

DESCRIPTION= =
THESE BASIC=CALLABLE CAMAC SUBROUTINES IN THREE VERSIONS FOR THREE INTERFACES PROVIDE MOST COMMAND FACILITIES FOR CONTROL AND DATA TRANSFER, DATA WORDS MAY BE 16 OR 24 BITS LONG (ONLY 16 BITS FOR HPCC=066), BINARY, BCD OR LOGIC (0 OR 1), ROUTINES COVER BLOCK TRANSFERS, PROGRAMMED AND SEQUENTIAL ADDRESSING & UTILITY ROUTINES, IN TOTAL 18 & 3 OPTIONALLY,
GENERAL FORM OF CALL STATEMENT=-
= = =CALL (SUBROUTINE NUMBER,C,N,A,F,D,Q)
= = =CALL (SUBROUTINE NUMBER,C,N,A,F,D(I),Q,W)
WHERE W IS WORD COUNT, D IS DATA, C,N,A,F, & Q HAVE USUAL MEANING
EX=- CALL(10,1,2,0,16,D(I),Q,20)
TIME IS APPR 5 MSECS/STATEMENT, BLOCK TRANSFER CALL GENE= RATED DIRECTLY BY INTERFACE ARE MUCH FASTER,

READER SERVICE REF NO 14,5018
CLASS CODE = ,53(FORTRAN)
TITLE= = = = SPECIFICATIONS FOR STANDARD CAMAC SUBROUTINES
AUTHOR(S)= = RICHARD F THOMAS JR,
PUBL, REF, = CAMAC BULLETIN NO 6, MARCH 1973
NAME/ACRONYM = SEE DESCRIPTION
OBTAINABLE FROM USAEC NIM COMMITTEE, CAMAC SWG
AVAILABLE ON/AS ALGORITHM
OPERATIVE DATE= 1973
COMPUTER = INDEPENDENT, MEMORY SIZE NOT SPEC,
INTERFACE(S) = ANY
SOFTWARE TYPE = SET OF SUBROUTINES
LANGUAGE = FORTRAN
CAMAC FACILITIES FUNDAMENTAL CAMAC OPERATIONS, STANDARD BLOCK TRANSFERS IN SINGLE & MULTIPLE ACTION STATEMENTS

DESCRIPTION= =
A SET OF 6 SUBROUTINES, OF WHICH ONE IS CALLED BY ALL THE OTHER PERMITS A GREAT VARIETY OF SINGLE AND MULTIPLE CAMAC OPERATIONS TO BE PERFORMED, DEMAND HANDLING, OTHER THAN BY TEST LAM, IS NOT COVERED,
THE SUBROUTINES EXECUTE CAMAC OPERATIONS AS FOLLOWS=-
CMCBSC = SINGLE CAMAC FUNCTION AT SINGLE ADDRESS ONE OR MORE TIMES
CMCSEQ = SINGLE CAMAC FUNCTION AT SUCCESSION OF ADDRESSES
CMCASC = SPECIFIED CAMAC FUNCTION IN ADDRESS SCAN MODE
CMCRPT = SPECIFIED CAMAC FUNCTION IN REPEAT MODE
CMCSTP = SPECIFIED CAMAC FUNCTION IN STOP MODE
CMCLUP = SPECIFIED CAMAC FUNCTION AT A HIERARCHICAL SEQUENCE OF ADDRESSES WITH OPTIONAL SKIP OF SEQUENCE BASED ON Q,
GENERAL FORM OF STATEMENT=-
CALL CMC,,, (PARAMETER LIST)
EXAMPLE=- CALL CMCSTP (F,B,C,N,AD,LN,DATA,ERROR,NEX)

READER SERVICE REF NO 14,5019
CLASS CODE = ,53(FORTRAN)
TITLE= = = = FORTRAN SUBROUTINES
AUTHOR(S)= = H POHL
NAME/ACRONYM = FORTRAN CALLS
VERSION= = = V002
OBTAINABLE FROM H POHL, ZEL, KFA, JUELICH
AVAILABLE ON/AS DECTAPE
OPERATIVE DATE= MARCH 1972
COMPUTER = PDP=11, 16K 16 BIT WORDS MEMORY
INTERFACE(S) = TYPE 1533A (BORER)
SOFTWARE TYPE = PROCEDURE CALLS
LANGUAGE = FORTRAN ON PDP=11 (THREADED CODE)
INCORP TECHNIQUE IN=LINE SUBROUTINE CALLS
CAMAC FACILITIES SINGLE ACTION STATEMENTS

DESCRIPTION= =
FORTRAN SUBROUTINES FOR SINGLE ACTIONS, MUCH SIMPLER THAN THE NIM APPROACH (REF, H, F, THOMAS) FOR THE BORER 1533A CONTROLLER WRITTEN IN RE=ENTRANT CODE,

READER SERVICE
CLASS CODE =
TITLE= = = =
AUTHOR(S)= =
NAME/ACRONYM =
VERSION= = =
MAINTENANCE BY=
OBTAINABLE FROM
AVAILABLE ON/AS
OPERATIVE DATE=
COMPUTER =
INTERFACE(S) =
SOFTWARE TYPE =
LANGUAGE =
HOST LANGUAGE =
INCORP TECHNIQUE
CAMAC FACILITIES

REF NO 14,5020
,53
CAMAC FUNCTION FOR RT11
L BYARS, R KEYSER
CAMAC, CAMINT
RT11
ORTEC
ORTEC (SEE INDEX OF MANUFACTURERS)
PAPER TAPE
1974
PDP=11
DC011 (EG&G/ORTEC)
SUBROUTINES
PDP=11 ASSEMBLY
RT11/FORTRAN
CALLS TO FORTRAN LIBRARY ROUTINES
SINGLE OR MULTIPLE INSTRUCTIONS,
DEMAND HANDLING

DESCRIPTION= =
THIS SOFTWARE PACKAGE CONSISTS OF A NUMBER OF SUBROUTINES
FOR FORTRAN/RT11 CALLING CAMAC FUNCTIONS,
THE CAMAC CALL STATEMENT HAS THE FOLLOWING FORM==
CALL CAMAC (IF, IN, IA, IQ, IDATA)
THEY ARE USED TO TRANSFER DATA TO/FROM CAMAC AND FOR TEST
PURPOSES,
IF, IN, IA ARE RESPECTIVELY FUNCTION, STATION ADDRESS AND
SUBADDRESS, IQ IS BOTH QBIT AND XBIT,
CAMINT IS USED TO HANDLE INTERRUPTS FROM CAMAC CRATE, AND
HAS THE GENERAL FORM==
CAMINT(IN,NAME1)
WHERE IN IS THE STATION NUMBER AND NAME1 IS THE NAME OF THE
SUBROUTINE TO BE EXECUTED WHEN THE INTERRUPT OCCURS,

READER SERVICE
CLASS CODE =
AUTHOR(S)= =
NAME/ACRONYM =
OBTAINABLE FROM
OPERATIVE DATE=
COMPUTER =
INTERFACE(S) =
LANGUAGE =
SOFTWARE TYPE =

REF NO 14,5021
,53(FORTRAN)
J M STEPHENSON, L A KLAISNER
KSCLIB
KINETIC SYSTEMS (SEE INDEX OF MFRS)
1974
PDP=11, 16K CORE MEMORY REQUIRED
TYPES 3911A, 3991 & 3992 (KINETIC)
FORTRAN
LIBRARY OF FORTRAN FUNCTIONS AND
SUBROUTINES

DESCRIPTION= =
THIS SOFTWARE PACKAGE IMPLEMENTS THE CMCBSC SERIES OF STAND=
ARD FORTRAN CALLS DESCRIBED IN CAMAC BULLETIN NO 6, 1973,
IT ALSO INCLUDES THE BIT MANIPULATION FUNCTIONS EXCLUSIVE
OR, INCLUSIVE OR, AND, NOT, & SHIFT, THE PACKAGE SUPPORTS
UP TO 8 CRATES INTERFACED THROUGH MODEL 3911A UNIBUS *)
CRATE CONTROLLERS, UP TO 7 CRATES PER 3991 BRANCH DRIVER AND
UP TO 61 CRATES PER 3992 SERIAL BRANCH DRIVER, THE NUMBER
OF PARALLEL AND SERIAL BRANCHES SHOULD BE LESS THAN 8,

*) UNIBUS IS A TRADE MARK OF DIGITAL EQUIPMENT CORP,

READER SERVICE
CLASS CODE =
TITLE= = = =
AUTHOR(S)= =

NAME/ACRONYM =
OBTAINABLE FROM
AVAILABLE ON/AS
OPERATIVE DATE=
COMPUTER =
INTERFACE(S) =
MIN MEMORY SPACE

MIN SYSTEM CONFIG
SOFTWARE TYPE =
ENVIRONMENT FOR =
LANGUAGE =
FACILITIES =

REF NO 14,5022
,53
I/O MACROS FOR CAMAC
D STUCKENBROCK, G KLENERT,
SIEMENS AG, KARLSRUHE
MACAM
SIEMENS (SEE INDEX OF MFRS)
PAPER TAPE, CARDS & SOURCE DECK
NOVEMBER 1974
PR 320/330
CC 320 & SC 330 (SIEMENS)
,5K = 1K OF 16 BITS (SUPERVISOR EXCL)
DEPENDING ON HARDWARE
TTY AND SUPERVISOR PROGRAM
I/O ROUTINES, LAM HANDLING
CAMAC SOFTWARE IS ASSEMBLER 300
MACROS = ASSEMBLER,CALLS = FORTRAN
CONCURRENT MULTI=USER OPERATION, SYSTEM
RUNS UNDER REAL=TIME SUPERVISOR

DESCRIPTION= =
A SET OF I/O MACRO SUBROUTINES CAN BE CALLED BY ANY USER
PROGRAM CONCURRENTLY RUNNING ON THE COMPUTER, PROVIDED THEY
OPERATE UNDER A REAL=TIME SUPERVISOR PROGRAM, THE ROUTINES
COMPRISE THE FUNCTIONS READ, WRITE, AND EXECUTION OF CONTROL
COMMANDS, BLOCK TRANSFERS ARE PERFORMED ON CONSTANT OR
VARIABLE CAMAC ADDRESS, AND IN INCREMENT MODE OR RANDOM=LIST
MODE, THE COORDINATION OF USER PROGRAMS AND CAMAC PROVIDED
BY THE SUPERVISOR, FACILITATES GREATLY THE LAM HANDLING,
THE SYSTEM ALLOWS UP TO 8 BRANCHES, EACH WITH 7 CRATES,
SYSTEM SOFTWARE ENVIRONMENTS FACILITATE INCORPORATION OF
THE SUBROUTINE CALLS AS STATEMENTS EMBEDDED IN FORTRAN
PROGRAMS,

READER SERVICE
CLASS CODE =
TITLE= = = =
AUTHOR(S)= =
NAME/ACRONYM =
OBTAINABLE FROM=
AVAILABLE ON/AS=
OPERATIVE DATE =
COMPUTER = =
MIN MEMORY SPACE
INTERFACE(S) =
SOFTWARE TYPE=
MIN SYSTEM CONFIG
INCORP TECHNIQUE
CAMAC FACILITIES

REF NO 14,5023
,53 (BASIC)
BASIC = SUBROUTINES
D STUCKENBROCK, SIEMENS AG, KARLSRUHE
BASIC = CALLS
SIEMENS (SEE INDEX OF MANUFACTURERS)
PAPER TAPE, CARDS
1973
PR 320
1K OF 16 BITS (BASIC COMPILER EXCLUDED)
CC 320
SUBROUTINES
TTY AND BASIC COMPILER
EMBEDDED BASIC CALLS TO SUBROUTINES
LAM HANDLING

DESCRIPTION= =
THE SUBROUTINES IN ASSEMBLER ARE HANDLED BY THE BASIC=ON=320
COMPILER (INTERPRETER?),
THE STATEMENT = =
CALL (CM, PARAMETER LIST)
CAUSES PROGRAM TO JUMP TO SUBROUTINE CALLED,
THE FOLLOWING CAMAC OPERATIONS CAN BE EXECUTED = =
= SINGLE OPERATION (READ, WRITE, CONTROL)
= INTERRUPT REGISTRATION AND JUMP TO LAM HANDLING ROUTINE
= WAITING FOR LAM
'PARAMETER LIST' IS A STRING OF CHARACTERS SPECIFYING THE
OPERATION TO BE EXECUTED,
EXAMPLE = =
CALL(CM,NAF,11,0,0,X1)
= WHERE 11,0,0, = STATION,SUBADDRESS,FUNCTION, X1 = VARIABLE

READER SERVICE
CLASS CODE =
TITLE= = = =
AUTHOR(S)= =
PUBL, REF, =

MAINTENANCE BY
OBTAINABLE FROM=
AVAILABLE ON/AS=
OPERATIVE DATE =
COMPUTER = =
INTERFACE(S) =
OPERATING SYSTEM
SOFTWARE TYPE=

LANGUAGE = =
HOST LANGUAGE=
INCORP TECHNIQUE
CAMAC FACILITIES

REF NO 14,5024
,53
TWO=LEVEL CAMAC PERIPHERAL HANDLER
L M TAFF, UNIV OF GRONINGEN, NETHERLANDS
COMPUTER PHYSICS COMMUNICATIONS
(TO BE PUBLISHED)
AUTHOR
AUTHOR
DECTAPE (ASCII CODE)
1974
DEC PDP=11, MIN 8K OF MEMORY
CA=15 (DEC)
(SOFTWARE) = DEC MONITOR SYSTEM (ADSS)
CAMAC DRIVER/LAM HANDLER SUBROUTINE,
I/O DEVICE HANDLERS, CMCBSC SUBROUTINE
ASSEMBLER
ANY SUPPORTED BY SYSTEM
LINKED AT LOAD TIME
SINGLE CAMAC OPERATIONS, DATA CHANNEL
TRANSFERS, DEMAND HANDLING, RE=ENTRANT

DESCRIPTION= =
THE CAMAC DRIVER/LAM HANDLER IS A GLOBALLY LINKED SUBROUTINE
FOR EXECUTING SINGLE CAMAC OPERATIONS, CONTROLLING ACCESS TO 2
HARDWARE DATA CHANNELS VIA QUEUES, AND GIVING CONTROL TO THE
PROPER USER ROUTINE WHEN A LAM OCCURS, IT MAY BE CALLED BY
ASSEMBLER CODED USER PROGRAMS, THOMAS' STANDARD SUBROUTINE
CMCBSC (HENCE ALL OTHER OF HIS ROUTINES WHICH CALL CMCBSC)
=SEE ,53 ABOVE = AND I/O HANDLERS FOR CAMAC INTERFACED
PERIPHERALS, EITHER FROM MAINSTREAM OR LAM HARDWARE PRIORITY,
CAMAC INTERFACED DEVICES FOR WHICH HANDLERS CURRENTLY EXIST
INCLUDE A LINE PRINTER, CARD READER, INCREMENTAL PLOTTER, AND
A TEKTRONIX 4010 TERMINAL, FOR DEVICE HANDLERS, CAMAC IS
TRANSPARENT,
IT IS RELATIVELY EASY TO ADAPT A HANDLER FOR AN I/O BUS DEVICE
TO CAMAC SIMPLY BY SUBSTITUTING SUBROUTINE CALLS TO THE DRIVER
FOR I/O OPERATIONS AND OBSERVING A FEW NON=RESTRICTIVE CONVEN=
TIONS, THIS TWO=LEVEL APPROACH CAN ACCUMULATE CAMAC LANGUAGES
IF ACTION STATEMENTS ARE COMPILED INTO SUBROUTINE CALLS,

READER SERVICE
CLASS CODE =
TITLE= = = =
AUTHOR(S)= =
MAINTENANCE BY
AVAILABLE ON/AS=
OPERATIVE DATE =
COMPUTER = =
INTERFACE(S) =
SOFTWARE TYPE=

REF NO 14,5025
,53
CAMAC/FORTRAN V INTERFACE SOFTWARE
A GSPONNER, SEN ELECTRONIQUE
SEN
DISK (RDOS), FULL RDOS COMPATIBILITY
MAY 1975
ANY NOVA (WITH/WITHOUT FLOATING POINT)
CC 2023 (SEN)
POST PROCESSOR

DESCRIPTION= =

.54 Support Software I (translators)

READER SERVICE	REF NO 14,5026
CLASS CODE =	,54
TITLE= = = =	S/UNIP AN UNIVERSAL MACRO PROCESSOR
AUTHOR(S)= =	SOFTWARE=PARTNERS
MAINTENANCE BY=	SOFTWARE=PARTNERS
OBTAINABLE FROM	SAME, (SEE INDEX OF MANUFACTURERS)
OPERATIVE DATE=	APRIL 1974
SOFTWARE TYPE =	MACRO PROCESSOR
LANGUAGE =	WRITTEN IN HIGH LEVEL LANGUAGE
COMPUTER =	CAN RUN ON IBM, UNIVAC, CDC, ICL, SIEMENS, ETC,
CAMAC FACILITIES	INCORPORATED IN=LINE FOR FULL=SET IML WITH MACRO PROCESSOR DIRECTIVES

DESCRIPTION= =
S/UNIP IS A LANGUAGE INDEPENDENT MACRO PROCESSOR AND THEREFORE A TOOL FOR MACRO EXPANSION OF EVERY EXISTING OR OF FUTURE PROGRAMMING LANGUAGE. THUS S/UNIP MAINTAINS AND PROCESSES MACROS IN HIGH LEVEL LANGUAGES (FORTRAN, BASIC, ALGOL, PEARL, ETC,) AS WELL AS ASSEMBLY LANGUAGES. S/UNIP OPERATES AS A PRE=PROCESSOR GENERATING SOURCE CODE STATEMENTS FOR SUBSEQUENT COMPILATION, POSSIBLY ON ANOTHER COMPUTER.

READER SERVICE	REF NO 14,5027
CLASS CODE =	,541
TITLE= = = =	A MACRO ASSEMBLER FOR TYPE MBD=11 MICROPROGRAMMED BRANCH DRIVER
COMPUTER =	PDP=11
OBTAINABLE FROM	BI RA SYSTEMS (SEE INDEX OF MFRS)
SOFTWARE TYPE =	MACRO ASSEMBLER (TRANSLATOR)
INTERFACE(S) =	MBD=11 (BI RA SYSTEMS)

DESCRIPTION= =
THE MACRO ASSEMBLER HAS BEEN DEVELOPED TO FACILITATE THE WRITING OF PROGRAMS FOR THE MBD=11 MICROPROCESSOR=INTERFACE. THE ASSEMBLER TRANSLATES PROGRAMS WRITTEN IN MACRO CODE INTO INSTRUCTIONS ACCEPTABLE BY THE MBD=11. UP TO 4K INSTRUCTIONS CAN BE STORED IN THE MBD=11, A FUNCTION OF MEMORY SIZE WHICH GO FROM 256 TO 4K WORDS IN INCREMENTS OF 256 AND 1K. INSTRUCTIONS ARE MICRO=STRUCTURED FORMING A POWERFUL SET.

READER SERVICE	REF NO 14,5028
CLASS CODE =	,541(MACRO11)
TITLE= = = =	MACROS FOR 1533A
AUTHOR(S)= =	MR, HEER
NAME/ACRONYM =	MACRO 1533A
MAINTENANCE BY=	MR, HEER
OBTAINABLE FROM	MR, HEER, ZEL, KFA, JUELICH
AVAILABLE ON/AS	DECTAPE
OPERATIVE DATE=	FEBRUARY 1973
COMPUTER =	PDP=11, MIN 8K 16 BIT WORDS
INTERFACE(S) =	TYPE 1533A (BORER)
MIN SYSTEM CONFIG	DOS V004, 008, 009
SOFTWARE TYPE =	MACRO=SET
LANGUAGE =	MACRO 11
CAMAC FEATURES=	ARE INCORPORATED IN=LINE
ENVIRONMENT FOR =	CAMAC SOFTWARE IS ASSEMBLER
CAMAC FACILITIES	SINGLE ACTION STATEMENTS, SYMBOLIC DEVICE NAMES

DESCRIPTION= =
THIS IS A SIMPLE MACRO SET (NO DECLARATIONS) FOR SINGLE ACTION STATEMENTS. EXECUTION SPEED IS HIGHER (APPROX 30 MICROSECS PER INSTRUCTION, DEPENDING ON TYPE OF INSTRUCTION ON TYPE OF PDP=11). NOT INTERRUPTABLE MACROS (PRIORITY=/)

READER SERVICE	REF NO 14,5029
CLASS CODE =	,541(IML)
TITLE= = = =	MACRO=IML IMPLEMENTATIONS FOR DEC PDP=11 COMPUTERS
AUTHOR(S)= =	M KUBITZ, R KIND, HMI=BERLIN
PUBL, REF, =	CAMAC BULLETIN NO 12, APRIL 1975
OBTAINABLE FROM	M KUBITZ, BEREICH D/E, HMI=BERLIN GERMANY
AVAILABLE ON/AS	ALL MEDIA
OPERATIVE DATE=	1974
COMPUTER =	PDP=11, 16K, 24K, 44K, OR 52K
INTERFACE(S) =	CA=11A (DEC), 1533A (BORER)
MIN SYSTEM CONFIG	DOS V08/09, RSX=11D, RSX=11M
SOFTWARE TYPE =	MACRO SET OF IML (IMPLEMENTED)
LANGUAGE =	PDP=11 ASSEMBLY
CAMAC FEATURES=	INCORPORATED BY MACROS
CAMAC FACILITIES	FULL SET OF IML=MACROS INCLUDING DEMAND HANDLING

DESCRIPTION= =
IML IS IMPLEMENTED ON PDP=11 IN ACCORDANCE WITH THE MACRO SYNTAX AS DEFINED IN THE DOCUMENT ESONE/IML/01 (SEE CLASS ,501 ABOVE). VERSIONS ARE AVAILABLE FOR INTERFACE= CONTROLLERS AND DEC OPERATING SYSTEMS AS MENTIONED IN THE LEFT COLUMN.
IMPLEMENTATION COVERS THE FULL SET OF IML MACROS AND DEMAND HANDLING EXCEPT BLOCK TRANSFER ON SPECIAL LAM, X=ERROR CONTROL STATEMENTS, AND SUBSCRIPT MODE. TRANSFER MODES NOT IMPLEMENTED BY HARDWARE ARE SIMULATED BY SOFTWARE.
I/O TRANSFER INSTRUCTIONS ARE EMBEDDED IN THE MACROS AND ARE PERFORMED DIRECTLY IN ACTION BY THE MACROS.
ADDRESS CALCULATION AT ASSEMBLY TIME GIVES OPTIMIZED ADDRESS CALCULATION AT ASSEMBLY TIME GIVES OPTIMUM RUN TIME CODE. MOST LANGUAGES CAN BE PDP=11 MACRO ASSEMBLER OR FORTRAN (VIA SUBROUTINE CALL).
MEMORY REQUIREMENTS VARY WITH OPERATING SYSTEM AND IF FULL SET IS NEEDED, OR A SUB=SET IS ACCEPTABLE. 16K IS REQUIRED FOR A SUB=SET WITH DOSV08/09 OR RSX=11M AND 52K FOR FULL SET AND RSX=11D.

READER SERVICE	REF NO 14,5030
CLASS CODE =	,543(CATY)
TITLE= = = =	A CAMAC TESTING AID FOR USE ON PDP=11
AUTHOR(S)= =	F R GOLDING, APPLIED COMPUTER SYST,
NAME/ACRONYM =	CAT11
OBTAINABLE FROM	APPLIED COMPUTER SYSTEMS LTD, WENZEL ELEKTRONIK, NUCL ENTERPRISES, (SEE INDEX OF MANUFACTURERS)
OPERATIVE DATE=	1973
COMPUTER =	PDP=11, 4K OR 8K MEMORY REQUIRED DEPENDING ON VERSION
INTERFACE(S) =	C=CSC=11 (WENZEL), 9030 (N,E,)
MIN SYSTEM CONFIG	CONTROL VISTA, READER, PUNCH
SOFTWARE TYPE =	SYSTEM (EXECUTIVE, COMPILER ETC)
LANGUAGE =	CATY (BASED ON BASIC)

DESCRIPTION= =
USERS TEST PROGRAMS ARE TYPED IN AND THEREAFTER COMPILED AND RUN. IT IS POSSIBLE TO EDIT THE PROGRAM AND RERUN IT WITH= OUT HAVING TO RETYPE THE ORIGINAL PROGRAM. CAMAC COMMANDS ARE EMBEDDED IN PROGRAM AS STATEMENT LINES.
CAT11 HAS INTERRUPT AS SYSTEM FEATURE, THE USER MAY TYPE HIS OWN INTERRUPT ROUTINE.
THE CAT11 EXECUTIVE PROGRAM CHANGES SLIGHTLY WITH INTERFACE USED, BUT ALL ROUTINES ARE IDENTICAL.
VERSIONS OF THIS SYSTEM IS ALSO AVAILABLE FROM GEC ELLIOTT (SEE FOLLOWING ENTRIES)

READER SERVICE	REF NO 14,5031
CLASS CODE =	,543(CATY)
TITLE= = = =	A CAMAC TESTING AID = CATY = FOR PDP=11
AUTHOR(S)= =	F R GOLDING, R F CRANFIELD
OBTAINABLE FROM=	GEC ELLIOTT (SEE INDEX OF MANUFACTURERS)
OPERATIVE DATE =	1974
COMPUTER = =	PDP=11, MIN 4K REQUIRED
MIN MEMORY SPACE	
INTERFACE(S) =	PTI=11C/D, IVG=11 (GEC ELLIOTT)
MIN SYSTEM CONFIG	CONTROL TTY OR VISTA, READER, PUNCH
LANGUAGE = =	CATY (BASED ON BASIC)

DESCRIPTION= =
SEE PRECEEDING ENTRY

READER SERVICE	REF NO 14,5032
CLASS CODE =	,543(CATY)
TITLE= = = =	A CAMAC TESTING AID = CATY = FOR NOVA
AUTHOR(S)= =	F R GOLDING, R F CRANFIELD
OBTAINABLE FROM=	GEC ELLIOTT
OPERATIVE DATE =	MARCH 1975
COMPUTER = =	NOVA SERIES (DATA GENERAL), MIN 4K
INTERFACE(S) =	NOVA EXECUTIVE SUITE (GEC ELLIOTT)
MIN SYSTEM CONFIG	CONTROL TTY OR VDU, READER, PUNCH
LANGUAGE = =	CATY (BASED ON BASIC)

DESCRIPTION= =
(SEE CLASS ,501(CATY) AND PRECEEDING ENTRIES CLASS ,543)

READER SERVICE	REF NO 14,5033
CLASS CODE =	,543(CATY)
TITLE= = = =	A CAMAC TESTING AID = CATY = FOR THE
OBTAINABLE FROM=	GEC ELLIOTT
COMPUTER = =	2050 AND 4080 (GEC)
INTERFACE(S) =	EXECUTIVE SUITE FOR 2050/4080 (GEC)
LANGUAGE = =	CATY (BASED ON BASIC)

DESCRIPTION= =
(SEE CLASS ,501(CATY) AND PRECEEDING ENTRIES CLASS ,543)

READER SERVICE	REF NO 14,5034
CLASS CODE =	,543
TITLE= = = =	A BASIC MACRO=11 COMPILER
AUTHOR(S)= =	B BECKS
PUBL, REF, =	CAMAC BULLETIN NO 10, JULY 1974
NAME/ACRONYM =	MABA
MAINTENANCE BY=	B BECKS
OBTAINABLE FROM	B BECKS, ZEL, KFA, JUELICH
AVAILABLE ON/AS	DECTAPE
OPERATIVE DATE=	JANUARY 1974
COMPUTER =	PDP=11, 16K 16 BIT WORDS OF MEMORY
INTERFACE(S) =	TYPE 1533A (BORER)
MIN SYSTEM CONFIG	DOS V08 OR V09, 16K
SOFTWARE TYPE =	COMPILER
LANGUAGE =	BASIC
INCORP TECHNIQUE	IN=LINE
ENVIRONMENT FOR =	CAMAC SOFTWARE IS MACRO ASSEMBLER
CAMAC FACILITIES	SINGLE ACTION STATEMENTS

DESCRIPTION= =
THIS COMPILER TRANSLATES TESTED (INTERPRETIVE) BASIC PROGRAMS INTO MACRO=11 SOURCE CODE. RUN TIME IS IMPROVED BY A FACTOR OF 15 TO 20, EASILY ADAPTABLE TO OTHER CONTROLLERS (MACROS).
OUTPUT CODE LINKED WITH FLOATING POINT PACKAGE CAN RUN ON STAND=ALONE MINI=COMPUTERS.

READER SERVICE	REF NO 14,5035
CLASS CODE =	,543
TITLE= = = =	PRECOMPILER FOR IML SUBSET
AUTHOR(S)= =	W. KNEIS
PUBL, REF, =	CAMAC BULLETIN NO 10, JUNE 1974, AND GFK REPORT KFK2121, GFK, 1975 (IN PRESS)
NAME/ACRONYM =	META=II/X
OBTAINABLE FROM	W. KNEIS, IAK II/CYCLOTRON,GFK, D 7500 KARLSRUHE, POSTFACH 3640
AVAILABLE ON/AS	TAPE, CARDS
OPERATIVE DATE=	JULY 1974
COMPUTERS=	IBM/370 (TRANSL,), CDC 3100 (EXECUTION)
INTERFACE(S) =	IN=HOUSE TYPE
MIN MEMORY SPACE	36K BYTES (MAX 86K BYTES)
SOFTWARE TYPE =	PRECOMPILER (METACOMPILER SYSTEM)
LANGUAGES=	IML (USER), FORTRAN IV (SYSTEM), META=II (FOR COMPILER/WRITING)
INCORP TECHNIQUE	IN=LINE
HOST LANGUAGE =	COMPASS ASSEMBLER (CDC 3100)
FACILITIES =	SINGLE ACTIONS, MULTIPLE ACTION(MA) BLOCKTRANSFER(UBL), AND LAM=, CRATE=, AND SYSTEM=STATEMENTS

DESCRIPTION= =
META=II/X IS A SYSTEM FOR WRITING COMPILERS. THE IMPLE= MENTED VERSION OF THE IML PRECOMPILER IS A CROSS=COMPILER VERSION, I,E, TRANSLATION IS DONE ON AN IBM/370, EXECUTION ON A CDC 3100 COMPUTER. THE OBJECT CODE FOR PRECOMPILING IS THE MNEMONIC COMPASS ASSEMBLER (CDC), THEREFORE AN ADDITIO= NAL ASSEMBLER STEP IS INVOLVED. WITH META=II/X A PRECOM= PILER CAN BE WRITTEN AND TESTED IN A FEW DAYS. THE IML SUB= SET CONTAINS THE DECLARATION= (LOCL, LOCD) AND ACTION=STATE= MENTS (SA, SJU, SJNQ, MA, UBL, ALL LAM HANDLING=, SYSTEM= AND CRATE=CONTROLLER= STATEMENTS).
SET CONTAINS THE DECLARATION STATEMENTS LOCL AND LOCD. THE SUBSET ALSO CONTAIN ACTION STATEMENTS SUCH AS SA, SJU, SJNQ, MA, UBL, ALL LAM=HANDLING STATEMENTS, SYSTEM STATEMENTS, AND CRATE CONTROLLER STATEMENTS.

READER SERVICE	REF NO 14,5036
CLASS CODE =	,544(BASIC)
TITLE= = = =	A PDP=11 BASIC EXTENSION FOR CAMAC PROGRAMMING
AUTHOR(S)= =	I BALS, E DE AGOSTINO, CNEN, ROME
PUBL, REF, =	CAMAC BULLETIN NO 7, JULY 1973
OPERATIVE DATE=	1973
COMPUTER =	PDP=11
INTERFACE(S) =	EXECUTIVE SUITE (GEC ELLIOTT)
SOFTWARE TYPE =	INTERPRETER
INCORP TECHNIQUE	SUBROUTINES IN ASSEMBLY CODE
ENVIRONMENT FOR =	CAMAC SOFTWARE IS BASIC
LANGUAGE =	BASIC (EXTENDED)

DESCRIPTION= =
THE SUBROUTINES WHICH EXTEND THE BASIC INTERPRETER TO CAMAC ARE CALLED BY AN EXTERNAL FUNCTION STATEMENT, WHERE ADDRESS, FUNCTION, ETC, ARE TRANSMITTED AS ARGUMENTS. THE STATEMENT HAS THE FOLLOWING GENERAL FORM= =
LET U = EXF (A1,A2, ,,,, ,A10)
THE FIRST ARGUMENT SELECTS THE APPROPRIATE SUBROUTINE. DATALESS, READ, AND WRITE OPERATIONS WITH DIRECT/INDIRECT ADDRESSING ARE POSSIBLE. ALSO SINGLE OR BLOCK TRANSFERS IN ADDRESS SCAN, REPEAT OR STOP MODES CAN BE PERFORMED.
THE EXTENSION FEATURES LAM HANDLING.

READER SERVICE	REF NO 14,5037
CLASS CODE =	,544(BASIC)
TITLE= = = =	A CAMAC EXTENDED BASIC LANGUAGE
AUTHOR(S)= =	J M SERVENT (SCHLUMBERGER)
PUBL, REF, =	PROC CAMAC SYMPOS, LUXMBG, DEC 1973
NAME/ACRONYM =	CASIC
OBTAINABLE FROM	SCHLUMBERGER (SEE INDEX OF MFRS)
OPERATIVE DATE=	1973
COMPUTER =	PDP=11, 16K WORDS MEMORY
INTERFACE(S) =	ICP11 OR JCC11 (SCHLUMBERGER)
MIN SYSTEM CONFIG	TTY
SOFTWARE TYPE =	INTERPRETIVE LANGUAGE, EXTENDED WITH MACRO=INSTRUCTION GENERATOR
LANGUAGE =	BASIC (EXTENDED)
INCORP TECHNIQUE	IN=LINE CAMAC STATEMENTS
CAMAC FACILITIES	SYMBOLIC DEVICE NAMES, INTERRUPT HANDLING, RE=ENTRANT,

DESCRIPTION= =
STANDARD BASIC IS EXTENDED WITH A SET OF CAMAC RELATED STATEMENTS. EXECUTION TIME FOR A 100 LINE PROGRAM IS ABOUT 10 SECONDS. DECLARATIVE STATEMENTS ALLOW SYMBOLIC REFERENCE OF A MODULE. ADDRESS PARAMETERS CAN BE CONSTANTS OR VARIABLES, EVEN EXPRESSIONS, THUS PROVIDING GREAT FLEXIBILITY. SEVERAL CONTROL FUNCTIONS ARE IN MACRO=STATE= MENT FORM, SUCH AS = TST LAM MODULE (SAME AS MODULE(8)).
SOME SYNTAX CHANGES FACILITATES IMPLEMENTATION OF THE SEMAN= TICS OF IML (SEE ,501(IML)). TYPICAL STATEMENTS ARE = =
ASSIGN ADDRESS = = STATION(MODULE) = (B,C,N,A)
EXECUTING STATEMENT = =
SINGLE TRANSFER = = SA(F,MODULE,A)
MULTIPLE TRANSFER = = MA(F,MODULE,A)
CONTROL FUNCTION = EXEC MODULE(F)
LAM REG OPERATION= CLR LAM MODULE (=MODULE(10))
LAM/INTERRUPT= = = ON LAM(MODULE) DO 100

READER SERVICE	REF NO 14,5038
CLASS CODE =	,544(FOCAL)
TITLE= = = =	FOCAL OVERLAY FOR CAMAC DATA AND COMMAND HANDLING
AUTHOR(S)= =	F MAY, H HALLING, K PETRECZEK
PUBL, REF, =	CAMAC BULLETIN NO 1, JUNE 1971
NAME/ACRONYM =	FOCADAT
OPERATIVE DATE=	1970
COMPUTER = .	PDP=8, 4K OR 8K 12 BIT WORD MEMORY
INTERFACE(S) =	IN=HOUSE CC & INTERFACE
SOFTWARE TYPE =	INTERPRETER (EXTENDED)
INCORP TECHNIQUE	CAMAC EXTENSION OF OVERLAY, IN=LINE CODING OF CAMAC COMMANDS
ENVIRONMENT FOR =	CAMAC SOFTWARE IS FOCAL

DESCRIPTION= =
THE INTERPRETER IS PRIMARILY INTENDED FOR EASILY PROGRAMMED ON=LINE CAMAC SYSTEMS IN NON=TIME=CRITICAL CONTROL AND DATA HANDLING APPLICATIONS AND FOR TEST ROUTINES.
THERE ARE 9 CAMAC STATEMENT TYPES COVERING GENERAL CONTROLS (Z, C, I) AND CAMAC COMMANDS WITH/WITHOUT DATA TRANSFER.
THE GENERAL FORM OF A CAMAC STATEMENT IS =
*A CF,C,N,A,F,FB,MR [,LM,Q]
WHERE SEVERAL PARAMETERS MAY BE OMITTED.

READER SERVICE	REF NO 14,5039
CLASS CODE =	,544(BASIC)
TITLE= = = =	8=USER BASIC UNDER DOS WITH INTERPRETER EXTENDED FOR CAMAC
AUTHOR(S)= =	PFEIFFER, SPICKMAN, CARLEBACH
VERSION= = =	001
MAINTENANCE BY=	D P PFEIFFER
OBTAINABLE FROM	D P PFEIFFER, ZAM, KFA, JUELICH
AVAILABLE ON/AS	DECTAPE
OPERATIVE DATE=	JANUARY 1974
COMPUTER =	PDP=11, 16K OF 16 BIT WORD MEMORY
INTERFACE(S) =	TYPE 1533A (BORER)
MIN SYSTEM CONFIG	DOS V08 OR V09, 16K
SOFTWARE TYPE =	DOS SYSTEM INTERFACE TO CAMAC
LANGUAGE =	BASIC
INCORP TECHNIQUE	EXTENSION OF INTERPRETER

DESCRIPTION= =
THE 8=USER BASIC CAN BE RUN UNDER DOS. A HELP FILE CONTAINS ALL MODIFICATIONS OF THE 1 TO 8 USER BASIC. NO INTERRUPT HANDLING. COMMUNICATION BETWEEN THE 8 USERS IS POSSIBLE BY ONE COMMUNICATION WORD PER USER. EXPANDED ERROR MESSAGE HANDLING. FILE HANDLING EXTENDED. TIME COMMAND ADDED.

READER SERVICE	REF NO 14,5040
CLASS CODE =	,544
TITLE= = = =	ORACL (TM), AN INTERPRETIVE REAL= TIME MONITOR WITH CAMAC SUPPORT
AUTHOR(S)= =	L BYARS, R KEYSER (ORTEC INC)
NAME/ACRONYM =	ORACL (TM)
MAINTENANCE BY=	ORTEC
OBTAINABLE FROM	ORTEC (SEE INDEX OF MANUFACTURERS)
AVAILABLE ON/AS	PAPER TAPE AND DISK
OPERATIVE DATE=	APRIL 1974
COMPUTER =	PDP=11, MIN 5K 16 BIT MEMORY
INTERFACE(S) =	TYPE DC011 (EG&G)
MIN SYSTEM CONFIG	TTY & DC011
SOFTWARE TYPE =	INTREPRETER, SYSTEM MONITOR
LANGUAGE =	PDP=11 ASSEMBLER
INCORP TECHNIQUE	EMBEDDED CAMAC FEATURES
CAMAC FACILITIES	SINGLE OR MULTIPLE INSTRUCTIONS, DEMAND HANDLING IS INCLUDED.

DESCRIPTION= =
ORACL INTERPRETS ARITHMETIC STATEMENTS, PROGRAM CONTROL STATEMENTS, COMMENTS, I/O STATEMENTS, AND HARDWARE CONTROL STATEMENTS AND EXECUTES THE DESIRED FUNCTION.

ORACL (TM) IS A TRADE MARK REGISTERED BY ORTEC, INC.

READER SERVICE	REF NO 14,5041
CLASS CODE =	,544
TITLE= = = =	GENERAL PURPOSE I/O INTERFACE SOFTWARE
AUTHOR(S)= =	F WURM, SEN ELECTRONIQUE
MAINTENANCE BY	SEN
OBTAINABLE FROM=	SEN (SEE INDEX OF MANUFACTURERS)
OPERATIVE DATE =	MAY 1975
AVAILABLE ON/AS=	DISK
COMPUTER = =	NOVA SERIES (DATA GENERAL)
INTERFACE(S) =	ANY (IRRESPECTIVE OF MAKE)
SOFTWARE TYPE=	INTERPRETER
OTHER REMARKS	FULLY RDOS/SOS COMPATIBLE

DESCRIPTION= =

.55 Support Software II

READER SERVICE	REF NO 14,5042
CLASS CODE =	,553(FOCAL/PAL)
TITLE= = = =	A FOCAL INTERRUPT HANDLER FOR CAMAC
AUTHOR(S)= =	F MAY, W MARSCHIK, H HALLING
PUBL, REF, =	CAMAC BULLETIN NO 6, MARCH 1973
NAME/ACRONYM =	FOCALINT
OPERATIVE DATE=	1971
COMPUTER =	PDP=8
SOFTWARE TYPE =	INTERRUPT HANDLER (SYSTEM PROGRAM)

DESCRIPTION= =
FOCALINT IS A GENERAL PURPOSE SYSTEM PROGRAM, ADAPTABLE FOR SPECIAL USE. UP TO 3 CRATES WITH 24 INTERRUPTS EACH CAN BE SERVICED. ONE PROGRAM LINE IN FOCAL IS RESERVED FOR EACH INTERRUPT. SHORT ROUTINES CAN BE TYPED INTO THESE LINES SERVICING THE ASSOCIATED INTERRUPTS, ALTERNATIVELY A FOCAL SUBROUTINE CAN BE USED. CURRENT LINE IN THE BACKGROUND PROGRAM WILL BE FINISHED BEFORE JUMPING TO INTERRUPT ROUTINE AND RETURNS TO NEXT LINE IN THE BACKGROUND PROGRAM AFTER SERVICING.

.57 Test Routines

READER SERVICE REF NO 14,5043
CLASS CODE • .57
TITLE• • • • TEST PROGRAMS FOR SYSTEMS, BRANCH DRIVER & MODULES
OBTAINABLE FROM BI RA SYSTEMS (SEE INDEX OF MFRS)
OTHER REMARKS FOR BRANCH DRIVER MBD•11, SYSTEM TEST MODULE 6102, AND DATA MODULES

DESCRIPTION• •
A SET OF THREE DIAGNOSTIC PROGRAMS ARE SUPPLIED WITH THE MBD•11 MICROPROGRAMMED BRANCH DRIVER, TESTS OF MEMORY, FILE REGISTERS, INSTRUCTION SET, DMA TRANSFERS, INTERRUPTS ETC, A COMPLETE SYSTEM TEST IS SUPPLIED WITH 6102, A CAMAC TEST ROUTINE IS SUPPLIED FOR CAMAC MODULE TESTING FROM THE TELETYPE, NO ASSEMBLY LANGUAGE KNOWLEDGE REQUIRED,

READER SERVICE REF NO 14,5044
CLASS CODE • .573
TITLE• • • • CAMAC TEST PROGRAM
AUTHOR(S)• • DR, B MERTENS, IKP, KFA, JUELICH
AVAILABLE ON/AS PAPER TAPE, ASCII CODE
OPERATIVE DATE• 1971
COMPUTER • PDP•11, 16K OF 16 BIT WORDS MEMORY
INTERFACE(S) • TYPE 2200 (BOREK)
SOFTWARE TYPE • TEST ROUTINES, STAND•ALONE PROGRAMS

DESCRIPTION• •
STAND ALONE PROGRAMS TEST SOME FUNCTIONS OF THE BOREK TYPE 2200 INTERFACE, THE CRATE CONTROLLER AND TWO IN•HOUSE MODULES (C01 & C02), ERROR MESSAGES ARE OUTPUT IF THERE ARE HARDWARE FAILURES,

READER SERVICE REF NO 14,5045
CLASS CODE • .573
TITLE• • • • 3911A TEST CAMAC
AUTHOR(S)• • L A KLAISNER
OBTAINABLE FROM KINETIC SYSTEMS (SEE INDEX OF MFRS)
OPERATIVE DATE• 1973
COMPUTER • PDP•11, 4K OF CORE MEMORY REQUIRED
INTERFACE(S) • TYPE 3911A (KINETIC)
SOFTWARE TYPE • TEST ROUTINE

DESCRIPTION• •
A STAND ALONE PROGRAM FOR EXERCISING A CAMAC SYSTEM FROM A TELETYPE, IT SUPPORTS UP TO 8 CRATES WITH MODEL 3911A UNIBUS *) CRATE CONTROLLERS, A FUNCTION MAY BE EXECUTED ONCE OR REPETITIVELY,

*) UNIBUS IS A TRADE MARK OF DIGITAL EQUIPMENT CORP,

READER SERVICE REF NO 14,5046
CLASS CODE • .573
TITLE• • • • TEST CAMAC
OBTAINABLE FROM KINETIC SYSTEMS (SEE INDEX OF MFRS)
OPERATIVE DATE• 1972
INTERFACE(S) • TYPE KS0011 (KINETIC)
COMPUTER • PDP•11, 4K OF CORE REQUIRED
SOFTWARE TYPE • TEST ROUTINE

DESCRIPTION• •
A STAND ALONE PROGRAM FOR EXERCISING A CAMAC SYSTEM FROM A TELETYPE, IT SUPPORTS ONE BRANCH DRIVER WITH UP TO 7 CRATES, A FUNCTION MAY BE EXECUTED ONCE OR REPETITIVELY,

READER SERVICE REF NO 14,5047
CLASS CODE • .573
TITLE• • • • PDP•11 INTERFACE TEST PROGRAM
OBTAINABLE FROM GEC•ELLIOTT (SEE INDEX OF MFRS)
OPERATIVE DATE• 1974
COMPUTER • PDP•11
INTERFACE(S) • PDP•11 EXECUTIVE SUITE/GEC•ELLIOTT
SOFTWARE TYPE • TEST ROUTINE
LANGUAGE • PAL•11 ASSEMBLER

DESCRIPTION• •
THIS IS A STAND•ALONE PROGRAM USED IN CHECKING THE EXECUTIVE SUITE, A MODULAR PDP•11 • CAMAC INTERFACE, DIAGNOSTIC MESSAGES ARE ISSUED,

READER SERVICE REF NO 14,5048
CLASS CODE • .573
TITLE• • • • TEST PROGRAMS FOR BRANCH DRIVER AND SYSTEM WITH MODULE 6102 AND TYPE A
OBTAINABLE FROM• BI RA SYSTEMS (SEE INDEX OF MFRS)
COMPUTER • • PRIME COMPUTER
INTERFACE(S) • 1260 (BI RA SYSTEMS)
SOFTWARE TYPE• DIAGNOSTIC PROGRAMS
MIN SYSTEM CONFIG BRANCH DRIVER 1260, 6102 CAMAC TEST MODULE/DATAWAY DISPLAY

DESCRIPTION• •
A SET OF DIAGNOSTIC PROGRAMS ARE SUPPLIED WITH THE MODEL 1260 PRIME COMPUTER BRANCH DRIVER, A COMPLETE SYSTEM TEST IS SUPPLIED, BUT REQUIRES MODEL 6102 TEST MODULE,

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* Obtainable from: Office for Official Publications of the European Communities. Luxembourg, P.O. Box 1003.

** Publications in the previous CAMAC Bulletin issue are listed on the inside front cover of this issue.

WAS IST CAMAC?

CAMAC ist ein international verbreitetes Instrumentierungssystem zum Anschluss von Prozessperipheriegeräten an digitale Prozessoren und Rechner für automatische Mess- und Steuereinrichtungen.

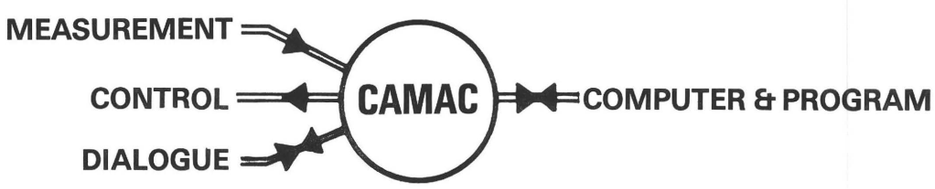
Die System-Spezifikationen umfassen:

— ein digitales Interface, in dem Daten über einen standardisierten Datenweg übertragen werden;
— ein modulares Gerätekonzept zur Anpassung von Peripheriegeräten und Rechnern an den Datenweg.

Mit den modularen, in Überrahmen zusammengefassten Einheiten können viele Peripheriegeräte im Multiplexverfahren über den Datenweg betrieben werden. Weitere Spezifikationen bestehen für parallele und serielle Datenübertragungswege zur Realisierung grösserer Systeme mit mehreren Überrahmen.

CAMAC gewährleistet, dass Geräte verschiedener Hersteller austauschbar oder kompatibel sind und gemeinsam in unterschiedlichen Systemen verwendet werden können. So sind auch Änderungen der Systemkonfiguration aufgrund neuer Anforderungen leicht möglich. Für unterschiedliche Anwendungen stehen kompatible Geräte von Firmen aus vielen Ländern zur Verfügung.

CAMAC ist das Ergebnis einer multinationalen Zusammenarbeit von System-Ingenieuren, aus dem Gebiet der Prozessdatenverarbeitung und **ist ein firmenunabhängiger internationaler Standard, der von jedermann lizenzfrei benutzt werden kann.**



WHAT IS CAMAC?

CAMAC is an internationally used scheme for connecting digital processors and computers to on-line peripherals in systems for Computer Automated Measurement And Control.

There are rules for:

— a digital interface for transferring data on a common highway;
— a modular equipment format for adaptors to match peripherals and computers to the highway.

A compact assembly of these modular units can be used to multiplex many peripherals. Additional parallel and serial highways are defined for larger systems consisting of several of these assemblies.

CAMAC ensures that items of hardware from various suppliers are compatible and can be used together in any system, and also their subsequent reconfiguration to meet changing needs. Compatible products are available from firms in many countries and for uses in different application areas.

CAMAC is the result of multinational cooperation between data-processing system engineers. **It is a non-proprietary international standard that can be freely used by any organisation.**

QU'EST-CE QUE CAMAC?

CAMAC est un concept utilisé sur une base internationale pour relier des processeurs digitaux et des ordinateurs à des périphériques en ligne, dans des systèmes de « Contrôle – Commande Ainsi que Mesure Automatisés par Calculateur ».

Des règles définissent :

— une interface numérique transférant des données sur une interconnexion générale;
— un format d'équipement modulaire pour l'adaptation des périphériques et des ordinateurs à cette interconnexion.

Un ensemble compact de ces unités modulaires peut être utilisé pour multiplexer de nombreux périphériques. Des interconnexions complémentaires, parallèle aussi bien que série, sont également définies pour des systèmes plus importants composés de plusieurs de ces ensembles.

CAMAC assure la compatibilité des éléments matériels fournis par différents producteurs ainsi que leur utilisation conjointe dans tout système; il facilite la constitution et la programmation des systèmes de même que leur reconfiguration consécutive à des changements d'utilisation. Dans de nombreux pays, différentes firmes proposent des produits CAMAC.

CAMAC résulte d'une coopération multinationale entre ingénieurs spécialistes des systèmes de traitement de données. **C'est une norme internationale non brevetée pouvant être utilisée librement par tout organisme.**