COMMISSION OF THE EUROPEAN COMMUNITIES

COM(85) 776 final

Brussels, 23 December 1985

COMMUNITY ACTIONS IN THE FIELD OF MICROELECTRONIC TECHNOLOGY

COUNCIL REGULATION (EEC) NO. 3744/81

THIRD REPORT BY THE COMMISSION TO THE COUNCIL
AND THE EUROPEAN PARLIAMENT

COM(85) 776 final

EXPLANATORY MEMORANDUM

On 7 December 1981 the Council adopted Regulation No. 3744/81 concerning Community projects in the field of microelectronic technology.

Article 9 of this Regulation stipulates that each year the Commission shall forward to the European Parliament and to the Council a report on the development of the activities in the Community falling within the scope of the Regulation.

This document, which is the subject of a written procedure, is the third annual report on such activities.

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INTRODUCTION

On 7 December 1981, the Council adopted Regulation N° 3744/81 [1] on Community actions in the field of microelectronics technology.

The actions were to address two domains of microelectronics : the "CAD for VLSI" (Computer Aided Design for Very Large Scale Integrated Circuits) and the "Equipment for Manufacturing and Testing VLSI".

Article 9 of the Regulation stipulates that the Commission shall each year forward to the Council and the European Parliament a report on the development of the activities in the Community falling within the scope of this Regulation. Before submission of the yearly report, its draft is presented to and discussed with the Consultative Committee which has been set up in order to advise the Commission on the implementation of the programme.

The first activity report on microelectronics (covering the period from the beginning of the programme until 15 July 1983) was submitted to the Council in October 1983 (COM (83) 564 final). The report covered the actions for the introduction of the Regulation, the various phases in the first call for proposals and its results, the reasons which led to the Commission amending the list of projects benefiting from Community support under Regulation N° 3744/81 and publishing a second call for proposals, and the work carried out to coordinate national activities and the dissemination of the results. It also covered the links between the Regulation and the ESPRIT research and development programme.

The second activity report (covering the period from 16 July 1983 until 30 June 1984) was submitted to the Council in October 1984 (COM (84) 567 final) and included the second call for proposals and its results, the

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1 O.J. L376/38 of 30.12.81

progress of the projects launched through the first call for proposals, the work carried out to coordinate national activities and the dissemination of the results.

The present (third) report covers the period from 1 July 1984 until 30 June 1985 and it is organized in four sections.

In section I is presented a summary appraisal of the programme to date. Section II gives a current status summary report for each of the 15 projects that were launched as a result of the two calls for proposals.

In sections III and IV is reported work on the two additional actions of Regulation 3744/81, i.e. on the coordination of national activities and on the dissemination of the results of the supported projects respectively.

I. SUMMARY APPRAISAL OF THE PROGRAMME TO DATE

The programme has been in operation approximately three and a half years with 7 of the projects (launched early 1983) running for about two and a half years and 8 (launched early 1984) for about one and a half years.

Completion of projects is expected to start end of 1985/beginning 1986 but some of the projects will be continued perhaps up to the end of 1987.

At this stage, it is difficult to attempt evaluation of the results that are expected to be achieved in all 15 projects.
However, for most of the projects that are close to completion, it can be said that their achievements appear to be up to the initial expectations or more.
The Commission has discussed and agreed with the Consultative Committee that an overall evaluation of the programme should be made. The evaluation should produce results of both qualitative and quantitative nature. A set of measurable data will be extracted for each project and presented in statistical form and interviews with the major project partners will be arranged to complement the information. However, due to the small size of the programme compared to other Community (e.g. ESPRIT) and national activities, it is doubtful whether the impact of the programme can be extrapolated from these partial data.

It may be appropriate here, without attempting an out of scope analysis, to summarize the position of the Community in the two domains addressed by the programme (i.e. equipment and CAD for VLSI). The Community is still lagging considerably behind U.S. and Japan and it is still dependent on imports for most of the state of the art equipments that are used for the production and testing of VLSI circuits. It is also noted that neither the coordinated efforts (at national or Community level) nor the industry response on the equipment domain appear to be sufficiently intense.

In CAD the situation is more encouraging because the Community appears not to be falling behind. In this case it can be noticed that the various coordinated actions on CAD (e.g. Regulation 3744/81, ESPRIT and national programmes) and industry's positive response to these actions are producing sizeable results.
A noticeable weakness of the Community (that may aggravate the situation in these technological domains) is the scarcity of qualified, highly specialised personnel. This problem has been identified on several occasions and it was the subject of a panel discussion in the fourth CAVE workshop (page 42). The panel concluded that this problem is affecting the universities, research institutes and small and medium companies the most and to a lesser extent the big companies which can bring in new people and re-train existing ones.

The current situation within the framework of the programme can be summarized as follows:

In the equipment domain:

7 equipment projects are under way. It is expected that the completion of these projects will contribute to the ability of the respective Community manufacturers to introduce equipment of increased competitivity in the world market. Already now the bi-directional transfer of know-how between manufacturers and users (partners) in the projects will considerably upgrade the Community technological level in this domain. Some of the equipment and know-how developed are being or will be used in ESPRIT projects that were launched last year or will be launched this year.
For some of the equipment developed under the programme there are early indications that their acceptance by the Community and the world market will be very wide. Such examples are: the "Low Pressure CVD" equipment (project MR-11-ASM), the "E-Beam Testing" equipment (project MR-15-CAM) and the "Plasma Etching" equipment (project MR-12-ELT).
Details are given in the individual project reports in Section II of this report.

In the CAD for VLSI domain :

8 CAD projects are under way. Most of the Community organisations that have any kind of interest in this technical domain are involved in these projects.
Some intermediate results of these projects are already used by the organisations involved in the VLSI circuits design and testing phases. Such examples can be taken from the largest project supported under the programme (project MR-04-CVT) or from much smaller projects such as the MR-03-KUL.

The overall programme :

Subject to confirmation by a formal evaluation of the overall programme, the Commission, based on the individual project reports, is currently of the view that the programme will prove to be a successful one.

Considering the nature of the programme (i.e. advanced R and D in a highly competitive field where large investments are necessary and previous developments are becoming rapidly obsolete) some of the projects may not produce the intended results. However, even for these projects, side-effects such as the development or acquisition of know-how, the upgrading of the Community technological base and the (indirect) impact on the training or re-training of highly qualified personnel, will be substantial.

It is worth noting that the contribution of the programme in establishing the concept of Community-wide cooperation in this type and level of area of technology is considered to be remarkable. In this respect the Microelectronics Regulation 3744/81 programme is considered as one of the most important factors that paved the way to a widely acceptable and successful ESPRIT.

II. CURRENT STATUS OF THE SUPPORTED PROJECTS

The status of the 15 projects listed below is examined in the following pages of Section II.

PROJECT MR-01-IMG

Prime Contractor	: IMAG/MICADO
Participants	: TMC Ltd, SGS-ATES, RTC, PHILIPS SA PARIS, PHILIPS TELECOMMUNICATIE INDUSTRIE HILVERSUM
Title	: CERES (cascade environment for the realisation of electronic systems)
Total Community support	: 4 172 000 ECU
Expected duration	: 30 months
Started	: February 1983
Expected Completion	: November 1985

AIMS AND CONTENT

To develop an integrated CAD system of VLSI circuits, supporting all the design stages from the initial specifications of the circuits to the production of the layout, test and documentation.

Main parts of this system :

- mixed mode simulation with a unique description language covering all the modelling levels (systems, behavioral, register transfer, logical gates, switch and electrical levels)
- fault modelling and fault simulation at different levels
- test data generation for PLAs
- logic compiler and silicon compiler
- general command and control language with integration of all the parts of the system
- graphical editor for circuit description (at all modelling levels)
- floor planner and leaf block design
- electrical modelling.

The main challenge of this programme is to integrate everything around a unique internal data structure.

EXPECTED DELIVERABLES

A set of reports structured in several volumes covering the following:

1) the functional architecture of the overall system together with a short description of the individual tools and pointers to the volumes containing more detailed information.

2) A set of research reports including motivations, overview of the state of the art, result of research and suggested avenues of attack and/or prototype specification where applicable.

3) Draft use documentation with examples on the developed languages and tools.

4) Evaluation reports on aspects of the system.

PROGRESS TO DATE

4 reports have been received, the latest covering the period August 84 to January 85.

The following results have been achieved:

- first mixed mode (RTL-electrical) simulation prototypes
- first concurrent gate level simulation prototype
- PLAs unfolder for test data generation
- specification of: switch level simulator, overall command system, simulation environment, temporal profile and input waveform, description languages, syntax and semantics at all standard description levels
- research has been pursued on: functional faults, parallel and concurrent simulation, decomposition methods at electrical level, formal proofs of assertion, logic compiler.

There has been one contractual change which, however, has still not been ratified. That is the change of ownership of PTI to the new partnership of APT.

A major project review was carried out at the end of January 85. The review panel concluded that CERES was worthwhile whilst expressing reservations on certain aspects of the project resulting in a number of recommendations which are in the process of being implemented. The main outcome is that the project lifetime has been extended up to the end of October 1985 and, during the remainder of the time, the issue of integration will be emphasized at the expense of further work on parts. A further project review, mainly for the benefit of the partners' management will be held in early July.

EXPLOITATION/DISSEMINATION

Continuation of aspects of the project within the industrial partners and the possible setting up of a company, by the Prime Contractor, to market the results of the project.

PROJECT MR-02-RAL

Prime Contractor	: RUTHERFORD APPLETON LABORATORY
Participants	: G.E.C. HIRST RESEARCH CENTRE, UNIVERSITY COLLEGE OF SWANSEA, N.V. PHILIPS EINDHOVEN, TRINITY COLLEGE OF DUBLIN
Title	: Three dimensional semiconductor device simulation including transient and thermal behaviour
Total Community support	: 1 774 000 ECU
Expected duration	: 36 months
Started	: April 1983
Expected completion	: April 1986

AIMS AND CONTENT

The aim is to develop robust and efficient algorithms to simulate either static or transient behaviour of semiconductor (silicon) devices. The behaviour of the device is modelled by solving Poisson's equation, the electron and hole current continuity equations and the heat flow equation by numerical techniques. The model includes expressions for relevant physical phenomena, e.g. band gap narrowing, field dependent mobilities, recombination mechanisms. The equation are to be solved in up to three spatial dimensions.

As well as studying the formulation and discretisation of these equations effort is directed towards improvements in non-linear equations solving, linear equation solving for sparse systems of equations and adaptive meshing techniques.

EXPECTED DELIVERABLES

The end deliverables proposed for the project were recommended sets of algorithms for the simulation of semiconductor devices. These algorithms will be tested by more than one partner on a range of typical semiconductor problems (benchmarks). The algorithms will be described using a pseudo-code language in sufficient detail for easy implementation by other users. The communication of algorithms at this level avoids problems of machine dependence of the deliverables and difficulties in modifying existing software to take advantage of ideas generated in the project.

PROGRESS TO DATE

Three reports received to date, the last one covering the period March 84 to August 84 was received on 10.12.1984. The 4th report is now due.

It now appears that the main proposed deliverables will be modified and negotiations are in progress concerning acceptable alternatives. The project team believes it would be better to produce more robust, better researched 2D algorithms capable of being applied to the 3D case, than to attempt to meet their original, rather ambitious target of a transient 3D solution. The current negotiations are centred on an acceptable benchmark against which the capabilities of the 2D algorithms will be tested.

They also plan to deliver a working 2D code.

EXPLOITATION/DISSEMINATION

Incorporation of the results of the 2D algorithms (extendable to 3D) in a code which would have an, at least, better than state-of-the-art performance. Continuation of the work to build a true 3D simulator in an ESPRIT project.

The 2D algorithms will be available to European industry and a code, incorporating them, produced by the end of the current project.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

A proposal for the extension of the project was submitted and approved for support under the ESPRIT second call (proposal No. 962).
Complementary work by the UK partners is under way in the ALVEY (UK) programme.

PROJECT MR-03-KUL

Prime Contractor	: ESAT LABORATORY, KATHOLIEKE UNIVERSITEIT LEUVEN
Participants	: LABORATOIRE D'AUTOMATIQUE DE MONTPELLIER (UNIVERSITE DU LANGUEDOC), N.V. PHILIPS EINDHOVEN, SIEMENS AG, SILVAR LISCO, BELL TELEPHONE
Title	: Mixed-mode behavioural verification system for MOS VLSI design
Total Community support	: 567 000 ECU
Expected duration	: 36 months
Started	: January 1983
Expected completion	: February 1986

AIMS AND CONTENT

The objective of this project is the development of a prototype system for the verification of behavioural correctness and testability of MOS VLSI design.

Both the top-down Boolean design phase as well as the bottom-up electrical and timing verification phase are envisaged.

EXPECTED DELIVERABLES

New to this system is that an expert system (DIALOG) is used to reduce the enormous amount of simulation time traditionally used in design by zooming in into potential critical trouble spots in the design (guided simulation) based on good design knowledge.

Therefore the expert system guides two Mixed-Mode simulators. One for top-down Boolean design covering functional, gate, switch level including assignable delay modelling (LOGMOS). Also switch-level fault-simulation is under development.

The other simulator is a new electrical/switch level simulator based on dynamic decomposition methods (DIANA) and on segmented waveform analysis (SWAN) whereby one to two orders of magnitude higher performance and same accuracy as SPICE is envisaged.

In order to communicate with this system a user interface including a procedural structural description language (HILARICS) and a symbolic, connectivity based graphics editor as well as compaction system is developed (LUDIEC) together with procedural PLA, ROM generator (PLASCO). The deliverables thus are in the form of the set of programmes LUDIEC, PLASCO, HILARICS, DIALOG, LOGMOS, DIANA, SWAN.

PROGRESS TO DATE

Four reports have been received, the latest covering the period May 84-October 84. The fifth report is now due.

The contractors have not reported any significant delays, but a small delay was reported on the data-base work because of under-estimation of the effort required. Corrective action is being taken.

First phase test versions of all programmes have been built and are being tested by the industrial partners. DIALOG, LOGMOS, DIANA and PLASCO have been successfully used for debugging, simulation and designing of VLSI chips. DIALOG experiments show the feasibility of an expert system for guided simulation while DIANA shows performance improvements of 15 to 25 with respect to SPICE. The underlying principles of SWAN have been tested successfully and now detailed transistor models are being entered in it. A first version of HILARICS is being interfaced to LUDIEC and new DIALOG whereby the knowledge base is built up using a PASCAL-PROLOG like language. Tests using PROLOG are also under way.

To date considerable progress has been made towards the integration of the existing tools as well as in the development of these tools themselves. A new LISP environment LEXTOC for design style description has been implemented. Use of this language allows a remarkable circuit debugging speed of 20000 transistor/hr on a VAX 11/780. All tools are now integrated using HILARICS. The design management system is under test. The only fundamental differences in the outcome of the project will be the extension of the packages currently in the system and the addition of a data-base prototype to the system.

EXPLOITATION/DISSEMINATION

In addition to the in-house use by the industrial partners commercial exploitation of the system (or parts of it) will be undertaken but the participating in the project software house (Silvar-Lisco).

Dissemination is guaranteed through the CAVE workshops, publication of technical papers and the participation of two Universities.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

A proposal for a complementary project was submitted and approved for support under the ESPRIT second call (proposal 1058).

PROJECT MR-04-CVT

Prime Contractors	: CNET, CSELT, FI/DBP
Partners	: CII-HB, CIT-ALCATEL, CENG-LETI, IMAG, INRIA, THOMSON EFCIS, SGS-ATES, ITALTEL, OLIVETTI, AEG-TELEFUNKEN, STANDARD ELECTRIC LORENZ, THE UNIVERSITIES OF BOLOGNA, GENOVA, MILANO AND TORINO, THE UNIVERSITIES OF AACHEN, BREMEN, DARMSTADT, DORTMUND, KAISERSLAUTERN AND KARLSRUHE, GMD, FRAUNHOFER GESELLSCHAFT
Title	: CVT (CAD for VLSI for TELECOMMUNICATIONS)
Total Community Support	: 12 000 000 ECU
Expected duration	: 3 years
Started	: February 1983
Expected completion	: April 1986

AIMS AND CONTENT

The overall objective of the CVT project is to implement an integrated CAD system to be used by system designers, with particular reference to the requirements of the telecommunication field.

From the user point of view, the main features required in the system are:
- to be simple, that is easily accessed by system designer
- to be fast and sure, providing system designers with a way to go from high level descriptions to silicon implementations either automatically (when possible) or with the help of an intelligent assistant suggesting solutions, providing tools and verifying and comparing results.

The system proposed has a modular structure for the following reasons :
- it has to take advantage of the existing tools;
- it has to be flexible, to cope with the foreseen evolution during the time of design methodologies, application tools and supporting hardware;
- it has to be multi-user, leaving to each designer (or Company) the opportunity to assemble the system in the way which best suits his (or its) needs and constraints.

Summarizing, the CVT project is aiming at the following main objectives:

- to define and implement the kernel of the integrated CAD system that is the design data base system and the user interface;
- to originate a complete set of tools for description, analysis and synthesis, to aid the designer during the architectural design phase, going from the initial specifications to floor plans (this is a key item towards the VLSI devices design, establishing a link between the two previously separated worlds of system designers and circuit designers);

- to define a set of coherent criteria for designing complex fault-tolerant, possibly self-repairing architectures, easy to test with the aid of functional test generators;

- to develop symbolic layout tools, which are the VLSI way to layout (as a matter of fact, from one side they provide the circuit designer with an intermediate, easy to use description of the masks, and from the other side they make easier the task of developing tools for automatic placement and routing);

- to provide device models helping both, the technologists to produce the device structures which best suits the TLC application needs, and the circuit designers to obtain effective simulators for circuits manufactured using advanced VLSI technologies;

- to start the work on knowledge based system, which if successful and when successfully integrated with the previously defined system, will give rise to a second generation of integrated CAD systems.

EXPECTED DELIVERABLES

The kernel of an integrated CAD system (user interface and data base management system) plus a set of advanced CAD tools mainly in the areas of a design at system level, testing, symbolic layout and device modelling.

PROGRESS TO DATE

Four interim reports have been received until now. Two major reviews of the project were carried out in October 1983 and June 1985. The results of both reviews were positive.

The following events are also noted:

a. University of Pisa withdrew from the project (did not sign the contract). Their task was taken over by CSELT.

b. A new major task (task 5) was inserted for the integration of the system and shared between CSELT, CNET and FI/DBP and

c. the work programme for one of the subtasks was transferred from Univ. of Dortmund to Fraunhofer Inst. (it was requested by both parties) as of 1st August 1984.

d. The Commission has initiated discussions with the prime contractors for the "future" of the CVT system. The Commission has invited the partners to draft and adopt a plan for the maintenance/evolution/exploitation of the system after completion of the project.

The project is progressing well with only some delays (from 3 to 6 months) in very few of the 36 subtasks.

One of the subtasks has encountered serious problems (i.e. difficulties in implementing a specific theoretical approach) and it was decided to discontinue the work.

In a second subtask the contractors have requested to reduce the workprogramme because it was found that the theoretical and technical difficulties require extensive resources not foreseen when starting the project.

Neither of the above two subtasks is critical for the project. Testing of many of the software tools has started in real applications (e.g. 20.000 transistors chip). Each of the 3 prime contractors is starting to assemble the tools that were developed in their country around a common data base and user interface. The integration of the 3 sub-systems to one system is expected to start in November 1985. In March 1986 it is expected to have operational a single system with most of the tools connected to it. However debugging of the system will have to continue over longer period well beyond the formal completion of the project.

EXPLOITATION/DISSEMINATION

In addition to the in-house use by the industrial partners the system (or part of it i.e. the tools) will be available through the participating research institutes (prime contractors) for use by other Community organisations. The terms of such availability have still to be arranged.

Dissemination is guaranteed through the CVT open workshops, the CAVE workshops, publication of papers and the participation of the University partners.

The first CVT open workshop took place in Torino (April 1984), the second in Darmstadt (April 1985) and the third is planned for April 1986 in Grenoble where it is expected that the integrated system will be demonstrated to invited representatives from industry, research and academia.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

A proposal for the continuation/extension of the project was submitted and approved for support under the ESPRIT second call (proposal No. 802). It is expected that this project may have spin-offs within the RACE programme.

PROJECT MR-05-SIE

Manufacturer	: SIEMENS A.G.
Users	: EFCIS SA, GRUNDIG AG, ITALTEL SpA
Title	: VLSI TESTER 764/780
Total Community support	: 6 712 000 ECU
Expected duration	: 36 months
Started	: January 1983

AIMS AND CONTENT

The aim of this project is the development of VLSI Testers SITEST 764 and SITEST 780. It is planned to develop other VLSI Testers based on a similar technology in order to be able to offer to the customers a whole family of VLSI Testers.
The two VLSI Testers SITEST 764 and 780 differ quite considerably in their performance. The essential features of VLSI Testers are the bit repetition rate with the related system accuracy and the maximum number of Pins per testhead. The corresponding figures are 12 MHz and 64 Pins for the SITEST 764 and 50 MHz and 256 Pins for the SITEST 780.

EXPECTED DELIVERABLES

The users will receive prototype equipment of VLSI Tester 764 in mid 1984 and prototype equipment of VLSI 780 in mid 1985. The users' experience, obtained through the use of the equipment for testing advanced VLSI circuits, will be documented (reports). It is expected that after completion of the project the testers will be fully commercialized.

PROGRESS TO DATE

Four progress reports have been submitted covering the period until end of November 1984 and the fifth is due beginning July 1985. The hardware and software development and testing of the SITEST 764 is completed and the Hw/Sw integration (that has encountered technical problems) is expected to be completed by July 1985. Four hardware prototypes are operational (one installed at Grundig) but complete installations at all users' sites are expected in August 1985. This represents a 15 months delay in the original schedule of the SITEST 764.

Due to the technical difficulties encountered and the considerable increase in cost to develop both the SITEST 764 and SITEST 780, Siemens has announced their intention to "relax" some of the target specifications

of the SITEST 780 and instead to produce an intermediate tester the SITEST 770 with target delivery automn 1988. The additional costs would be covered entirely by Siemens resources.

In view of the above the Commission held (1.2.85) a major project review in order to identify the associated problems (technical or other).

The results of the review can be summarized as follows:
the reasons for the delay can be broadly justified, the inherent difficulties of developing an advanced tester (the SITEST 780) are admittedly great but the timing and the new target specifications for the SITEST 770 (although well above the target specifications given in the Technical Annex of the Regulation 3744/81) are not the optimum compared to the current trends in the world market.

Considering all the factors and specifically the aims of the Council Regulation 3744/81, the efforts of Siemens to develop these testers that fit within their major programme of CAD/CAT integration and the reservations expressed by two of the partners (EFCIS and ITALTEL) in respect to the delays, the Commission has requested all the partners to the project to review their position and workprogrammes. Currently the situation is being examined and discussions are being held by all parties and the outcome is expected in July 1985.

PROJECT MR-06-STL

Prime Contractor	: STANDARD TELECOM LABS
Participants	: STANDARD ELECTRIC LORENZ, BRITISH TELECOM, G.E.C. TELECOM, LABORATOIRE CENTRAL DE TELECOMMUNICATIONS DE VELIZY
Title	: VLSI verification and compilation
Total Community support	: 677 000 ECU
Expected duration	: 36 months
Started	: January 1983
Expected completion	: March 1986

AIMS AND CONTENT

a) To reduce the time taken to produce correct and compact custom VLSI;

b) to formalise a conceptual framework in which designers can manage to think about the behaviour of VLSI systems;

c) to provide computer aids which will help designers to progress from the behaviours conceived for VLSI systems to circuits implementing those behaviours;

d) to establish the role of verification in VLSI design.

The intention is to apply techniques of programming and advances in the theory of computing to chip hardware design. The designer will specify the behaviour of the chip as a programme in a 'behaviour language', simulate the behaviour to show that it conforms to what is expected of it, and transform the behaviour into a layout which correctly implements it. The layout will be formed from cells some of which may have been constructed by the designer in a 'layout language'.

EXPECTED DELIVERABLES

a) Specifications of languages, calculi and user interfaces to computer aids;

b) reports by the user firms on the trials of the computer aids;

c) published technical papers;

d) programmes and related documents on which to base a programme product.

Once initial versions of the languages, the calculus and the computer aids have been devised, their soundness and practical utility will be examined by trying them out on real VLSI systems and verification strategies. The reports on the trials by the users will be relied on in the production of revised versions of the languages, the calculus and the computer aids.

PROGRESS TO DATE

Three reports have been submitted, the first in January 84 covering the first 12 months work, the second in October 84 covering the period 1.1.84 to 30.6.84, and the third in February 85 covering the period 1.7.84 to 31.12.84.
The definition of the Behaviour Language "LTS" has been completed.

The system simulator for the behaviour language has been completed. It is based on the ML language developed at the University of Edinburgh.

Two manipulation tools have been developed. The first is an interactive tool which will partition a set of boolean equations into sets which have limited interconnection. The second is the verifying editor which allows behaviour descriptions to be transformed according to the rules of the calculus underlying the language. At present only a limited set of manipulations are implemented.

On the layout side of the project leaf cell generators have been developed for PLAs and Weinberger arrays. These can be driven directly from the behaviour language.

The hierarchical structure of the behaviour description is used to generate the floor-plan of the chip.

The floor-plan and the leaf cells are used as input by the chip-assembler which creates the final chip layout. The current chip assembler has not been created by the project. A prototype version of the "Astra" system has been loaned by one of the user firms (BRITISH TELECOM) and this will be used in the initial user trials.

The work during the last period reported has been dominated by the user trial and the need to extend the facilities of the programs as the trial progressed.

At the start of the period a revised Designers Guide was issued to the users and they continued developing their chip descriptions. To help the users to come to terms with the language and to animate their emerging descriptions a revised Simulator was released in August. User Workshops were held in August and September to enable all users to become more familiar with the operation of the tools.

Work continued during the user trial on extension of the tools. The number of manipulations available was increased continuously and the manipulator was released as version 1.2 in August, 1.3 in September and 1.4 in October. Similarly there was a continuous program of work on the

simulator. This was released in August in a fast and slow form as version 1.3. There were corrections and improvements released in September and October as versions 1.4 and 1.5.

Work on the Silicon Compiler included programs to automatically generate power and ground grids and also automatically generated pin orientation. A major development was the generic structure generator program which automatically generates layouts from recursive behaviour definitions.

The user trials were completed at the end of October and a review meeting was held. The general consensus was one of continued support and enthusiasm with some specific criticisms. Unfortunately none of the users reached the stage of generating a layout.

During November we received a new version of the ASTRA program. This was installed and is now working. However considerable rewriting of the interface software was required to achieve this.

After the user trial a complete revision of the type assignment program was undertaken. This is now more efficient and reliable but the problem of type assignment still requires more fundamental work.

A revised workplan covering the remainder of the project for 1.7.85 is currently being negotiated.

EXPLOITATION/DISSEMINATION

In house use by the prime contractor and on an agreed basis by the other partners. Contractually it is foreseen (as in all the other projects) that if the contractors do not exploit the results within one year from completion the results should be made available with commercial terms to other Community organizations.

Dissemination through the CAVE workshops. A series of lectures (for the Universities of Aston and Dublin) is based on work done under this project.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

The UK partners are carrying out complementary to this project work under the ALVEY (UK) programme.

It is noted also that British Telecom has allowed the "Astra" system, parts of which were developed under the project MR-09-DFT, to be used by this project for the initial user trials.

PROJECT MR-07-CRK

Prime Contractor	: UNIVERSITY COLLEGE OF CORK
Participants	: MICROELECTRONICS LABORATORY OF QUEENS UNIVERSITY OF BELFAST, ANALOG DEVICES, GEC
Title	: Two and three dimensional numerical modelling of MOS devices
Total Community support	: 366 000 ECU
Expected duration	: 36 months
Started	: February 1984
Expected completion	: February 1987

AIMS AND CONTENT

The project entails the development and application of a suite of computer programmes for numerical analysis of 2D and 3D MOS devices.

A hierarchical range of programmes will be developed, namely:

a) quasi-analytical models (micro-computer)
b) 2D static and transient, finite element and finite difference models (super mini-computer)
c) 3D static, finite element and finite difference models (super mini-computer)

The aims of the project are:

a) to develop finite element and finite difference computer programmes for the simulation of 2D and 3D MOS devices
b) to develop computer graphics packages compatible with and complementary to (a)
c) to develop simplified quasi-analytical computer programmes for use on micro-computers
d) to apply the above programmes to a wide range of MOS devices.

EXPECTED DELIVERABLES

The deliverables shall consist of a series of reports giving :

a) details of the software developed
b) the associated algorithms and numerical techniques
c) details of application to MOS devices of the suite of programmes.

PROGRESS TO DATE

Within the project, this is the current status of the main tasks :

Task 1 - Development of the mesh digitization programme has been completed, save for the final documentation.

Task 2 - This has been fully completed, including documentation. (Deliverables QUB-2.2 and QUB-2.5 are enclosed with this report).

Task 3 - A rudimentary surface plotting programme has been developed.

Task 4 - Algorithms for the Quasi-analytical modelling have been developed.

Task 5 - The 2D FE modelling programme was tested and verified, then it was applied to the analysis of simple MOS devices.

Task 9 - Ad-hoc versions of the 2D FE modelling programme have been written and used for analysis of simple MOS structures. An algorithm was developed, based upon the Frontal method, for the solution of the large sparsely-populated nonlinear matrix equations which are associated with SCD modelling.

EXPLOITATION/DISSEMINATION

The computer programmes could be made available, on a commercial basis, to other European organizations as well as being used and further developed within the project partners organizations.

PROJET MR -08-PHL

Manufacturer	: N.V. PHILIPS GLOEILAMPENFABRIEKEN, Eindhoven
Users	: UNIVERSITE DE DELFT, BELL TELEPHONE, SIEMENS AG, FRAUNHOFER INSTITUT BERLIN
Title of project	: "High resolution Electron Beam Lithography"
Total Community support	: 2 224 000 ECUS
Starting date	: November 1983
Duration	: 3 years
Expected completion	: November 1986

AIMS AND CONTENT

The project is a joint effort of the five partners to further the development of high resolution lithography and its applications. The introduction of high-resolution E-beam lithography equipment will be accelerated, providing a tool for development and production of advanced IC's. Two main application fields will be explored i.e. direct write on wafers with submicron structured patterns and X-ray mask preparation.
The end result will be an improved product offering advanced lithographic equipment from European source. Technology for production of advanced IC's will be made available to European industry and to European maskmaking centre for X-ray masks.

EXPECTED DELIVERABLES

The manufacturer will deliver to the users a number of enhancements for the Electron Beam Pattern Generator (EBPG). Siemens/Fraunhofer will be using the equipment as a tool for the generation of X-ray masks. Bell/Delft will be using it for direct writing on wafers.
Both applications are expected to give results not only for improving the equipment but also for improving the respective parts of the process for manufacturing advanced VLSI circuits.

PROGRESS TO DATE

Three reports have been submitted covering until May 1985. The equipment manufacturer (Philips) has completed most of their tasks and all the equipment enhancements have been installed at the users' premises.

Work by the manufacturer is continued now for improving (second versions) of one hardware subassembly and parts of the system software.

The Siemens/Fraunhofer work programme: preliminary tests on the equipment are done and the work is progressing on the investigation and optimization of X-ray mask writing process (mask technology and resist development process for sub-micron structures). The Bell/Delft work programme: it is well under way making-up for the initial delay (due to late shipment of their equipment enhancements). Preliminary tests on the equipment are done and work is starting on resist and sub-micron patterns, marker detectors for direct writing on wafer and upgrading certain parameters of the equipment, as well as relevant experiments on the process at Bell Telephone (MIETEC facilities). Overall the project seems to advance in a satisfactory way without any major (technical or other) problems.

EXPLOITATION/DISSEMINATION

Commercial exploitation of the enhanced equipment will be undertaken by the manufacturer PHILIPS.

Dissemination as foreseen in the "General Measures" (page 42 of this report).

PROJECT MR-09-DFT

Principal contracting party	: UNIVERSITY OF DELFT
Associates	: I.C.S. Rotterdam, T.H. Eindhoven, T.H. TWENTE Enschede, BRITISH TELECOM RESEARCH LAB., P.C.S. Munich, I.C.N. Enschede
Title of project	: "The cooperative development of a hierarchical VLSI design system"
Total Community support	: 2 260 000 ECU
Starting date	: December 1983
Duration	: 2 years
Expected completion	: January 1986

AIMS AND CONTENT

The design, development and prototype production of a complete, consistent and integrated system for the CAD of VLSI; the system to be implemented on intelligent design stations running a standardized portable operating system under which will be implemented a hierarchical multilevel file system plus management software to provide controlled access to stored relevant design and test data.

A complete set of efficient application programmes will be produced to work with the data and to support a range of design methods for VLSI. The system will be designed with the needs of independent designers in mind and will provide interfaces to fabrication facilities in silicon foundries.
Provision for the communication of individual workstations will be made via local or wide area networks to form a distributed design system which can include larger computational units.

EXPECTED DELIVERABLES

A prototype ICD system will be demonstrated by the end of the project together with full documentation.
Software modules of parts of the system will be produced throughout the project lifetime. There will be a complete report on the results of the project, as well as the standard interim and other reports required by the Commission.

PROGRESS TO DATE

Two reports have been received, the latest covering the period May 84 - October 84. The third report is due now.

In general it may be stated that all partners have achieved considerable progress towards meeting their goals. All major components of the system are now present in prototype form and can be demonstrated.

In addition to the piecewise linear simulator, the project will add to the system a switch level simulator and a timing simulator. Also an interactive and incremental design-rule checker will be added. These items were not specified in the original Technical Annex. The project does not report any major problems. Occasional personnel shortage seems still to occur. The project reports they will be able to produce more than originally promised.

EXPLOITATION/DISSEMINATION

In addition to the in-house use the system will be commercialized by the ICD Co. (NL).

Dissemination is guaranteed through the CAVE workshops and the University partners.

It is expected that a public announcement of the project results will be made in the Custom Electronics and Design Techniques Show (London, 5-7 November 1985).

LIAISON WITH OTHER PROGRAMMES/PROJECTS

A proposal for extension/complementary work was submitted and approved for support under the ESPRIT second call (proposal No. 991).
The UK partner is carrying out complementary work under the ALVEY (UK) programme and the Dutch partners under the NELSIS (Netherlands) programme.

Parts of the "Astra" system (British Telecom) have been developed under this project. The "Astra" system will be used in MR-06rSTL.

PROJECT MR-10-MOV

Manufacturer	:	M.O.VALVE Company Ltd, London
Users	:	UNIVERSITY COLLEGE OF CORK, MOSTEK IRELAND Ltd CII-HONEYWELL BULL
Title of project	:	"Development and evaluation of manufacturing equipment for the production of low cost, high reliability packages suitable for hermetic protection of integrated circuits of high pin count"
Total Community support	:	942 000 ECU
Starting date	:	January 1984
Duration	:	3 years
Expected completion	:	January 1987

AIMS AND CONTENT

a) Define the requirements of the equipment by establishing package specifications as required by the micro-electronic industry with particular emphasis to the one required by each partner.

b) Develop the equipment for the manufacture of the packages of the chosen design.

c) Commission manufacturing equipment and demonstrate large scale production.

EXPECTED DELIVERABLES

1) a. Initial samples) To the users for assessment of the
   b. Final samples) equipment under development

2) Interim and Final reports. The final report will contain equipment description and specification.

3) Possible presentation of work at conferences, technical meetings and reports in technical journals.

PROGRESS TO DATE

Package specification and acceptance procedure, manufacturing method and specification of equipment for package manufacture have been defined during the first period.

The second period has concentrated on defining the method of fabrication. A review meeting took place on 19th March at London and the second interim report covering the period 1.7.84 to 31.6.85 has been accepted.

General Comments

The cooperation between the partners and the management of the project are effective.

The choice of equipment appears good, there were some delays in the delivery of some of the equipments but the production facility implementation at MO-Valve should be completed soon.

The implementation of the production facility mainly includes equipments and dedicated processes for

- laser drilling ans scribing
- silk screening of conductor and vias
- glass sealing
- lead frame production.

The next two periods will lead to the finalisation of production techniques and to the production of initial prototype samples to be assessed by the users (Mostek and Bull).

The problem of the procurement of suitable type of material for package manufacture is not completely solved yet.
Although success has been achieved, the choice of pastes, the control of glass flow during firing and the lead frame production are keypoints of the choosen process; investigations on these subjects are still under way.

Conclusion

Facilities installed and equipment received and commissioned look to be satisfactorily and should be effective. Further evidence of success should be demonstrated after the evaluation of package samples by the users.

EXPLOITATION/DISSEMINATION

The manufacturer intends to commercialize the results of the project. A patent has been applied for.

Dissemination as per "General Measures" described in page 42.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

- The MO-Valve Company together with Thomson have submitted the ESPRIT (2nd call) proposal N° 830 "Packages for High Speed Digital GaAs Integrated Circuits". The proposal has been approved for support.

- CII-Honeywell Bull together with British Telecom, GEC, Marconi Research Centre, have submitted the ESPRIT (2nd call) Proposal N° 958 "High Performance VLSI Packaging for Complex Electronic Systems". The proposal has been approved for support.

- MO-Valve together with other British organizations are involved in the Alvey project "High Performance Packaging Interconnect".

PROJECT MR-11-ASM

Manufacturer	: ASM EUROPE BV, Bilthoven, Netherlands
Users	: MATRA-HARRIS SEMICONDUCTORS, INSA Lyon, PLESSEY RESEARCH CASWELL LTD
Title of project	: "Development of a refractory metal deposition process and related equipment"
Total Community support	: 1 169 000 ECU
Starting Date	: December 1983
Duration	: 3 years
Expected completion	: June 1987

AIMS AND CONTENT

The main aim of this project is the development of advanced equipment for chemical vapour deposition process (CVD) of refractory metals. Initially efforts will be concentrated on tungsten deposition and at a later stage other refractory metals will be investigated. Phase I of the project will cover straight-forward tungsten CVD and Plasma enhanced CVD in order to prove the feasibility and to gain experience at the users premises with all influencing parameters. Phase II will cover CVD process with improved features as deposition, automatic wafer handling, high throughput etc.

EXPECTED DELIVERABLES

Initially two equipment prototypes (Mark I) for low pressure CVD will be delivered to INSA and Plessey and one for plasma enhanced CVD to INSA. After the evaluation of the Mark I two advanced prototypes (Mark II) will be delivered to Matra-Harris and Plessey for further evaluation and optimization.

PROGRESS TO DATE

Two interim reports have been submitted covering the period until the end of 1984 and a third is due in July 1985.

Two equipment prototypes (Mark I for low pressure CVD) have been delivered to the users (Plessey and INSA).

The plasma enhanced version of MKI is now (end of June 1985) operational at ASM and it is planned to be shipped for testing at Plessey (autumn 1985) and INSA (spring 1986).

The partners have agreed, for technical reasons, to prolong by approx. 6 months the period of experimenting with the Mark I and thereafter, based on their results, to commence the development of the updated version of the equipment (Mark II).

Matra-Harris in cooperation with INSA and Plessey have started their workprogrammes on selective deposition of tungsten on silicon substrates and due to the importance given to their workprogrammes their efforts are intensified.
Generally there are some delays in the execution of the project the most serious (about 6 months) being at INSA due to infrastructure problems.

EXPLOITATION/DISSEMINATION

The manufacturer intends to commercialize the equipment under development.

Dissemination as per general measures described in page 42.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

Results from this project are expected to be utilized in the ESPRIT project No. 554. A proposal for complementary work was submitted and approved for support under the ESPRIT second call (proposal No. 1125).

The UK partner is carrying out complementary work under the ALVEY (UK) programme. Philips (Netherlands) has indicated an interest and currently it is examined the possibility that they contribute to the project without Community support.

PROJECT MR-12-ELT

Manufacturer	: ELECTROTECH RESEARCH LTD, Bristol, United Kingdom
Users	: SIEMENS AG, EUROTECHNIQUE
Title of project	: "MINSTREL, the development of a production orientated plasma/reactive ion etching system for all major processes"
Total Community support	: 1 140 000 ECU
Starting date	: November 1983
Duration	: 2 years
Expected completion	: April 1986

AIMS AND CONTENT

The aim of the project is to strengthen Europe as a leading equipment manufacturer for current and future VLSI devices. It is intended to meet the requirements of the worldwide semiconductor manufacturers through the remainder of this decade and into the 1990's. The final system will set new standards of performance and it is hoped that at the time of its introduction it will be significantly more advanced than any competitive system.
Emphasis will be given to such process requirements as throughput, selectivity, uniformity, inhibition of particulates whilst fully automated cassette-to-cassette, minimum floor space in critical clean room areas and ease of service access will be essential features, it is intended that the basic design will allow for varying etching modes to be conducted with minimal adjustment, it will have the ability to process all materials both in current use and planned future technologies, and will utilize new concepts in controlled environment for lowering particulate contamination.

EXPECTED DELIVERABLES

The manufacturer will deliver to the users initially a single chamber equipment prototype and later on a four chamber prototype.
Both users will test and improve the equipment carrying out their own R&D project. The end goal is the application of the equipment (system) for the preparation of 1 um line resolution for very high scale MOS circuits in an industrial environment.

PROGRESS TO DATE

Two progress reports have been submitted covering the period until end of October 1984 and a third is due now.

Two single-chamber prototypes have been delivered to Siemens and Eurotechnique (April and July 1984 respectively) and one four-chamber prototype has been delivered (April 1985) to Siemens. A second four-chamber prototype is under completion and it will be delivered to Eurotechnique in August 1985.

In Siemens the single-chamber prototype is currently employed in the development of aluminium etching processes and the four-chamber prototype is in fairly advanced debugging phase.
In Eurotechnique the single-chamber prototype is being used for polysilicon etching and the facilities for accepting the four-chamber prototype are under preparation.

There has been a delay of about 6 months in the delivery of the four-chamber prototypes but otherwise the workprogramme is progressing without any other major (technical or other) problems.

EXPLOITATION/DISSEMINATION

The manufacturer intends to commercialize the equipment under development.

Dissemination as per general measures described in page 42.

PROJECT MR-13-BUL

Principal contracting party : CII-HONEYWELL BULL, Paris

Associates : G.E.C. London, PLESSEY RESEARCH CASWELL LTD, UNIVERSITY OF DUISBURG, UNIVERSITY OF AACHEN, AUTOMATION AND MICROELECTRONICS LABORATORY OF MONTPELLIER (LAMM)

Title of project : "A CAD system for VLSI testing"

Total Community support : 2 279 000 ECU

Starting date : February 1984

Duration : 3 years

Expected completion : February 1987

AIMS AND CONTENT

Upgrade present test methods and CAD tools to cope with the needs of VLSI of late 80's.

Two main phases:

A) Analysis and specification :

Starting from the failure modes analysis of the most commonly used IC technologies and functional blocks

- define a method based on a combined implementation of built-in devices and comprehensive test generation algorithms
- Specify the CAD software to be developed and the associated data processing framework (including special purpose hardware if necessary).

B) Development and Integration :

- develop the CAD software modules and integrate them in a flexible integrated system, with easy to use interfaces.
- Implement examples of specific hardware to demonstrate feasibility and performances.

EXPECTED DELIVERABLES

- Reports on VLSI test methodology and design rules for testability
- Demonstration by examples of the capabilities of the CAD software system developed.
- Specifications of special purpose hardware (if any).
- Proposal of standards (if any).

PROGRESS TO DATE

Two reports have been received, the latest covering the period 1.5.84 to 10.84. A third report is now due.

Progress to date is as follows:

The period under review (named Period 2 of the CATE Project) from 1.5.84 to 31.10.84, was the first important period of the project after the introductory 2 months phase reported in the first Interim Report (E2/BU/C011).

With a global level of manpower of 74 person X months close to the forecasts, that is to say about 13% of the total scheduled effort during the 7 periods of the project, the Period 2 brought important results in the fields of:

- Working methods and communication means between the participants
- General framework of the project
- Design for test where some important choices have been already proposed.

The first five technical deliverable reports have been issued summarizing some of these results; nine other deliverables are under preparation for the next period.

EXPLOITATION/DISSEMINATION

The results of this project will be fully exploited by the participants within their own organizations as well as contributing to a parallel ESPRIT project. Other spin-offs from the project, especially those developed by the Universities, are capable of further, possibly, commercial exploitation within Europe.

PROJECT MR-14-EKC

Manufacturer	:	ELEKTRONIK CENTRALEN, Hoersholm, Denmark
Users	:	BRITISH TELECOM, SGS-ATES, MATRA S.A.
Title of project	:	"Static and dynamic burn-in systems"
Total Community support	:	1 841 000 ECU
Starting date	:	December 1983
Duration	:	3 years
Expected completion	:	March 1987

AIMS AND CONTENT

To develop and manufacture a general purpose dynamic burn-in/test system for complex integrated circuits.
A first prototype will be developed and manufactured to agreed specifications and delivered to the users. This will then be upgraded with the help of the feedback from the users to form the basis of a commercially realisable product.

EXPECTED DELIVERABLES

The users will start to receive the first prototype equipment from Mid 1985. Reports on system performance will be produced by the users and a final version of the equipment will be provided allowing final trials and reports by the end of the project.

PROGRESS TO DATE

Two reports have been received covering until the end of 1984 and a third is due in July 1985.

During this period development work has been carried out on all hardware sub-assemblies and software modules of the system.

The delivery of the first prototype SCANTEST 10 system is scheduled with a small delay (3 months) for October 1985. The users main workprogramme will start after the delivery of the system and until that time their participation is restricted to consultancy and assistance in the definition of the various technical specifications of the system.

Generally the work is progressing well, without any major problems (technical or other) except of the small delay mentioned above.

EXPLOITATION/DISSEMINATION

The manufacturer intends to sublicense the commercial exploitation of the equipment to another Danish company.

Dissemination as per general measures described in page 42.

PROJECT MR-15-CAM

Manufacturer	: CAMBRIDGE INSTRUMENTS LTD, Cambridge
Users	: SGS-ATES, CSELT Turin, Standard Elektrik Lorenz AG, SIEMENS AG
Title of project	: "Electron beam testing equipment for VLSI"
Total Community support	: 966 000 ECU
Starting date	: December 1983
Duration	: 2.5 years
Expected completion	: December 1986

AIMS AND CONTENT

The development and manufacture of an electron beam testing system for the testing and evaluation of advanced VLSI. The system to be based on the voltage contrast development work carried out at Siemens and the scanning electron microscope (SEM) systems developed by Cambridge Instruments. The equipment will be commercially realized by Cambridge Instruments. The development and manufacturing work will be carried out in 3 overlapping phases: Phase I - Development of basic equipment and extension of techniques; Phase II - Enhancements and transfer to the new instrumentation; Phase III - Upgrading of instrumentation to provide an automated system utilising the results of the earlier phases. Users will participate between Phases I and II and II and III.

EXPECTED DELIVERABLES

The major deliverables are the prototype equipment EB1, delivery from manufacturer to user to commence from Mid 1984, and the final equipment version EB2. There will also be user trials reports and a full report of the outcome of the project.

PROGRESS TO DATE

There was an initial lack of proper communication with the manufacturer that has been eventually settled.

The project has sustained a number of difficulties (including some modifications in the technical requirements of the users) that resulted in a delay of approx. 9 months.

The first EB1 unit was delivered to Siemens in Nov.1984 and the studies on the dynamic voltage measurements have started.
The second unit was delivered to CSELT/SGS in June 1985 and the third is expected to be delivered to SEL in July 1985.

The state of the above equipment prototypes is fairly good (approx. 75% of the target specifications have been achieved) and it is expected that it will improve during the second half of 1985.

It is expected that the manufacturer and users will intensify efforts for the prototype upgrading (EB2) and full computer control (EB3) so that to eliminate a good part of the 9 months delay.

There are good indications that the improved equipment will find a good response when (eventually) it is marketed.

EXPLOITATION/DISSEMINATION

The manufacturer intends to commercialize the equipment under development.

Dissemination as per general measures described in page 42.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

SGS-ATES and CSELT are participating in ESPRIT project No. 271 where the equipment developed under this project will be enhanced for automatic validation of ICs.

III. COORDINATION OF NATIONAL AND COMMUNITY ACTIVITIES

1. National Activities

Articles 1 to 3 of Regulation No. 3744/81 make provision for the setting up of an information and consultation "system" between the Member States and the Commission. The system covers all information of a scientific, economic and financial nature concerning any activities under the authority of the Member States in progress on the date the Regulation enters into force or contemplated after that date.

Because of shortage of staff when the programme was launched, the Commission felt it preferable to give priority to the direct support operations covered by the Regulation.

The Commission submitted (June 14th, 1984) for discussion in the Consultative Committee a proposal for a systematic approach for cross-exchange of information and concertation of activities.

Discussions (in subsequent meetings) on this subject concluded that although the Regulation had envisaged the setting up of a formal mechanism for information exchange between Member States and the Commission, there had been difficulties in reaching agreement on the form it would take. In any case much of the relevant information was being obtained informally. It was therefore agreed that, since there were now other Community programmes such as ESPRIT under way covering a broader area of technology, the procedure would be tackled within the framework of these programmes.

Within ESPRIT this activity will be continued for a much longer period than within the Regulation 3744/81 the validity of which expires at the end of 1985.

2. Community Activities

The work carried out on microelectronics within the framework of the ESPRIT[2] programme represents both a continuation and an expansion of the activities undertaken pursuant to Regulation No. 3744/81 and constitutes an indispensable complement to the development of advanced microelectronics within the Community.

Some of the ESPRIT projects either are drawing on information from or are follow-ups of projects launched under the Regulation No. 3744/81. This applies not only to CAD projects but also to equipment projects and to the (equipment) users research programmes. Some examples are: on CAD the ESPRIT project 802 that it is building on the results of project MR-04-CVT and on equipment the ESPRIT project 271 that is expanding work undertaken by the "equipment users" of project MR-15-CAM. Further details were given in the individual project reports.

The Commission is following closely these cases in order to facilitate the flow of information between the different programmes and projects.

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2 Ref. O.J. L67 of 9.03.1984, p. 54
O.J. L81 of 24.03.1984

IV. DISSEMINATION OF THE RESULTS

In each of the individual project reports reference is made to the various forms of utilisation and dissemination of the results.

The common elements (policy) to the dissemination that were followed troughout this programme can be summarized as follows :

1. Specific measures

The dissemination of the results for the CAD projects which are granted support under the Council Regulation 3744/81 is insured within the framework of the CAVE (CAD for VLSI in Europe) workshops.
The attached annex 1 gives an overall view of the work which has been done during the first 5 workshops.

For the dissemination of the results of the CVT project (the largest CAD project supported through Regulation 3744/81) two workshops were organized in Torino (12 and 13 May 1984) and Darmstadt (17, 18 and 19 April 1985), where attendees from all Member States were invited. The third and last workshop will be organized in 1986 in Grenoble.

The nature of the equipment projects involving higher users-suppliers relationship is somehow different and, specific measures for the dissemination of the results have not been adopted on top of those envisaged through the general measures described below.

2. General measures

It has been provided in all contracts that, upon completion of the projects, the contractors will produce a separate (from the final) report suitable for publication. Publication of papers in recognized technical journals and delivery of lectures (specifically in projects where there is university participation) are additional means envisaged for the dissemination of the results.
The contractors are obliged within one year from completion of the projects to exploit commercially the results either themselves or to make them available to third parties in the Community.

ANNEX 1

REPORT ON THE CAVE WORKSHOPS

(Computer Aided design for Very large scale integration in Europe)

Background

The special aim of the CAVE workshops, which are held twice yearly, is to be used as one of the vehicles for disseminating the results of CAD for VLSI projects supported under the Council Regulation 3744/81. Also, the workshops are used to foster personal relationships at a technical level in order to smooth the path of future collaboration in the Community in R and D in CAD for VLSI. This is rather different from many technical workshops. In order to be successful the CAVE workshops must atract a kernel of attendees who will attend regularly so that personal relationships can be built up. There is also a smaller percentage of different attendees at each workshop to ensure fresh input of ideas. Most of the CAD for VLSI topics are covered at each workshop. The location of the workshops is rotated amongst the Member States. A technical committee comprised of representatives from all Member States is assisting the Commission in the organisation of the workshops.

Statistical information on the participants of the workshops is given in the attached Table 1.

First Workshop

This was organised in l'Aquila, Italy, on 24-26 May 1983 and it covered 5 CAD topics:

- simulation and modelling
- CAD systems
- testing
- layout and
- design methodologies.

Second Workshop

This was organised in Villard-de-Lans, France, on 12-14 December 1983, and it covered 4 CAD topics:
- VLSI design workstations
- WLSI testing
- compact MOS modelling and
- autolayout

For the first time a panel session on "collaboration in CAD R&D" was also held.

Third Workshop

This was organised in Rungsted, Denmark, on 14-16 May 1984 and it covered 4 CAD topics:
- specification languages
- expert systems for VLSI CAD
- multi-level simulation and
- silicon compilation

Two panel sessions on "Portability and compatibility of CAD tools" and on "EEC funded projects in CAD" were also held.

Fourth Workshop

This was organised in Het Meerdal, The Netherlands, on 11-13 December 1984 and it covered 4 CAD topics:
- tools for testability
- Interfacing process, device and circuit simulation
- Design Management and Databases
- Floor-planning

One panel session on "Education and Training in CAD for VLSI".